A Study of the Thermomechanical Reliability of Solder Joints in Surface Mount Electronics Technology

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DECLARATION

I certify that this work has not been in substance accepted for any degree, and not concurrently submitted for any other degree other than that of Doctor of Philosophy (PhD) of the University of Greenwich. I also declare that this work is the result of the investigations I carried out except where otherwise identified by references and that I have not plagiarised the work of others.

Signed by Jude E. Njoku ----------

(Student)

Date: ----------

Signed by 1st Supervisor ----------

Date: ----------

Signed by 2nd Supervisor: ----------

Date: ----------

DEDICATION

"To God and to all who has departed."

The dedication of this PhD thesis is to the greater glory of the Almighty God and to those whom I know that passed away from the family. The people include late grandpa and ma, Nze & lolo Patrick Ebegbulem Njoku-Iwuoha (Papa & Mama Nkeukwu). The next was the brother of Grandpa, late Chief James Chkwunyere Njoku (my granduncle and onye isiala II) & his lolo, late Madam Philomena (Mama Joe). The demise of the beloved parents from whom into this world I came, late Nze Matthew & Lolo Margarita Ugbodiya Ebem Njoku and that of the most cherished late brothers, Brother Daniel Ezealaeboh, and Bro Engr. Richard Ewusie Ebem Njoku were most painful, and to them, and together for their remembrance, this thesis is devoted. This dedication will not be complete without the inclusion of the late uncle, Mazi Ansellam Omasirim Ebem Njoku and a late aunt and her late husband, Madam P. C. Chukwu (nee Njoku) & Chief Pius Chukwu. Next dedication goes to the extended family favourite uncles and aunts, late Mazi Kirian & his wife Rosanna, late Mazi Anthony & his wife Gladys, and late Mazi Basil all Onyeneghe Njoku. The thesis also is dedicated to late Mazi & lolo Daniel Egbuho Njoku (an ex-Biafra veteran soldier) and late Mazi Sabastin Onuohachukwu & his wife lolo Urediya Ogu Njoku. Also remembered for this devotion are late Mazi & lolo Martin Ogu Njoku, late Nze & lolo Odomagwu Iwuoha Njoku (onye isiala I) and the late Chief & lolos Isaac Iwuoha Njoku (ex-2nd world war veteran soldier and warrant chief). Nonetheless, those cousins of mine who passed into glory are not left out in this remembrance and dedication. Dede Linus Egbuho Njoku (Biafra war victim soldier), Longinus, Joseph (Gwobe) & Kenneth Onye Njoku, Miss Bernadeth Chikamnele & Mr Bruno Ugochukwu Ebem Njoku, Mr Ignatius Opkabi and Isaac Ebere Iwuoha Njoku, Michael Njoku's wife; late Juliana, Ngozika and Cyprian Ogu Njoku are all remembered. Finally, the thesis is also dedicated to our good neighbours, late Mazi Leo & lolo Elizabeth Iwuji and their late son and sister-in-law, Patrick and Jude Iwuji's wife. Late Mr & Mrs Mathias Iwuagwu (mama & papa Franca) and lately late Mazi Christopher Onuohaegbu Iwuagwu, all who has departed and rested onto the Lord; may their gentle souls rest in perfect peace (RIPP) - Amen.

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ABSTRACT

Solder joints have been an integral part of any electronic assembly. They serve as both the electrical and mechanical connections between surface mount component and the substrate. This function is crucial in Surface Mount Technology (SMT) owing to its capability in supporting the realisation of high density, functionality and performance of electronic devices. With the increase in miniaturisation of electronic components, enabling the manufacture of high-density products, the mechanical reliability of small component solder joints has become critical. The criticality increases with operations at elevated temperature and harsher ambient conditions. Severe conditions include vibration and shock which under-the-bonnet automotive electronics experience during vehicle drive. The transactions occurring in this ambient accelerate the damage of solder joints, which causes early crack initiation that later, propagates across the joint leading to system's failure over continued operations.

This PhD research work studies and evaluates the thermo-mechanical reliability of lead-free solder joints in surface mount electronic components assembled on substrate Printed Circuit Boards (PCBs). In carrying out the research, activities and factors, which influence solder-joint thermo-mechanical reliability, have been investigated. The events and factors are soldering processes, ambient temperature, joint's architecture, solder material composition, solder-joint common defects and duration of device operation.

Two type of components used for the investigation were Ball Grid Array (BGA) and a chip resistor. The designed research studies used the techniques of the Design of Experiment (DoE) and Taguchi methods. After conducting the trial tests that served as control experiments, next was the formation of test vehicles with components assembled on PCBs using lead-free solder paste, and later subjected to different thermal loading conditions. Numerous mechanical tests were carried out using the assembled test vehicles to determine, quantify and evaluate the effects of the activities and factors on the degradation of the solder joints. Fractured solder joint surfaces, which resulted after the shear test, were inspected and analysed for brittle and ductile mode of failure. The examination and analysis of the microstructure were done using the Scanning Electron Microscopy (SEM). The Coffin-Mansion equation helped in calculating the accelerated factor of solder joint degradation at field service conditions. The shear strengths of the joints were evaluated to determine the thermo-mechanical reliability of the solder joints.

The findings of this investigation are significant, and from the observations, the shear strengths of solder joints depend on the stages and values of the reflow parameter settings. A combination of high preheat, and low peak temperature produces joints with high shear strengths. Further studies on reflow parameters show that these two factors have a significant main effect on the integrity of solder joints. Also, results found show that elevated temperature operations changed the microstructure and morphology of the solder joints. Change from fine to coarse microstructure resulted in a decrease in shear strength of the joints. The joints are found to fail predominantly by brittle fracture occurring mostly at the boundary between Intermetallic Compound (IMC) layer and the solder bulk. From the results, the standoff height of a solder joint is adjustable as desired by a controlled variation of the bond pad diameter on the PCB. The standoff height of a solder joint is found to significantly impact on the bond structural integrity such that the lower the standoff height, the greater the shear strength of the joint. More results demonstrate that paste type, activation temperature used in reflow soldering process and the pad surface finish on the substrate PCB play a substantial role in determining the percentage of voids in solder joints. Besides, the results show that for minimum voiding in lead-free solder joints of Ball Grid Array, the paste type 97 may be used instead of type 96; an activation temperature of 200 °C should be utilised instead of 190 °C, and a Ni surface finish would be better than Cu surface finish. Other results establish that the magnitude of degradation of solder joints in electronic assemblies is linearly dependent on the duration of the device operations in the field. The cause of the degradation is found to be a change in the solder microstructure and the formation of CSH as well as the growth of brittle IMC layer in the joint.

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TABLE OF ABBREVIATIONS

ABS	Automatic brake system
AECU	Auto electronic control unit
AF	Acceleration Factor
AFM	Atomic Force Microscopy
AGS	Automatic Gear Selection/System
APS	Advanced planning and scheduling
AR	As Reflowed
ASIC	Automobile specific integrated circuits
ASSP	Application-specific standard products
ATC	Accelerated thermal cycling
BGA	Ball Grid Array
BSE	Backscattered electrons
CME	Coffin-Manson's Equation
CMP	Chemo-mechanical polishing
COB	Chip-on-boards
COTS	Commercial-off-the-shelf
CPU	Central Processing Unit
CSH	Component standoff height
CSP	Chip scale package
CTE	Coefficient of thermal expansion
CuSF	Copper surface finish
DCA	Direct chip attach
DfM	Design for manufacturability
DfT	Design for testability
DIP	Dual-Inline-Packages
DMM	Digital Multimeter
DoE	Design of experiment
DSC	Differential scanning calorimetry
DSP	Digital signal processing
ECA	Electronics Components Assemblies
EDS	Energy dispersive spectrometer

EDX	Energy-dispersive X-ray spectroscopy (EDS, EDX, or XEDS)
ENIG	Electroless nickel immersion gold
EOL	End of life
EPMA	Electron probes microanalysis
ESCS	Electronic stability control systems
The EU	European Union
FC	Flip Chip
FCB	Flexible Circuit Board
FCOB	Flip chip on board
FEA	Finite Element Analysis
FEM	Finite element method
FPGA	Field Programmable Gate Arrays
FSB	Favourable solder bump
GWL	Gull Wing Leads
HATT	Highly accelerated test temperature
HAZ	Heat affected zone
HTE	High temperature electronics
IC	Integrated Circuit
IMC	Intermetallic compound
IPC	Interconnecting and Packaging Electronics circuits
JEM	Journal of Electronic Manufacturing
LCCC	Leaded Ceramic Chip Carrier
LCT	Lifecycle time
LF	Lead-Free
MDS	Monocrystalline diamond suspension
MTTF	Mean time to failure
OEM	Overall equipment manufacturers
OSP	Organic Solderability Preservatives (OSPs)
PBGA	Plastic Ball Grid Array
PCB	Printed circuit board
PLCC	Plastic Leaded Chip Carrier
PnP	Pick and Place
PSD	Particle size distribution
PWB	Printed Wiring Board

R&D	Research and development
RoHS	Restriction of Hazardous Substances
RPTs	Reflow Peak Temperatures
RSS	Ramp-Soak-Spike
RTS	Ramp-To-Spike
SAC	Tin-Silver-Copper (Sn-Ag-Cu)
SEM	Scanning Electron Microscope
SJs	Solder Joints
SJR	Solder joints reliability
SJSS	Solder joints shear strength
SJT	Solder joint technology
SLICC	Slightly Larger than IC Carrier'
SMAAT	Surface mount area array technology
SMAT	Surface Mount Assembly Technology
SMC	Surface mount component
SMD	Surface mount devices
SMEC	Surface mount electronic components
SMT	Surface mount technology
SnSF	Tin Surface Finish
SO	Small Outline
SOH	Standoff height
SSS	Solder shear strength
TAL	Time above liquidus
THAAD	Theatre High-Altitude Area Defense
THC	Through-Hole-Component
THT	Through-Hole-Technology
TMA	Thermomechanical analysis
TMC	Thermomechanical Cycling
TMF	Thermomechanical fatigue
TMR	Thermomechanical Reliability
UBM	Under-bump metallisation
USB	Unfavourable solder bump
VHG	Vernier Height Gauge
WEEE	Waste from electrical and electronics equipment

LIST OF NOTATIONS

Name	Symbol	Dimension Unit
Acceleration Factor	AF	-
Activation energy in electron	Ea	Volts (eV)
Average Shear Force	F	N
Average shear strength	τ	N
Base of the natural logarithms	E	-
Boltzmann constant	K	eV/K
Cycle Frequency in the field	F_{field}	$24h^{-1}$
Cycle Frequency in the Laboratory	F_{test}	$24h^{-1}$
Field temperature maximum	T_{max} field	K
Laboratory temperature maximum	T_{max} field	K
Mean Time before Failure	$\emptyset$	-
Number of Failures	R	-
Failure Rate over time	$\lambda(t)$	-
Failure Rate inverse	$\frac{1}{\lambda}$	-
Number of field temperature cycles	N_{field}	-
Number of test temperature cycles	N_{test}	-
Shear Area	A	m^2
Temperature difference in the field	ΔT_{field}	K
Temperature difference in the Laboratory	ΔT_{test}	K
Time for a cycle	T_{cycles}	mins
Time for test	T_{test}	A
Time in the field	T_{field}	A
Total time	T	mins
Junction Temperature	T_J	ºC

Chapter 1: Introduction

1.1 Background

In Surface Mount Technology (SMT), the solder joints thermomechanical reliability of area array packages such as Ball Grid Arrays and Chip Scale Packages (BGAs & CSPs), including Flip Chips on Board (FCOB) under field use or safety critical operating conditions are very vital to the electronic industry. The solder joint though often characterised by rough or lumpy surfaces called cold joints, emanating from soldering and operational environment, has many reliabilities related issues. It experiences cyclic thermomechanical fatigue loads caused by Coefficient of Thermal Expansion (CTE) mismatches or thermal gradients occurring at various parts of a package or an assembly. These problems range from misalignment of components on substrate pad, pad lifting, partial wetting, dewetting or nonwetting, solder weakening, necking, pop-corning, bridging, voiding and to solder joint cracking and failure.

It is thus imperative to note that dealing with the reliability challenges in solder joints have been a significant concern to the electronic industry. However, the future of the 21st Century Integrated Circuit (IC) boards is comprised of BGAs, chip capacitors and resistors and designed to reach ultimate circuitry density. The needs for a high volume production and more Input-Output (I/O) terminals that require higher device power are also critical with burning concern to the industry (Menon, 2010; Hong, Yuan and Junction, 1998). Following the advancements in IC technology, especially considering low cost, small size and multi-functional electronic products, electronic packaging and the niche consumer and an overall market demand, there is a need to find an innovative approach to discharge these requirements. In response to these, however, packaging related areas such as design, packaging architectures, materials, processes and manufacturing equipment are all changing at a faster pace with significant challenges that require attention and which are under consideration by the author.

Moreover, the continuing demand towards high density and low profile packaging has accelerated the development of ICs typical of BGA devices as used in surface mount technology of Direct Chip Attach (DCA), flip chip, and CSP. One of the most commonly used BGA devices is the plastic ball grid arrays, PBGAs (from Topline), of which its solder joints are relatively of weak structural compliance (Schubert et al., 1998; Yao, Qu and Wu, 1999). Nevertheless, the reliability of BGA/Flip Chip (FC-BGA) interfacial adherence, mechanical and electrical compliance when mounted on a Printed Circuit Board (PCB) mainly depends on the integrity of solder joints assembly (Yao, Qu and Wu, 1999; Lea, 1988).

This thesis focuses on the reliability of lead-free solder joints, especially areas where, or of less given attention by previous researchers. The area of interest includes but are not limited to reflow profile parameters, the impact of shear speed, effect of Component Standoff Height (CSH) on temperature variations and pad sizes, the influence of Intermetallic Layer (IMC) thickness that constitutes the volume and height of the joint. Others include reliability challenges posed by voiding in solder joints of electronic components and understanding the factors underlying the long-term reliability assessment of solder joints; including their failure rate, Mean Time To Failure (MTTF) and Mean Time Between Failure (MTBF) (Sangwine, 1994).

Furthermore, the determination of optimal CSH in a BGA/FC-BGA for reliable solder joint operations at high-temperature excursion and thermal cycling condition is the primary goal and a considerable part of this research. A description of an area array package of a typical BGA solder joint is in Figure 1.1. Area array packages offer the advantages of high I/O devices. They possess shortest electrical connection; and hence improved electrical performance, low cost and rapid production in microelectronics assembly.

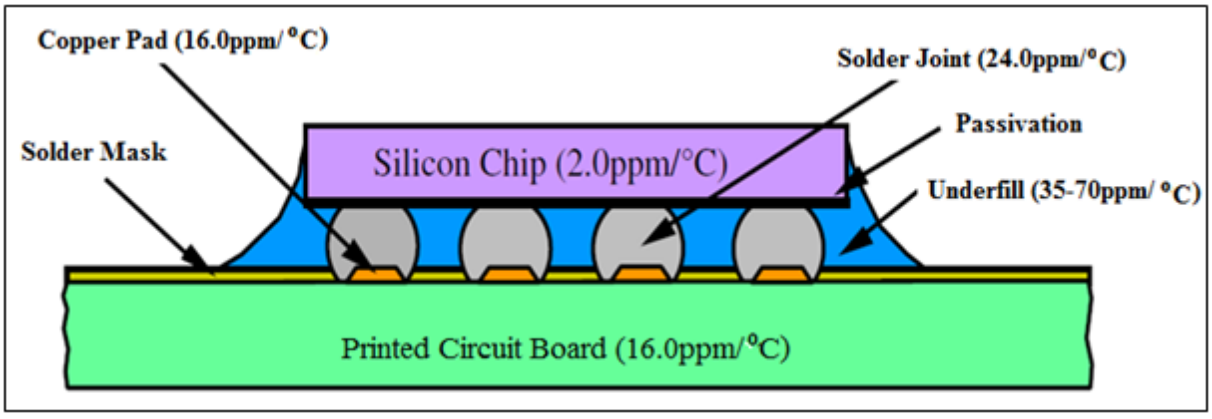


Figure 1.1: Cross section view of area array BGA solder joint

Source: (Hariharan, 2007)

1.2 Packaging of Advanced Microelectronics

Ball Grid Arrays (BGAs) solder bump and CSPs are one of the superior chip-level technologies currently used to package advanced microelectronics. The joints of the BGA contain IMC at interconnects between solder and bond pads. The primary concerns in the structural integrity

of the assemblies at high-temperature excursions include among others the CSH and an accelerated accumulation of damage at the joints.

The determination of an optimal BGA standoff height and the actual magnitude of fracture will provide an in-depth understanding of the board level reliability for an accurate prediction or determination of a device fatigue life. However, Miniaturisation is still a key design trend, and the electronics modules are increasingly finding applications in sectors where operating ambient temperatures are harsh (Amalu, Ekere and Bhatti, 2009; Braun et al., 2006). Nevertheless, design and manufacture engineers have come under pressure to develop a quality product of a reliable solder joint to meet with customer expectation of a device extreme performance at a thermal load and high temperature in the field.

Power modules, which operate at a temperature above traditional electronics working limit of 125oC (specifically above 150oC), are high-temperature electronics (HTEs). Their high mortality rate indicates the assemblies' susceptibility to failures in the field. Consequently, the reliability of BGA solder joints at high temperature and thermomechanical load has become a critical concern (Normann, 2005). The difficulty in the achievement or development of reliable high-temperature devices lies in the complexity encountered in the component architecture, material and physical property characterisation. Real power devices for HTEs packaging require knowledge drawn from many engineering and materials disciplines, which include electronics, heat transfer, mechanics and materials science. The challenge is in the identification of the underlying physical relationships that link the performance of the power electronic systems to the microstructure and structural arrangement of the constituents (Shaw, 2003).

The reliability of electronic devices operating at high-temperature ambient greatly depends on many factors as previously mentioned, which influence the static structural integrity of its components at service conditions. Again, the criticality of the effect of these factors increases also as stated earlier with miniaturisation process (Reichl, Schubert and Topper, 2000) and specifically exponentially with ambient temperature (Amalu, Ekere and Bhatti, 2009). One key component of HTEs, which enables miniaturisation trend, is the BGA. The reliability concern at the board level over CSPs is that finer pitch limits the size of solder balls attached on die and stencil thickness used in an assembly. The finer pitch configuration leads to much smaller joint volume and standoff height while larger die-to-package ratio typically means higher stress level caused by the CTE mismatch (Xie et al., 2010). This situation may not be different for BGAs

and FC-BGAs. The physics of failure has been by induced plastic stress, which in turn produces strain in the joints of the components.

In general, many factors determine the reliability of the joints in a BGA mounted on a PCB using solder alloy or flux. With proper reflow soldering (E. H. Amalu et al., 2011; Lau, et a.l., 2011) and selection of the appropriate high-temperature solder and materials (Amalu, Ekere and Bhatti, 2009), differences in the bonded materials CTEs, can be addressed. However, the thickness and properties of the formed IMC at materials interfaces of a solder joint, the hostile service condition and the solder joint geometry are all contending factors in chip-level device operational efficiency. Stress inducement during temperature variations and cycling account for mismatches in the CTE of the different bonded materials in the assembly. The geometric consideration of the solder joint's architecture is thus the primary driving force of thermomechanical failure, (Hong, Yuan and Junction, 1998; Shaw, 2003; Xie et al., 2010; Liu, Haque and Lu, 2001; Hung et al., 2001).

The brittle nature of IMC is likewise reported to impact HTE chip level reliability (Alam, Chan and Tu, 2004). The fatigue failure mode is usually by crack initiation (Libres and Arroyo, 2010) and propagation (Shaw, 2003; Ghaffarian and Kim, 2000; Yang and Ume, 2008). The fatigue phenomenon is most destructive in the presence of low or high CSH of the solder joints (Ladani and Razmi, 2009). It is thus imperative to state categorically that the assembly architecture and precisely the profile of the bonded material play a crucial role in the overall systems reliability.

1.3 Problem Statement and Challenges

The previous analysis has shown that BGAs are essential components of SMT electronic assemblies and their SJs serve as mechanical support and pathways for the chip's electrical connection to PCBs. The SJs of BGAs degrade over time, and the degree of the damage is more critical for high- temperature applications. However, failure of these SJs will result in the modules and system failures. Thus, there is a need to study the failure of BGA packages and assemblies induced by both thermomechanical and metallurgical changes of their solder joints.

Literature review (Menon, 2010; Yao, Qu and Wu, 1999) conducted revealed that the mechanical integrity of SJs in SMT area array assembly depends on the CSH (fig. 1.2), existing at interconnection boundaries between the component and the substrate printed circuit board. In a further review of reflow process parameters (Hariharan, 2007), two factors (Peak

Temperature and Time above Liquidus) were also found to affect SJs integrity and hence the CSH; and thus their impact is investigated. Other factors reviewed include the mismatch in the CTE of the different bonded materials in the assembly and the formation of brittle IMCs at the solder-substrate and solder component interfaces during reflow soldering process and ageing temperature (Menon, 2010; Schubert et al., 1998). This innovative work is based solely on solder joint quality assessment regarding collective strength, employing shear and pull tests.

A modified approach for assessing the failure of SJs, including failure mechanism and sites of failure is the use of accelerated life testing within a single chamber, between -40^0C and $+125^0$C, -40 and $+150^0$C, and -40 and + 175^0C respectively. The thermal cycling experiments help to simulate the solder joint life cycles by employing the joint's damage acceleration factor and may include MTTF/MTBF. The reliability analysis of an optimised solder joint for use in microelectronic packaging will be using the details of intermetallic layer thickness, the growth rates as well as the changes in microstructures in the lead-free solder joint gathered. To date, there is no standardised CSH for CSPs and area array assemblies (typical of micro BGA). The determination and adoption of optimal CSH for SMT BGA assembly will improve the integrity of assembled components SJs and consequently the fatigue life of electronic devices manufactured using the surface mount BGA.

A Typical SMT BGA is an area array lead-free component type comprising a mixture of Sn, Ag and Cu solder ball/alloy. The alloy composition varies from 3.0 to 4.0 weight % of Ag and 0.5 to 0.7 weight% of Cu contents; while the balance is made up by Sn (Pecht and Anupam, 2007). The assembly process requires two stages. The pre-reflow process step involves solder flux printing/robbing on the PCB followed by BGA placement while the post reflow stage involves the fusion of solder flux and paste from solder ball during metallisation to form a solder joint.

After carrying out the reflow process and joint formation, a reliability test conducted to determine the integrity of the finished joint follows. However, most of the projected results on CSH of SJs are on effects only. They are also model predictions and lacked experimental validation. A cross section of SMT assembly process on solder joint formation, described and presented in Figure 1.2, comprises of the pre and post reflow stage of BGA attachment on board, interconnection boundaries and CSH.

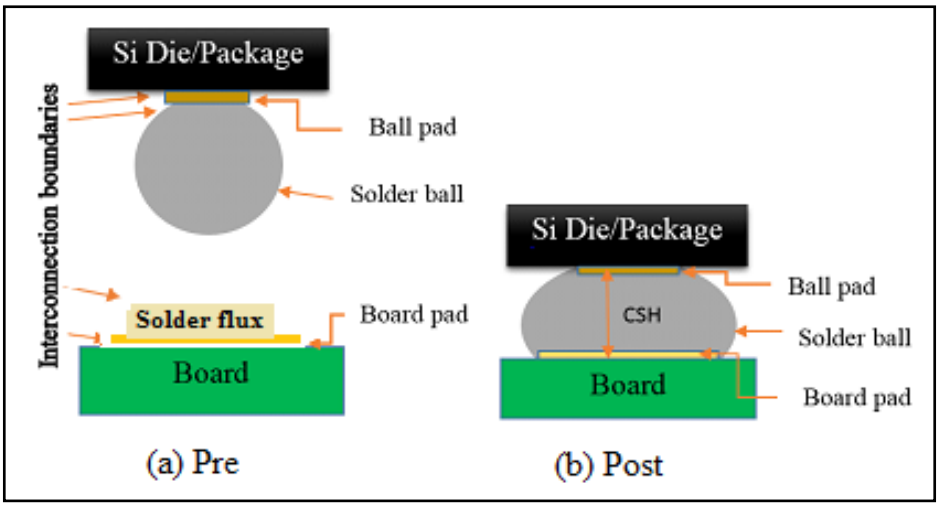


Figure 1.2: Pre & Post reflow stage of BGA solder joint assembly

Source: (Pecht and Anupam, 2007)

Finally, as there is little research on the Sn-Ag-Cu lead-free solder alloys, a study on their solder joint microstructure, alloy composition, formation and growth of IMCs and variation in joint's height would provide a better understanding of their effect on the long-term reliability of solder joints in electronic device packaging. Understanding of the complex relationship between operating environment (temperature, humidity and vibration), and HTE device/assembly solder joint long-term reliability performance serves as the primary focus of this study.

1.4 Motivation for the Study

1.4.1 Thermomechanical Reliability of Microelectronics Devices

Thermomechanical Reliability (TMR) of electronic devices has its root from thermal management of interface materials and is currently a critical issue in the industry. It is triggered by mechanical restraints that may either be external or internal or by a non-uniform distribution of temperature, coupled with mismatch and differences in the CTE of bonded materials, for example from high expansion Copper (Cu) and small expansion Silicon (Si) dies. Its effect from various reports (Menon, 2010; Vettraino, 2004) and by observed failures could be a decline in the lifetime of components and systems, structural design failures in component architecture, process and packaging induced stresses. A typical TMR stress can cause a plastic deformation capable of inflicting a permanent damage as voiding and migration to the

microstructure of a device solder joint, thereby influence its reliability. This phenomenon can be critical at a high temperature of operation. However, in the researcher's opinion, the solder joints adhesive and cohesive strength must be considered as key issues to be addressed in the industry through a careful approach to 'TMR' of microelectronics (Wang et al., 2009).

1.4.2 Miniaturisation in Electronics Products

Miniaturisation in electronics has occurred on a very vast scale and every single moment the functionality, and the size of every single electronic chip increased and decreased. The most apparent reason for this extensive Miniaturisation is to save resources and cost of manufacturing ultimately. Since electronic components are getting smaller and their usage is increasing simultaneously, the need to build stronger and reliable electronic solder joints with appropriate materials also arises. The problem is that the small components have to go through all the mechanical shocks and should be able to withstand the vibration without failing or being fractured. Small chips, attached to PCBs, are mostly prone to breaking off during mechanical shocking since the solder joints between the chip and PCB are feeble and cannot withstand high shear forces. Tests performed with high-temperature solder joints demonstrated high-quality joints with lead-free SnAgCu solder alloy [NPL, 1999]. The low strength of solder joints adversely affects the overall performance of every high speed, and high volume electronic device and countering this problem is by employing numbers of methods. The most promising are selecting the right solder alloy, which would give the solder joint its ductility and tensile properties, make it more sustainable and give it the ability to withstand all sorts of shocks. To achieve product Miniaturisation requires people with skills and research interests for which I have the passion.

1.4.3 The Growing Interest in Multichip Technology

Another key consideration for the study of solder joint reliability of BGA and CSP is the growing interest in the multichip technology used in today's oil well-logging, aerospace, automotive and mobile networks motherboards. Research has shown that the pace at which these technologies fail at service conditions under high-temperature ambient is huge. However, the demand for HTE components in the packaging of advanced microelectronic modules has escalated due to the severity of device's life cycle and operational ambient condition and the complexities in surface mounting. The complexities as earlier discussed may include CTE

mismatches between the component die and the laminate substrate or PCB. Other major concerns are the configuration of ball and pad sizes, molten solder surface tension and wetting behaviour, including packaging and standardisation issues. These concerns may pose coplanarity problems, surface termination and finish of lead or some reliability concerns in either hand-held consumer electronics, automobile, aerospace or oil well logging operations per se. Sometimes the device's operational safety problems may result in catastrophic failures that might involve human life and property in a huge sum. Thus, the high demand for miniaturised electronic products in the market today has called for urgent attention through Research and Development (R&D) to address these issues.

1.4.4 Development in the Research Efforts Devoted in Soldering Science

The assembly processes of BGA architectural enhancement have been through explosive growth in research efforts dedicated to soldering science (Liu, Haque and Lu, 2001). The method allows the use of solder metallisation (molten solder alloys) in innovative and rapid SMT assemblies of HTEs. Thus, product assembly at elevated temperatures is a future concern for the niche markets whose assembled components and product manufacture have much relevance to critical solder joint reliability appraisals at reduced costs. A sound knowledge of the reliability assessment method will be a significant contribution to the microelectronics industry and their partners.

1.4.5 Urgent Need for R&D Engineers

There is a need for R&D engineers and SMT implementation scientists who will use compliant (lead-free) solder alloy in component assembly to address issues relating to SJR. Also, research has shown that to determine the fatigue life, the MTTF and the end of life management of device operation in the field, needs personnel. Other key considerations for R&D requirements may include the management of Waste from Electrical and Electronics Equipment (WEEE) as well as the Restriction of Hazardous Substance (RoHS). The suggestion for its elimination was approved and pledged under the European Union (EU) directive of 2006, revised 2012 (Frear et al., 2008; Amalu et al., 2015; Lin, Yin and Wei, 2011; Kotadia, Howes and Mannan, 2014).

1.4.6 Challenges Faced by Mobile Devices & Other Electronic Components

Mobile devices and other electronic components are facing severe challenges ranging from accidental drop off and transportation problems because of their fragile nature. However, and in tandem with popular journals, media technology and media-rich environments, mobile devices and other electronic components will continually face more challenges in the future. As the devices continue to get smaller, smarter, faster, and highly functional on multiple levels of joints connectivity and mechanical strength, there is bound to be various problems that would occur or be envisaged (Libres and Arroyo, 2010; Ghaffarian and Kim, 2000). Through hands-on designated research engineers and component manufacturers, it can be easy to resolve the challenges in the prolific technology of the future. The speciality of these engineers would lie on the proper and more accurate examination of the device's microstructure for the prediction and or determination of its life cycle time and MTTF. A direct assessment of mobile phones damage by accidental dropping or other environmental conditions is made possible through a consolidated study.

1.4.7 Capabilities in the Design for an Electronic Power Module

Investigations show that the technology of SMT BGA, FCOB and FC is a key to designing ICs and microchips of high thermal resistance for microelectronic packaging. Moreover, a critical examination of the thermomechanical properties of BGA solder joints revealed they are not only time-dependent but also hugely influenced by the package geometry. The information can lead to the design of a power electronic module with a reliable IC technology. It can also buttress an enhanced thermal, mechanical and electrical connectivity at service conditions, especially when operating ambient temperatures are harsh (Yang and Ume, 2008; Ladani and Razmi, 2009; Amalu and N.N. Ekere, 2012).

Furthermore, being part of the design process for the achievement of ICs with BGAs can lead to novelty. Thus, the architecture of BGA components embraced with lead-free solder joints evolves in SMT as a technology of the future, poised with challenges that are resolved only through a critical research. However, the criticality of a systematic study in its combination can deal with the milestones or gaps in the research area to produce optimal solutions for the reliability of BGAs and flip chips-on-board. The measures leading to gaps closure can also raise hope of success for chips component assembly in the industry.

1.5 Aim and Objectives of the Study

The aim/drive for this research work is to evaluate the TMR of lead-free solder joints in SMT assembly with particular emphasis on joints of BGA and Chip Size Resistors (CSRs) subjected to different thermal loading conditions. The study has the following objectives:

- To investigate the effect of reflow profile parameter setting on the shear strength of SJs TMR in chip resistor SMT assembly.
- To study the effect of strain rate on the shear strength of aged and non-aged surface mounted SJs in electronic manufacturing.
- To determine the effects of Component Stand-Off Height (CSH) on the shear strength of BGA SJs at (a) Varying pad sizes and (b) Varying reflow peak-temperatures.
- To establish the effect of solder type, reflow profile and PCB surface finish on the formation of voids in SJs.
- To investigate the effect of temperature and extended/long operations on SJs shear strength under Accelerated Thermal Cycling (ATC) condition.

1.6 Research Plan and Programme of Work

Figure 1.3 presents the programme of work for the PhD study carried out in this thesis. The study started with an extensive review of relevant and related literature assembled from previously published works. The literature review focused on finding the gaps in knowledge in the reliability study of solder joints of BGAs and CSPs assembled on a printed circuit board with Sn or Cu surface finish. SnAgCu lead-free solder paste is the candidate alloy used to carry out the study. Some of the assembled test vehicles subjected under accelerated thermal and isothermal cycling ageing will enhance and induce joints stabilisation, thermal fatigue and growth of IMC in the solder joint. There are five gaps in knowledge identified after a substantial search of the literature. There are discrepancies found between predicted and experimentally determined solder joints on the effects of reflow profile parameter settings, strain rate deformation, low or high CSH, voids formation in solder joints, temperature and extended operation on solder joints shear strength. Until date, there is still no known CSH for solder joints reliability in the field. However, most of the opinion held by various researchers on the factor effect determination for a reliable solder joint are different, and some are inconclusive; and this research will clear some of these doubts. The identified gaps, therefore, formed an integral part of the studies carried out in this work and reported in some areas in this thesis.

Chapters 3 to 4 incorporate laboratory experiments designed to investigate each of these concerns. The key results obtained for an improved solder joint reliability are in the chapter conclusion of this novel work. The key results are also found itemised in the programme of work presented in Figure 1.3.

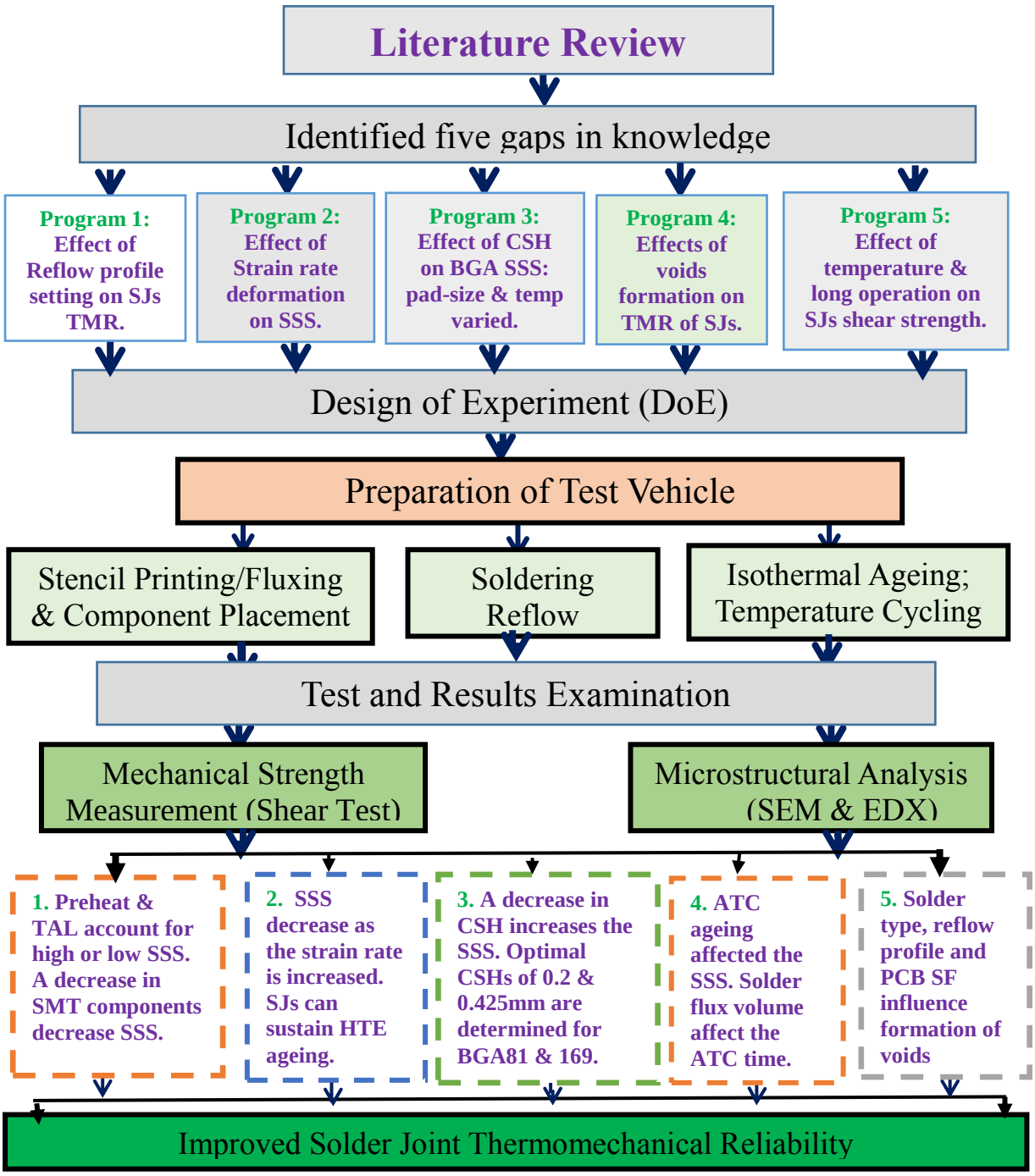


Figure 1.3: Programme of Work for the research study

1.7 Overview of the Thesis

This thesis presents in chapter one an introduction to the thermomechanical reliability of lead-free solder joints in surface mount electronic component assembly. It proceeds in chapter two to give a comprehensive review of relevant and associated kinds of literature in the areas of solder joint integrity and thermomechanical reliability. Chapter 3 presents and discusses general methods, equipment and materials used to prepare the experiment test vehicles. Experiment chapters are chapters 4 to 8. Chapter 4 presents the study on reflow soldering process widely reported to account for over 50% of common defects in solder joints' of surface mount component assemblies. Chapter 5 reports on the effect of strain rate on the thermomechanical reliability of surface mounted chip resistor solder joints on Cu substrate used in electronic manufacturing; (the imposed strain-rates that cause deformation during the heating stage of the cycle are affected by elevated temperature operations on the integrity of the solder joint). The high-temperature operation is simulated in each experiment using the concept of temperature soaking and thermal cycle Ageing. In chapter 6, there is a detailed report on a study on the effect of component standoff height (a factor affecting the structural integrity of solder joint); while chapter seven reports on the effect of solder type and PCB surface finish on the formation of voids in solder joints. Chapter eight reports on the impact of accelerated thermal cycling ageing on the long-term reliability of BGA solder joints. Chapter nine presents the conclusion of the research work reported in this thesis.

Chapter 2: Literature Review on SMT Assembly and Thermomechanical Reliability and Challenges in Solder Joints Technology

2.1 Introduction

This chapter provides a review of previous research studies in manufacturing process and thermomechanical reliability of solder joints of electronic components in Surface Mount Technology (SMT). Areas covered include component assembly and applications, manufacturing processes with emphasis on solder printing processes and reflow soldering. A critical review of the thermomechanical reliability of solder joints was also made, namely on three broad subheadings: 2.4.1, 2.4.2 and 2.4.3 for resistors, ball grid arrays and other new trends in electronic components of high volume technology. The effects of thermomechanical load and solder joint failure mechanism and damage formed part of the discussions and summary given in this chapter.

2.2 Surface Mount Electronic Components, Assembly and Applications

2.2.1 Surface Mount Electronic Components

Surface Mount Electronic Components (SMECs) used in SMT can produce reliable assemblies at reduced weight, volume and cost. The components could be passive or active and have no functional difference but can be more reliable when compared with their conventional through-hole-counterparts. Passive components are Surface Mount Devices (SMDs) such as resistors, capacitors and inductors and they are the most common types of leadless chips surface mounted components. Others are small outline compliant leaded SMDs like transistors and integrated circuits, leadless and leaded fine-chip carriers, for example, quad flat chips and flip chip ball grid arrays (FC-BGAs), popularly characterised as active components (Yılmaz, 2008; Prasad, 1997). The SMECs are practically in use when mounted on the surface of PCBs or substrate to form electrical interconnections on its base metal. In SMT, a Surface Mount Component (SMC) or SMD is relatively small, with either smaller or no lead at all. It is usually smaller than its through-hole-counterpart and for this reason provides greater packaging density. SMECs may have short pins or leads of various styles, flat packs or contacts, a matrix of solder balls for example, in BGAs or terminations on the body of the components. Today there are various amounts of SMECs with varying lead counts and pitches. In SMT, one can define pitch as the distance between lead centres. There are some SMT benefits associated with SMECs and of more significance and cost effective is the real estate savings, achievable through component size reduction (Prasad, 1997).

However, the general trend in today's microelectronic packaging has been towards product miniaturisation leading to smaller parts, pitches, and contact area, followed by higher I/O pin count. Subsequently, BGAs and chip-size resistors, as well as Chip Scale Packages (CSPs), play major roles in the industry because of their categorisation possibility and recognisable pitch size. As a result, interconnection density has become paramount in the manufacturing sector. Moreover, with the shift in the lead-free soldering, components of SMD had the challenges to meet new requirements, which include materials e.g. type of flux applied or nature of stencil printing, temperature, the size of materials and reflow methods used.

Further Miniaturisation of SMECs and the new trends in component assembly for example, in the packaging of area array components (CSP, µBGA, FC-BGA), thick film technology, and in the technology of package-on-package. It has led to a continuous demand for smaller sizes, as well as widespread use of fine pitch (20 and 25mil pitch) and ultra-fine pitch (a pitch of 0.5mm or less) in the industry. Also, CSP, package size not more than 1.2 times die size and Direct-Chip-Attach (DCA) components according to Ray Prasad (1997) are becoming more popular in the achievement of further densifications. The packaging and assembly of SMECs affected not only the real estate management or board level reduction but also the electrical performance of the device structural integrity. However, due to basic packaging differences in component assembly especially, those found in the CTE mismatch, the parasitic losses such as capacitance and inductance in surface mounted devices are considerably lesser to those obtained from the Through-Hole Technology (THT).

Among other significant functional benefits of SMECs, include protection of devices from the environment, provision of the communication link, heat dissipation possibility, opportunities offered for component handling and testing. In general, SMECs assembly prototypes are much more complex than its conventional counterpart is. Figure 2.1 shows different types of surface mount electronic components, the majority of which are from 2014 topline dummy ICs.

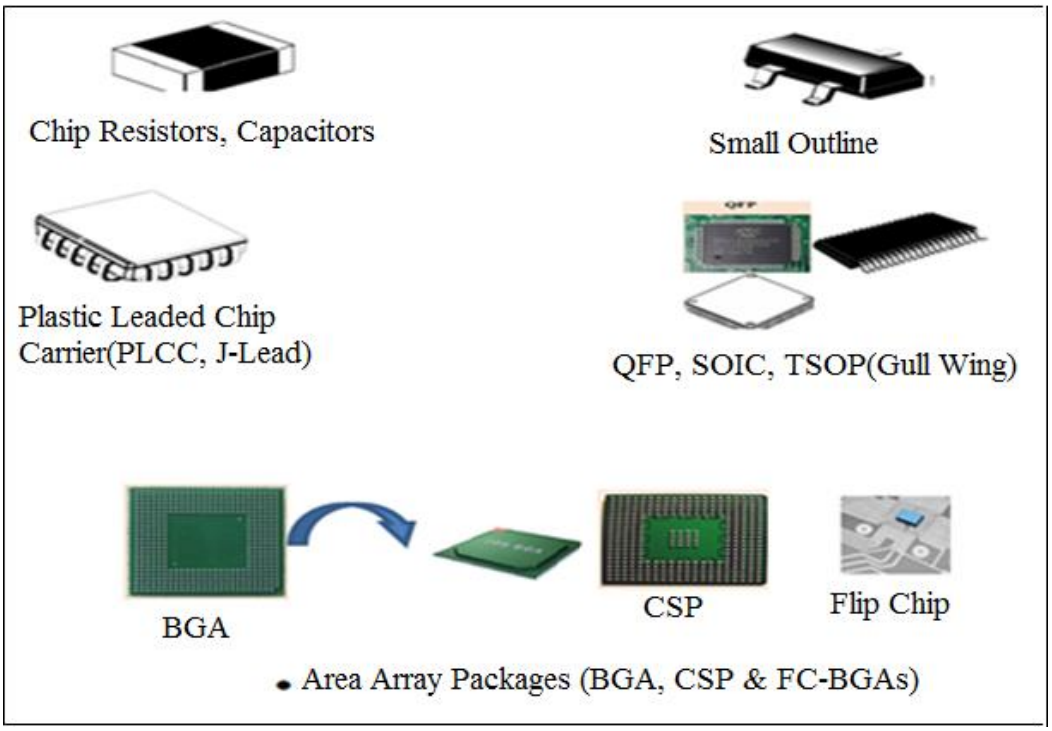


Figure 2.1: Common SMT components

Source: [online] 2014 Topline dummy Components, (Yılmaz, 2008))

2.2.2 Surface Mount Assembly Technology (SMAT)

SMAT is the description of the technology that incorporates the electrical and mechanical characteristics of electronics component to the PCB or a similar type of circuit or substrate (Lau et al., 1990; Trybula and Trybula, 2005). Some of the important variables considered in SMAT include the melting temperature of solder alloy, flux chemistry, wetting characteristics, the surface tension of the solder alloy composition and the reliability of its solder joints. The sequence of operation of an assembly of a surface mount process begins with the deposition of solder paste or flux on the pads or component terminations on the PCB surface. Next is the placement of the electronic components onto the PCB manually or through the aid of a pick - and- place machine to form a test vehicle (PCB with the components placed on them). The experimental test board was then reflowed in a reflow soldering oven to form surface mount solder joints. The assembly methods of SMT components are in three folds, Type 1, Type 2 and Type 3, and these are as described in sections 2.2.3.1, 2.2.3.2 and 2.2.3.3 respectively. The difference between has The SMT, and THT is described and schematically presented in Figure 2.2. The technology had gone through series of developments since the 1970s when the electronics industry discovered the need to enhance the robustness of its IC packages by

increasing the density of SMDs and by reducing their real estate constraints under cost reduction. According to Lee Ning-Cheng (2002), THT, which was in vogue in the 70s was unable to meet the growing requirements in commercial and industrial applications due to increased cost of drilling more holes, and the difficulty encountered in drilling smaller holes for smaller pitch dimensions gave way for SMT as an alternative technology.

SMT came into prominence because it presented the solution to the growing requirements for solder joint interconnections. There is also commercial availability for many SMD, which enables the interconnection bonding of surface mounted chip-on-boards (COBs), µBGAs, CSPs and FCs to become the primary acceptable assembly technologies especially, in hand-held consumer electronics such as mobile phones, computers, camcorders, cameras, televisions, to mention but a few. Lee, Ning-Cheng (2002) and Lau, J.H. et al. (1991) reported that SMT offers numerous advantages over THT from many viewpoints, which include cost, design, manufacturing, and quality. Moreover, that SMT, as opposed to THT, allows a higher degree of automation, higher circuitry density, smaller volume, lower cost, and better performance. They further concluded that the reliability of solder joints like any new technology is one of the most critical issues associated with SMT development; since the solder joint is the only mechanical means of attaching the component to the PCB. Figure 2.2 shows the schematic diagram to highlight the difference between SMT and THT.

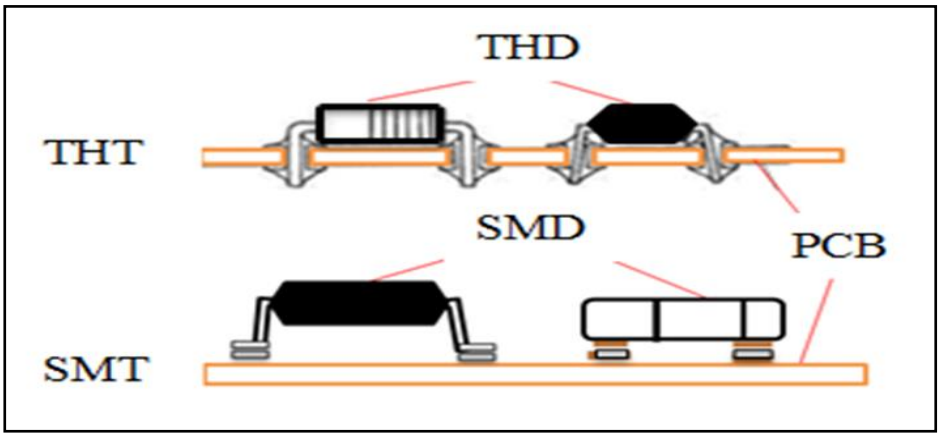


Figure 2.2: Difference between SMT and THT

Source: (Ning-Cheng, 2002)

However, the versatility of the SMT assembly process enables the mounting of a variety of SMT packages (otherwise called SMDs) on the same printed circuit board. A further advantage

is derivable from real estate reduction and component size mentioned earlier. SMT components are typically much smaller than the THT devices and attachable on both sides of the board. Among other benefits of surface mount technology is the fact that the repairs of surface mount assemblies are also easier and sustains less damage than the THT assemblies (Glenn et al., 2006; Lee, 2004). Many categories of electronic packages used in surface mount assembly include leadless devices and leaded chip carriers as stated in section 2.2.1**,** and they are prone to damage during reflow soldering.

Nevertheless, repair and rework are much easier in SMT than it is in THT assembly, which has problems with clenched leads. However, SMT repair is simpler because of rework or repair needs but cleaning and replacement of the components. In complex situations during rework, redress or repair, old components can be removed, depending on the type of heating system used; specialised tweezers have been invented to ease out the task of rework and repair (Glenn et al., 2006). SMT is not only versatile but is valuable and used in different ways, and varying situations under justifiable cost effectiveness, product sizing, design quality, high performance and repair advantage, and for these reasons have become one of the strongest trends in electronic packaging (Lau, Rice and Avery, 1987).

2.2.3 Types of Surface Mount Assembly Technology

In the assembly of electronics and electrical interconnects, components of different sizes are mounted on printed circuit boards to complete the circuitry of the device. The present trend in increased functionality of electronic components with smaller, smarter, lighter in weight and enabling circuit size, capable of operating on a larger scale in the interconnect, demands the need to mount more components on the PCB of fixed area. In electronic packaging, SMT plays considerably an important role in coping with the problem of component sizing and strength of the solder joints. However, and with SMT, it has been possible to design components of different sizes and specifications which can be made to fit in a given space in the circuitry of a device (Lau, 1991). Lee Ning-Cheng (2001) and Ray Prasad (1997) categorised Surface Mount Assembly Technology into three types:

2.2.3.1 Type I: Technology of SMCs on Both Sides of the Board

Type I is the assembly method of mounting components on both sides of the board as shown in Figure 2.3. The components indicated in the schematics are Small Outline transistors, Plastic Leaded Chip Carrier, Chip Capacitor, Dual-Inline-Packages, and Leaded Ceramic Chip Carrier (LCCC). Solder paste is applied on both sides of the board and used for achieving the bonding process of SMCs using reflow soldering method for fine pitch components. For thick components, on the other hand, and to avoid over-melting of the pre-assembled solder joints, wave soldering becomes the better alternative during the second reflow of the board underside. However, wave soldering, in general, requires adhesives to secure the components in place.

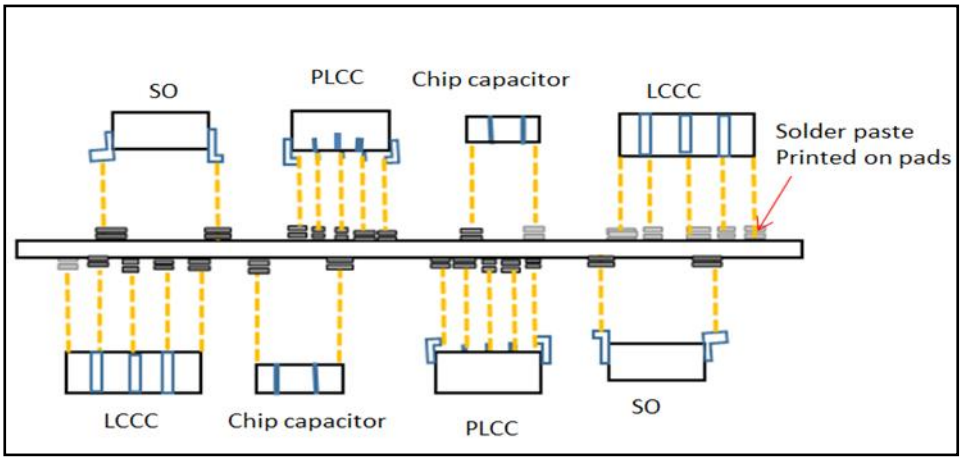


Figure 2.3: Type I - SMT device on both sides of PCB

Source: (Yılmaz, 2008; Trybula and Trybula, 2005)

2.2.3.2 Type II: Mixed technology of SMC & THT component (THC)

Type II is a mixed technology consisting of a combination of SMC and THC on the one hand and chip components on the other side of the board as shown in Figure 2.4. The Type II assembly process has the flexibility of using reflow soldering to attach SMC and wave soldering for Chip and THC. This reflow process may save a huge barrier in the assembly supply chain and can cater for SMCs limitations but might lead to construction complexities that are not cost effective, as more floor space may be required.

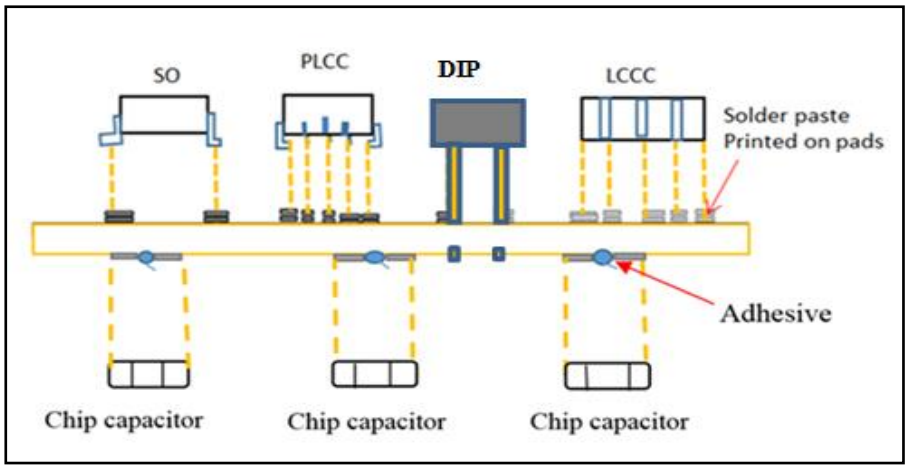


Figure 2.4: Type II SMT devices

Source: (Yılmaz, 2008; Trybula and Trybula, 2005)

2.2.3.3 Type III: THC on One Side and Chip Component on Reverse Side of PCB

Type III assembly shown in Figure 2.5 consists of THC on one hand and chip components on the reverse part of the board. The assemblage process is by wave soldering only and represents the initial stage of converting from conventional THT to SMT (Ning-Cheng, 2002). However, the given classification is not exhaustive (SMC: EIA, IPC and SMTA, 1999). Figure 2.6 shows a typical assembly device of SMT component on PCB from Chinapcba.com.

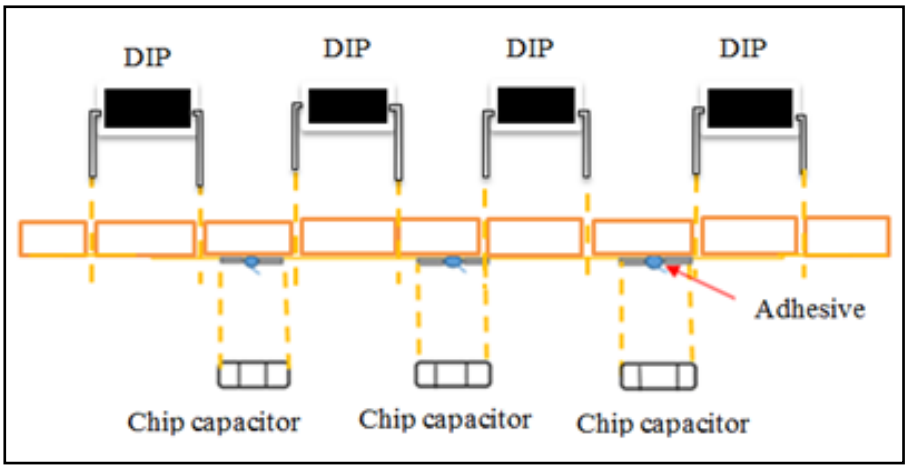


Figure 2.5: Type III - SMT device for Chip & THC

Source: (Yılmaz, 2008; Trybula and Trybula, 2005)

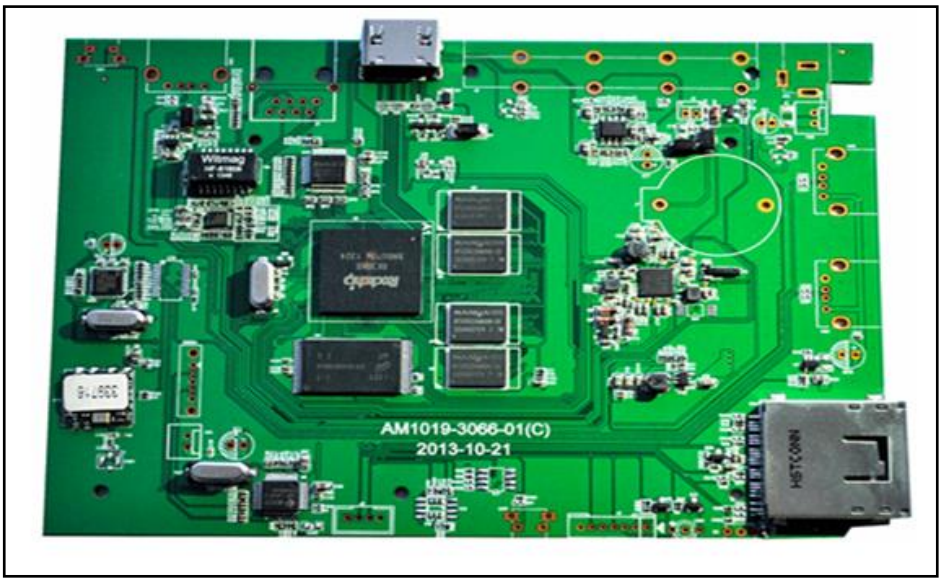


Figure 2.6: SMT assembly on PCB [454 x 341-Chinapcba.com]

Source: (Bysco Technology (Shenzhen) Co. LTD, 2015)

2.2.4. Manufacturing Processes and Application of SMAT

In electronic manufacturing processes of SMT, there are three critical parameters under consideration, which include:

2.2.4.1 Solder Printing Process

Stencil printing of solder alloy is a process by which a viscous material is deposited through a stencil aperture openings onto a substrate/PCB (Hanrahan, Monaghan and Babikian, 1992; Aravamudhan et al., 2002). The configuration of the stencil apertures determines the basic layout of the deposits. For the printing process to function and for efficient paste transmission, the stencil alignment to the substrate must be in close or direct contact with the surface of the substrate. An angled blade called a squeegee drives the material across the surface of the stencil at a controlled speed and force as shown in Figure 2.7 demonstrating the printing process for SMDs and flip chip packaging.

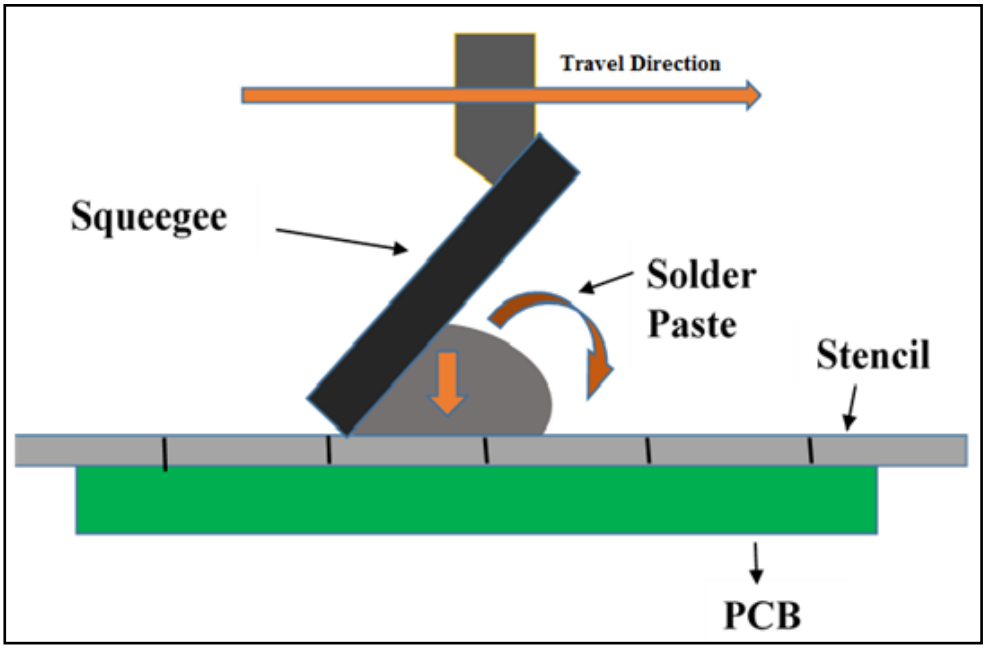


Figure 2.7: The solder paste deposition and the stencil printing process

Source: (Aravamudhan et al., 2002; Mallik et al., 2008, and Schmidt et al., 2008)

Stencil Printing has been the dominant method of solder deposition in surface mount assembly. With the development of advanced packaging technologies such as BGA and flip chip on board, stencil printing of solder bump will continue to play a significant role. The requirements of smaller size, lighter weight and higher performance for printing circuit boards led to the trend of electronic packaging and interconnection away from through-hole technology and towards surface mount technology (Hanrahan, Monaghan and Babikian, 1992).

The stencil printing process comes into three stages. The first is the paste travel stage, the second stage is the aperture filling process, and the third is the paste release stage. In stage I, the squeegee forces the paste roll in front of the squeegee and generates a high pressure. In stage II, the high pressure injects the paste into the stencil aperture. In stage III, the stencil releases leaving a pasted patch on the pad of the printed circuit board. Figure 2.8 represents a schematic of the stencil printing steps.

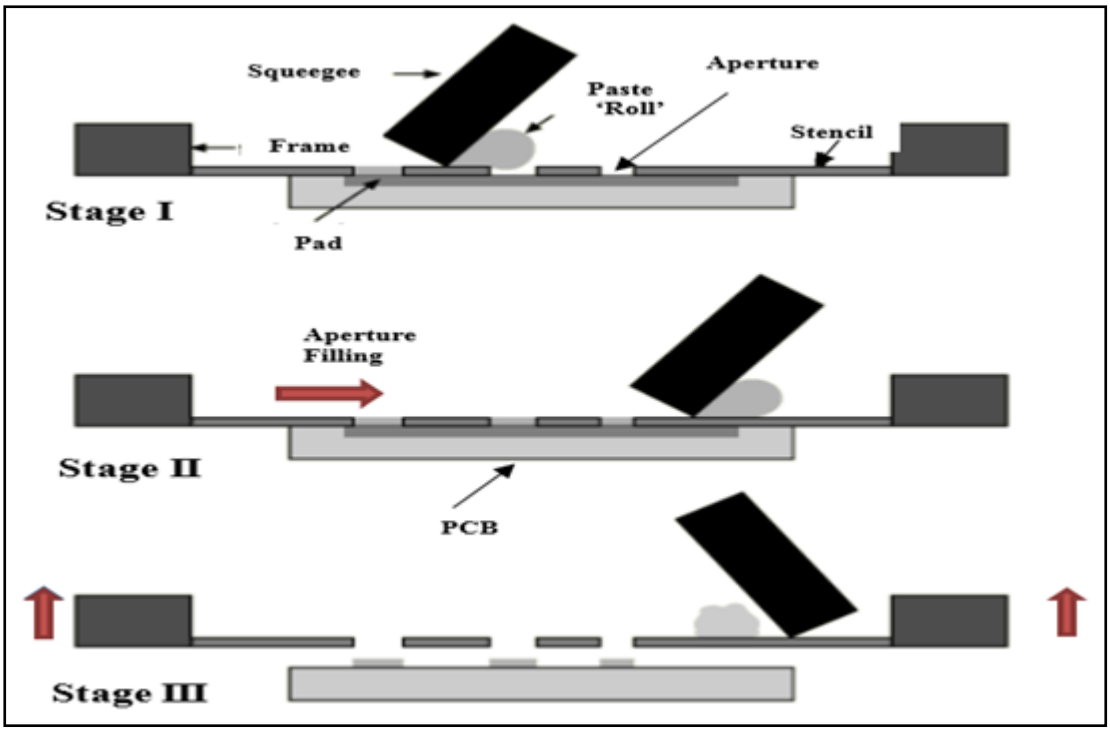


Figure 2.8: Stages of the stencil printing process

Source: ***(Pan et al., 2004; Durairaj et al., 2008)***

Notably, the pressure in the paste during and after aperture filling (Figure 2.9) helps to determine whether the adhesive will adhere onto the PCB, stencil or squeegee after completion of the hole emptying process after which the board mechanically were separated from the stencil (Figure 2.7, Figure 2.8 and Figure 2.9). However, the process of aperture filling mechanism (Figure 2.9) does not require excessive pressure, and if applied, for instance, bleeding of the paste underneath the stencil may cause bridging and will require frequent underside sponging and subsequently wiping. To prevent underside bleeding, it is important that the opening of the pad provide a means of gasketing effect during printing. In their report, however, (Mallik et al., 2008 and Amalu et al., 2011) suggested that achieving a good paste transfer will require the adhesive force between the substrate and paste to be greater than the frictional forces caused by the roughness of the walls. In contrary according to them is that the paste might fracture, leading to incomplete paste transfer (Mallik et al., 2009; Amalu, Ekere and Mallik, 2011).

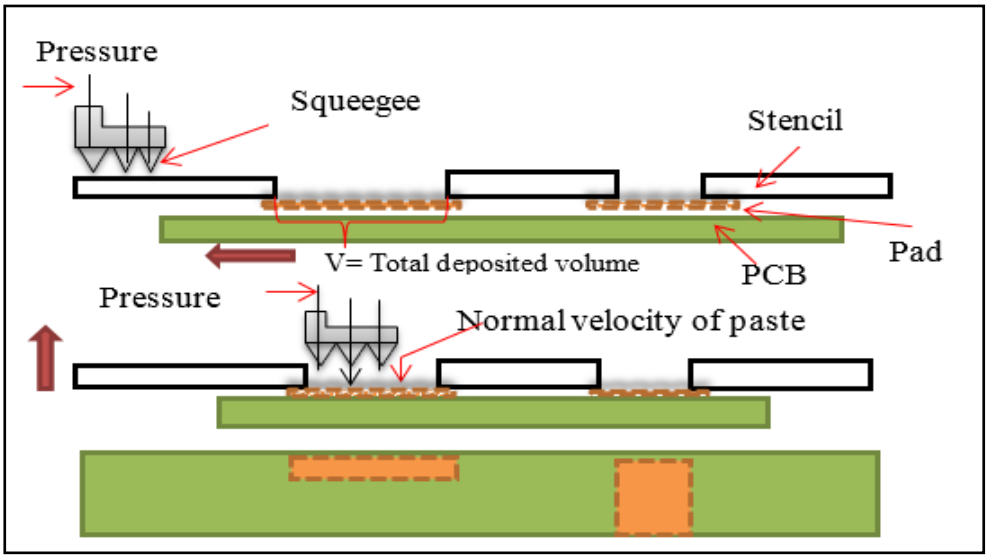


Figure 2.9: Aperture filling mechanism

Source: (Pan et al., 2004; Pan and Tonkay, 1999)

From the preceding, therefore, it is of common sense to deduce that there is no 100% efficiency in the printing process; hence, solder paste printing process as widely recognised is the primary source of soldering defects in SMAT. Previous studies show that more than 60% of the assembly errors can be traced to solder paste and the printing process (Mallik, Schmidt et al., 2008; Jensen and Ronald C Lasky, 2006). However, up to 87% of reflow soldering defects are caused by printing problems (Marks et al., 2007), which invariably affect the reliability of solder joints. Many variables affect the stencil printing process too. The components of the stencil printing process include the printer, the substrate, the stencil, the squeegee, the solder paste, and the process parameters. Since there are many existing independent variables, an analysis is necessary to determine the critical input variables that affect the output variables. The control of the correct volume of paste (invariably the standoff height and the diameter) on the board is essential to avoid solder bridges (too much solder paste), and open solder joints (insufficient solder paste) (Mannan et al., 1995; Barajas et al., 2008). Solder paste thickness is also necessary to attain low defect levels as shown in Figure 2.10.

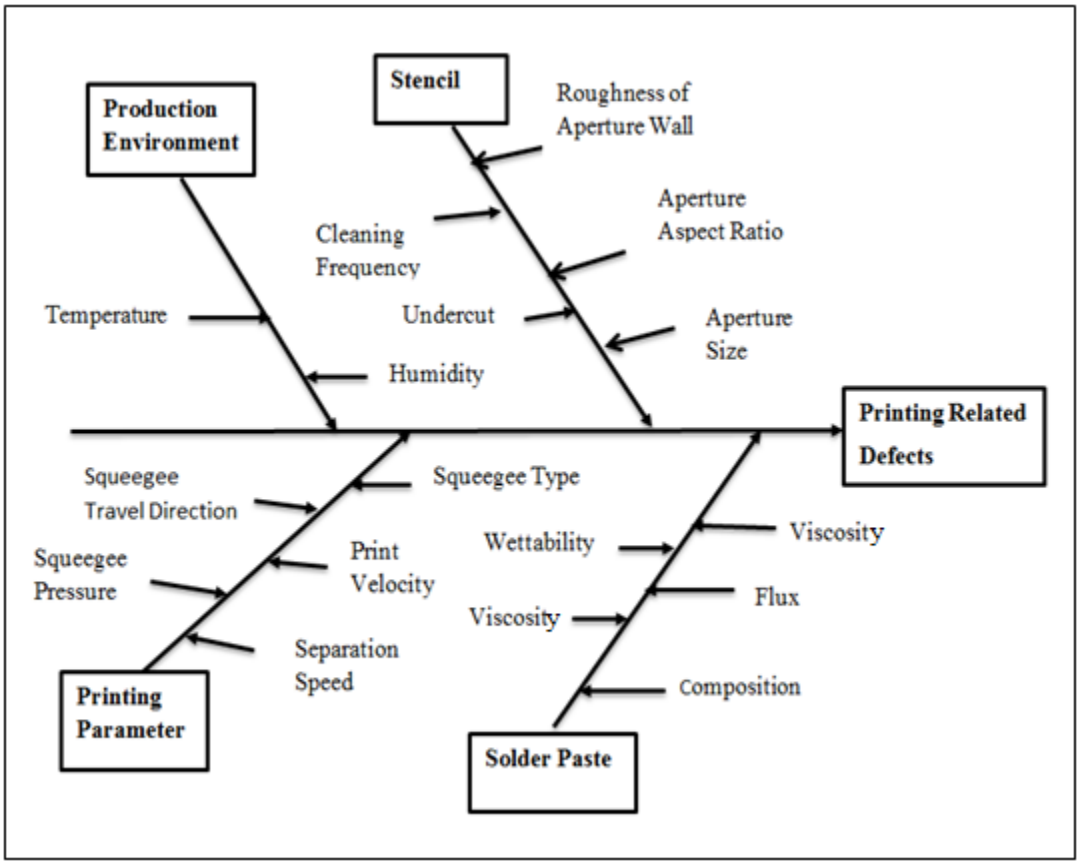


Figure 2.10: Cause and Effects diagram for printing related defects
Source: ***(Barajas et al., 2008)***

2.3 Reflow Soldering of Surface Mount Components

Reflow soldering is an innovative soldering technique developed to eliminate the challenges encountered in the wave soldering of SMCs initially used in the through-THT era. The rheology of the solder paste formed by pre-blending the solder powder and flux is usually formulated to be thixotropic to help facilitate the deposition process during stencil printing (Mallik et al., 2009). The sticky solder paste deposited on the PCB during stencil dispensing serves as a temporary adhesive to hold the SMCs in place before reflow process (Mallik, Schmidt et al., 2008). The populated board heats above the liquidus temperature of the solder paste when placed inside a convective reflow oven to reflow the solder alloy. At the liquidus temperature, the flux reacts and removes the oxides of both solder powder and metallisation which ultimately allows the solder to form solder joints (Amalu, Ekere and Mallik, 2011). However, reflow soldering is a high-temperature process that melts the solder paste so that it can form the final solder connection between the SMD and the board. The process is the most common

method of attaching surface mount components to a circuit board. In the solder reflow process, an optimised temperature profile restricts the printed circuit board from undergoing unrealistically high thermal stresses during reflow soldering. An example of equipment used to carry out the reflow soldering of SMCs is the convection reflow oven described in chapter three figure 3.7.8 of this thesis.

2.3.1 Reflow Profile for Lead-free Solders

The prohibition of lead-based solders in electronic products in 2006 led to the evolving transition into lead-free Sn/Ag/Cu (SAC) solder alloy, with a melting point of about 220^0C. To accommodate such constraints arising from the new solder, the peak temperature of lead-free assemblies' acceptability maintenance is between 230^0C and 245^0C, only a variation of 15^0C. In electronic assembly, the formation and bonding mechanism of solder joints need different pastes, and these require different reflow profiles for optimum performance. Hence, the solder reflow profile is becoming increasingly important because of their inherent characteristics in being product specific and flux dependent in joints formation. For the duration of the reflow profile development, the temperature of the top sideboard (fully loaded board) is monitored employing thermocouples. In the state-of-the-art SMT packaging, use of thermocouples is in the industry for accurate temperature (up to 100%) monitoring at critical points of the printed circuit board during the soldering process. Generic reflow ovens use inbuilt thermocouples and software packages which record the thermal profile data. The use of such profiles (thermocouple) has been important in surface mount assemblies to attain good yield without exceeding the temperature limits of different types of components (Prasad, 1997; Barajas et al., 2008).

Figure 2.11 (a, b and c) presents standard double and single tip thermocouples (T/C) and their attachment method. The thermocouples are low-cost general-purpose types (J, K, T and E) with a sensitivity of approximately 41 μV/°C. They can sustain a temperature range of −200 °C to +1350 °C (−330 °F to +2460 °F) (Vinoth Kumar and Pradeep Kumar, 2015).

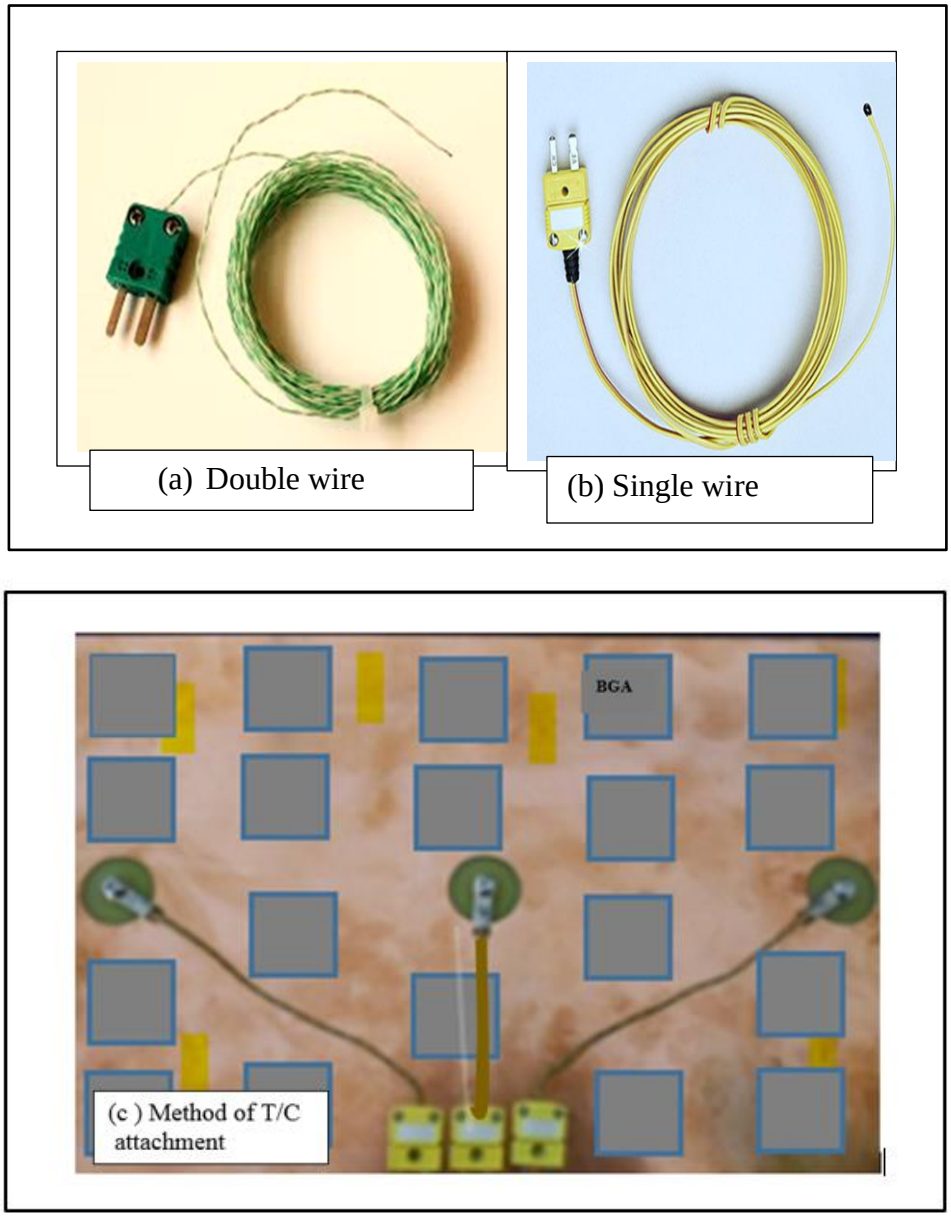


Figure 2.11*:* Typical epoxy coated double and single tip thermocouples
Source: ((Vinoth Kumar and Pradeep Kumar, 2015).

There are, however, four regions in a reflow profile where heat intensity are measured using thermocouples. They are discussed among other things as follows:

2.3.1.1 Preheat Zone

The 'Preheat Zone' is the section where the solvent in the paste begins to evaporate, thereby measuring the temperature changes on the PCB. It is the relationship between temperature and time, which establishes the ramp rate at the zone. A slow ramp-up rate is desired to help

minimise hot slump, bridging, tombstoning, skewing, wicking, opens, solder beading, solder balling, and component cracking (Lee, 2006). Solder paste may have a splattering effect due to overheating. Because this is the longest phase, it preconditions the PCB assembly before the actual reflow, removes flux volatile and reduces thermal shock (Wen, Krishnan and Chan, 2008; Prasad, 1997). In the preheat zone, the temperature is 30^0C-175^0C with 2-3^0C/sec ramp rate also to help circumvent thermal shock found in most delicate components as in ceramic chip resistors. A fast ramp rate rises the potential for solder balling (a defect caused by poor process conditions involving out-gassing from the flux during wave contact or excessive heat disorder as the solder flows back into the bath). It is better and safe to use 5^0C/sec ramp rate (Prasad, 1997).

2.3.1.2 Soak Zone

The 'Soak Zone 'helps to bring the entire test board up to a constant temperature. The ramp rate in this region is slower, almost flat when raising the temperature from 750C-2200C. The consequences of the temperature being too high in the soak region could be solder balling, spitting and splattering due to excessive oxidation of paste material. The soak zone (Figure 2.11) also acts as the flux activation region to enhance the metallisation of the base metal and for the adhesive strength of the solder alloy. The main purpose of the long soaking area is to minimise voids, especially in ball grid arrays (Ladani and Razmi, 2009; Previti, Holtzer and Hunsinger, 2011; Mallik, Njoku and Takyi, 2015; Barajas et al., 2008).

2.3.1.3 Reflow Zone

Printed Circuit Boards may char or burn in the reflow zone in the course of a high-temperature gradient. In contrast to high temperatures, especially when it is extremely low, it might result in cold and grainy solder joints. However, the peak temperature in this zone should be sufficient for an adequate flux enhancement and excellent wetting characteristics. The peak temperature should not be raised so high as to cause component or board damage, discoloration or charring of the board or the base metal. The solder reflow peak temperatures recommended in this zone are 2300C-2450C for lead-free soldering and 30-60 seconds for Time-Above-Liquidus (TAL) temperature. However, research shows that prolonged duration of the chamber temperature above the solder melting point or TAL will damage temperature-sensitive components and

might result in excessive intermetallic growth, which makes the welded solder joint brittle and reduces its fatigue resistance (Pang et al., 2001; Kotadia et al., 2012).

2.3.1.4 Cooling and solidifying Zones

The cooling speed of the solder joint after reflow soldering plays an essential role in the structural and mechanical reliability of the bonded joint. The quicker the cooling rate, the smaller the solder grain size, and the higher the fatigue resistance would be. The speed of cooling rate should be as fast as possible and controlled only by ensuring that the cooling fans are operational. Malfunctioning of the cooling fans will slow down the cooling rate, increasing grain size and resulting into weaker solder joints (Barajas et al., 2008). Most lead-free alloys require higher reflow temperatures than the 210-220^{0}C peak temperature of tin/lead. Reflow temperatures from 235-260^{0}C are common. As a result of these higher temperatures requirement, voiding tends to be more prevalent with lead-free alloys (Lee, 2006; Tsai, 2012). To reduce voiding in SJs, some standards and specifications as described in Section 2.2.3.6, is used. The description of the Ramp-To-Spike and Ramp-Soak-Spike methods of reflow are in Figure 2.12.

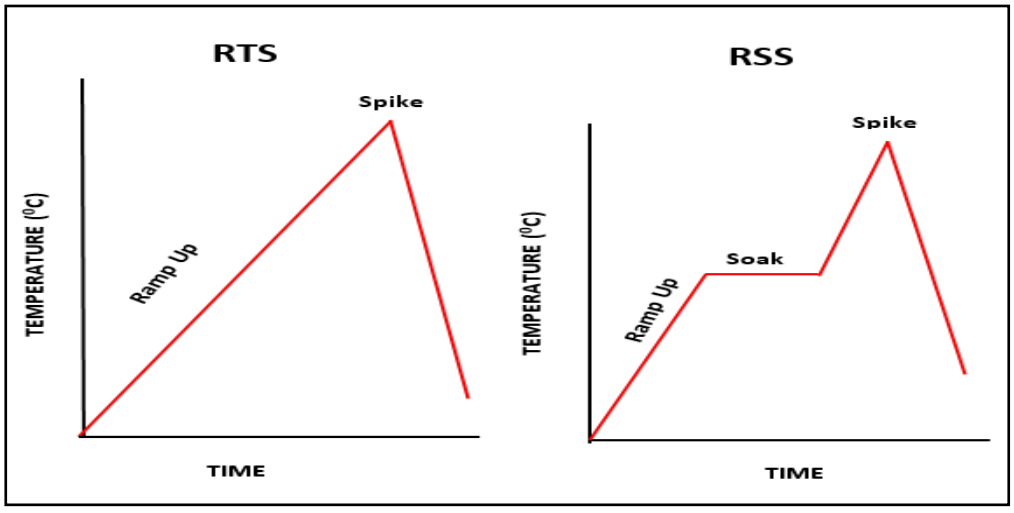


Figure 2.12: Ramp-To-Spike (RTS) and Ramp-Soak-Spike (RSS) Reflow profiles

Source: ***(Barela et al., 1995; Swaim, 2011)***

2.3.2 Reflow Soldering Standards and Specifications

There are because of the smaller solder volume (Hung et al., 2000; Primavera, 2000), internationally recognised organisations and companies, which have classified solder reflow profiles by specifying limits or intervals for all zones depicted in thermal profiles. Major bodies that set these standards to follow include,

- JEDEC - Joint Electronic Device Engineering Council, Arlington, Virginia 1958
- IPC - Institute for Printed Circuits founded 1957 in the USA; later changed in 1993 to Institute for Interconnecting and Packaging Electronic Circuits (IIPECs).
- ECA - Electronics Components (assemblies, equip. & supplies) Assoc., USA 1924.
- SMTA - Surface Mount Technology Association founded 1984 in California, USA.
- iNEMI - International Electronics Manufacturing Initiative, USA 1994.
- ACTEL and ALTERA Corporations, established in 1985 & 1983 in the USA.

JEDEC, a global standard for microelectronics industry in collaboration with IPC, iNEMI and ECA ensure that all products meet specified standards to avoid equipment failure. These measures have brought about an improvement in the reliability of electronics components. However, results from the most literature read have suggested a peak temperature of 230°C for the Sn-Ag-Cu lead-free solder joints. A further 40s suggestion for TAL was made for the RSS reflow profile and 50-70s for the RTS reflow respectively (Salam et al., 2004). A Pb-free reflow profile recommendation by IPC/JEDEC J-STD-020D.1 shown in Table 2.1 and consideration for package thickness in Table 2.2.

Table 2.1: Reflow profile recommendation for SnAgCu solder paste

Source: (Zardini and Deletage, 2011; Xie, Fan and Shi, 2010)

Reflow Parameters	**Lead-Free Assembly**
Minimum preheat temperature (Ts min)	150^0C
Maximum preheat temperature (Ts max)	200^0C
Preheat time	60-180 sec
Ts max to T_L ramp-up rate	3^0C /second maximum
Time above temperature T_L	217^0C, 60-150 sec
Peak Temperature (Tp)	Go to table 2.2
Time 25^0C to Tp	6-minutes maximum
Time within 5^0 of peak T_P	30 sec
Ramp-down rate	6^0C/sec maximum

Table 2.2: Pb-free process - peak reflow temperatures (Tp*)*

Source: (Zardini and Deletage, 2011)

Package Thickness	**Vol. < 350mm^3**	**Vol.350-2000mm^3**	**Vol.> 2000mm^3**
< 1.6mm	260^{0}C	260^{0}C	260^{0}C
1.6 – 2.55mm	260^{0}C	250^{0}C	245^{0}C
> 2.55mm	250^{0}C	245^{0}C	245^{0}C

2.3.3 Optimisation of Reflow Profile Parameters

Optimisation is a means to minimise the defects in reflow soldering. It might not necessarily be the best choice (Ning-Cheng, 2002). Research operations use optimisation techniques to ascertain the main effects and interaction of several factors in a process. They help in the study of many factors simultaneously to determine optimal conditions of input parameters, which will maximise output. Different approaches used in reflow profile optimisation include Taguchi methods and full factorial design of experiments. They are used in obtaining the optimal parameter settings for the reflow soldering and is evident in obtaining the thermal profile employed in this research work. Reflow profile parameters optimisation helps to minimise maximum stresses on solder joints.

By IPC/JEDEC standard, the maximum temperature of the assembly should be below 245 degrees Celsius. The time above liquidus temperature should be between 60 and 90 seconds while the initial ramp rate should be 1 degree Celsius/second to 2 degree Celsius/second. A typical target profile illustrated with fluctuating temperatures and time above liquidus for reflow soldering is in Figure 2.13.

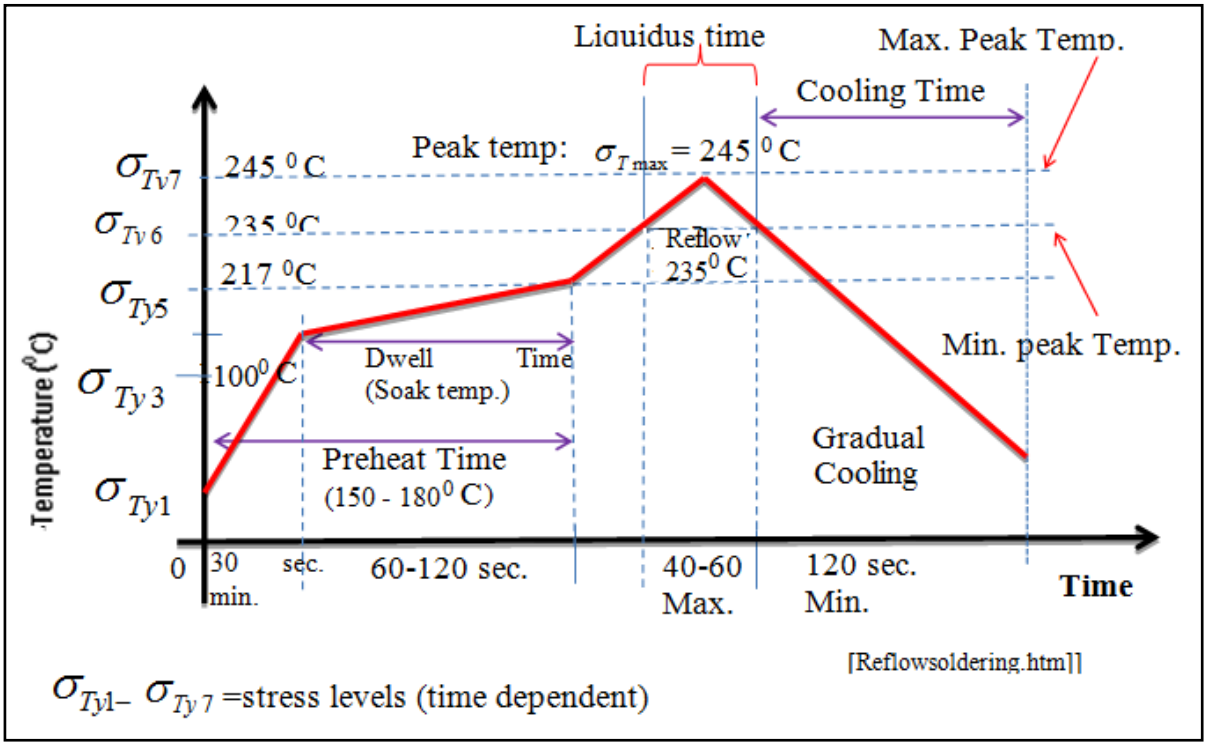


Figure 2.13: A typical target profile for reflow soldering of SMT

2.3.4 Applications of Surface Mount Electronic Components

As electronics technology and their components continue to develop swiftly, consistently meeting previously unthinkable goals, further attentions look towards the production of more electronics applications and the development of systems capable of facilitating human efforts. The SMECs designs are to meet among others, the requirements of three major applications, industrial, military and commercial, regardless of their implication to each other.

2.3.4.1 Industrial Application of SMAT

In overviewing of innovative research methodologies on electronics applications relevant to the industry, the environment, and the society as a whole, a variety of application areas emerge from automotive to space and from health to security. However, individual attention is devoted to the use of SMECs in embedded devices, oil well logging operations (Figure 2.14) and sensors for imaging, communication and control measures (De Gloria, 2014).

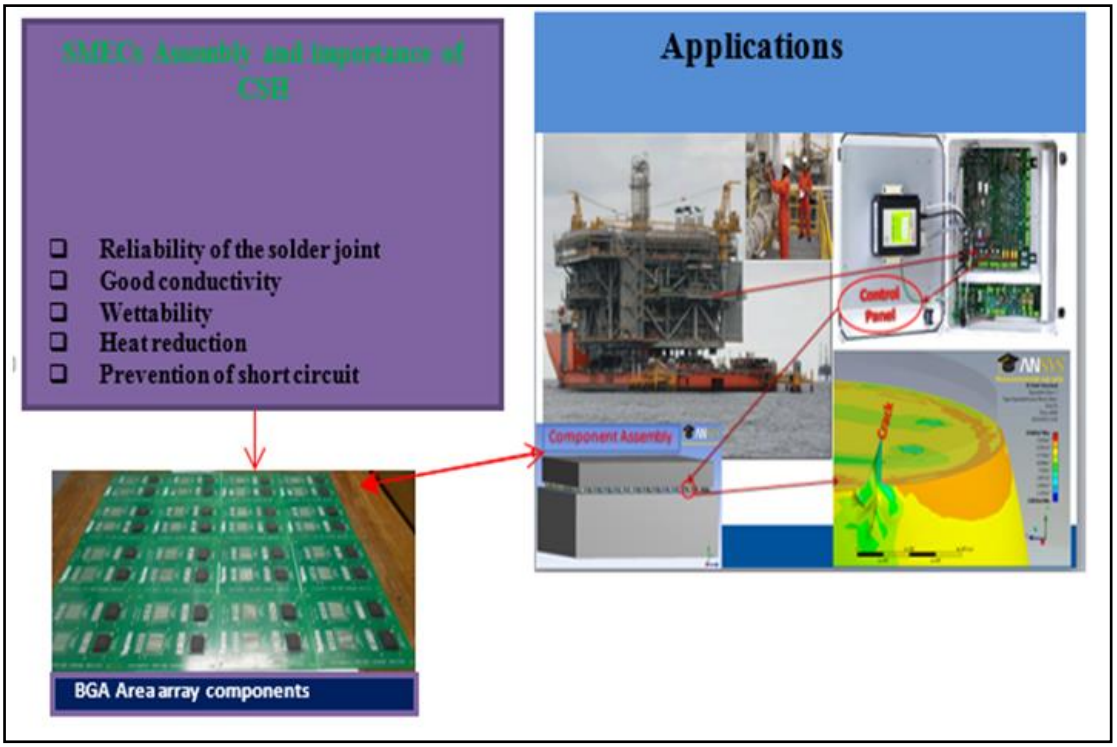


Figure 2.14: Industrial application of SMECs in oil well logging system

Source: **(Amalu and N.N. Ekere, 2012).**

In manufacturing industries, however, SMECs constitute an integral part of a system's central processing unit. SMECs under use condition, problematic and uncontrollable situation, their functions are critical to the overall performance of a system's motherboard interconnect. The importance of SMECs spans through all fragments of modern appliances. In a more diverse form and processes, the components usage are in the development of higher order materials and nanotechnology devices, for example, those that use high-powered Scanning Tunnelling Microscopes (STM) and Atomic Force Microscope (AFM). Advances in the use of SMECs have also tremendously increased the electronics volume functionality and embedded systems software in the industry. Power electronics that use SMECs have further improved the integrated circuits development in electronics industries which according to Gordon's (Moore, 2006) earlier prediction is continually experiencing volume increase in prolific and multiple facets as technology use advances.

More interestingly, the use of SMECs is of credible importance due to their miniaturised size, higher process speed, information storage capacity and prospects for bulk assembly through automation; and in all, they are cost effective. SMECs and SMAT are used in the improvement

of devices to maximise performance and industrial application specific functions (Theodore F Bogart, Jeffrey Beasley, 2013). Their importance also extends to other extensive use applications, which may include quality monitoring systems; including the control of product thickness, weight, moisture content, standoff height of solder joints in assembled components, and other material properties relevant to SMECs. The use of SMECs based electronics amplifier circuits is mostly on automated systems to amplify signals capable of controlling automatic doors, generic power systems and devices for high safety critical measures in the industry and beyond. For example, Power stations producing thousands of megawatts of electric current are measured using tiny electronic devices and circuits; while electronically controlled systems are more compatible with heating and cooling (De Gloria, 2014 and (Theodore F Bogart, Jeffrey Beasley, 2013).

In the automobile industry, there have been an incredible expansion and tremendous economic growth within the last decades. This development had led to severe environmental damage and full spread insecurity in fuel efficiency, which requires protection, and the growing need for customer's environmental safety demand became evident and needed urgent attention. Nonetheless, with the technology advancement in SMECs, automobile manufacturers can offer a variety of electronic systems to their customers and on demand. Take, for instance, those factors, which greatly depend on SMEC integrated circuits, a) the motherboard of an engine control system that incorporates other safety devices like an airbag, automatic brake system and fog light.; b) the dashboard information is provided, however, by the auto electronic control unit, which displays fuel and oil levels to ease refill time; and c) drivers' speed, gear and engine revolutions are made possible and read through the tachometer. All the same, more electronic systems as identified by (Chauhan D. S. and Kulshreshtha, 2009) include but not limited to automobile specific integrated circuits, electronic stability control systems, and Field Programmable Gate Arrays (FPGAs), down to application-specific standard products. Other SMECs products, which offer treasured and expensive premiums to the automobile industries, include traction control devices, anti-lock brake and steering systems.

Johnson et al. (Johnson et al., 2004) stated that the car underhood environment is harsh and this requires that present trends in the automotive electronics industry will be driving the temperature envelope for more electronic components for the niche marketplace. They further indicated that the transition to X-by-wire technology (Kanekawa, 2005) will replace both mechanical and hydraulic systems with electromechanical operations and will also need more

power electronics. Incorporation of power transistors and smart control devices into the electromechanical actuator will require power devices to operate at 175 0C to 200 0C. Hybrid electric vehicles and fuel cell vehicles will also drive the request for high temperature and power electronics devices further. In medical service industries and hospices, there is rapid growth in the use of electronics systems made from SMECs gadgets. Scientists, health and medical practitioners in control of ailments and in diagnosing and treating patients find the gadgets useful. The application of SMECs in medical services has extended to the use of general electronic equipment as in Electrocardiograms (ECG), Medication pumps, X-rays machines and Cathodes filaments, Ultrasound Device Scanners (UDS), and Shortwave Diathermy Units (SDU) for heating up joints. Also, monitors such as thermometers, vacuum pumps, blood pressure and blood sugar gaging tools are actually in use; most of which are user-friendly and electronically operated (Chauhan D. S. and Kulshreshtha, 2009).

In instrumentation technology and acquisition, the assembly of electronics measuring instruments and application devices (Zardini and Deletage, 2011) are not complete without SMECs solder joints that enhance the device thermal-mechanical reliability. The SMEC devices include ammeters, ohmmeters, multimeters and electronics laboratory instruments. Common examples include oscilloscopes, strain gauges, spectrum analysers, frequency counters, and signal generators (Yang, Agyakwa and Johnson, 2013; White, 2008; Theodore F Bogart, Jeffrey Beasley, 2013); and they are of immeasurable help in precise quantity measurements. However, the use of SMECs is common in circuits of automated industrial processes like in most research laboratories and some power stations.

Apart from the numerous advantages derivable from the utilisation of this technology, major concerns and challenges are still attributive to its use in the industry. They include some critical risk factors that have to do with environmental safety and operational security; including the cost of failure, systems monitoring for reliability, equipment maintenance, to mention but a few. Catastrophic failures are avoidable through instrumentation, critical safety and security appraisals and if employed, appropriate use of reliability predictions could determine a suitable replacement period for SMECs.

2.3.4.2 Military Application

SMECs gained grounds in the assembly of high-temperature electronics equipment for military applications. A typical example of SMEC system is the Leadless Ceramic Chip Carriers (LCCCs) developed in the 1960s. The package fabrication is usually at soldering temperatures above normal ambient (specifically 150^0C and above); and by shrinking package sizes for larger pin counts using hermetically sealed devices with leads on all four sides, Prasad (Prasad, 1997). Million Parts from SMECs are installed or delivered to the military for several weapons systems (White, 2008; Meyyappan, 2004), including for example highly sophisticated military aircraft and Marine Corps' helicopters and other weaponry such as Theatre High-Altitude Area Defence (THAAD) missile systems. However, in military aviation, thousands of electronic components necessary for various communications, navigation and avionic control systems which, are incorporated into an aircraft's motherboard to enhance its reliability and safety operation. Defence applications are entirely controlled by electronic circuits (Guerrier et al., 2000; Meyyappan, 2004) which can provide a means of secret communication between military headquarters and individual units using special radar systems. Hence, this has many significant developments in electronics and the industry.

2.3.4.3 Commercial Application

In commercial applications, SMECs and SMAT play a central role in interconnection technology when applied via motherboards, mostly in entertainment and communication networks. In the last few centuries, more than 30 years ago, telephony and telegraphy serve as the primary application of electronics in entertainment and communications system. According to (Thaduri et al., 2013; White, 2008)], the communications industry became revolutionised through the advent of microelectronics. It has been possible for radio waves and messages to pass to different locations and regions without the use of wires. The wireless network development has paved the way for the improvement of digital ICs applied in switching and memory devices, as well as digital signal processing for computation networks and communication satellites (Guerrier et al., 2000; Benini and Giovanni, 2002).

The application of electronic components are virtually found in every industrial segment commercial or military and has increased with today's technology (Meyyappan, 2004). The implementation areas include but are not limited to transportation, communications,

entertainment, instrumentation and control; aviation, IT, banking, medical appliances, home appliances, and manufacturing. In the context of electronics-driven products lifecycle and reliability concerns in accordance to (IPC/JPCA, 2000; Bogart, Beasley and Rico, 2001), efficient management and maintenance culture will be required. For them, an effective product outcome is achievable through accurate experimental methods for solder joints reliability assessment and measurements. The same views were held by (Thaduri et al., 2013; Whalley, 1991; Khatibi et al., 2009; Tu, 2007). The result will help to compare with the predictive assumptions from literature.

2.4 Thermomechanical Reliability of Solder Joints

The thermomechanical reliability of solder joints in microelectronics assembly depends on the standoff height of the component (CSH) used in the manufacture. Thus, CSH of electronic devices has been widely reported to affect the reliability of the devices service life (Arulvanan, Zhong and Shi, 2006; Emeka H. Amalu and Ndy N. Ekere, 2012). At high temperature and harsh environment typical of automotive, aerospace and oil well logging operations, the solder joint reliability becomes more critical because it experiences accelerated degradation, which culminates in premature failure.

The thermomechanical reliability of solder interconnects, including both tin-lead and lead-free alloys, is determined by creep and fatigue interaction of the solder alloy. The CTE mismatch in the system (component, solder, and substrate) imposes cyclic strains (most notably shear strains) in the solder under varying temperatures (Hong, Yuan and Junction, 1998). The spatial and temporal distribution of shear stresses in the solder joint is dependent on the geometrical and material parameters of the interconnect system. The critical concerns may include the CTE mismatch, the range of the temperature variation, the solder joint geometry, the component configuration, and solder joint distribution (Numi, 2005; Alander et al., 2002). Moreover, BGA solder joint (FC-BGA or COB) which is the focus of this study undergoes severe damage due to wear-out, or the severity of the environmental and fluctuating ambient condition during operation. The thermal blueprints of the package are easily exceedable during reflow soldering or thermal ageing, which may lead to spontaneous and or gradual solder joint failures, exhibited through crack initiation, propagation and eventual failure.

The mechanical failures of the solder joint may be due to mechanical overload or fatigue. In their study, (Lai and Wang, 2005) reported that overload failures occur when the stress in the solder joint exceeds the capacity or strength of the solder alloy. For example, in mechanical tests ` such as pull, shear, drop, static bending and impact load, the joints may fail in a single or multiple events. By contrast, fatigue failures happen even at stress levels far below the strength of the solder alloy under cyclic loading and through a wear-out mechanism over a period. The thermal loading imposed by cyclic temperature excursions (cycling or vibration), may consequently lead to solder joint fatigue failure. Thus, SJs exposed to hostile thermomechanical cycling (thermal ageing/creep) during service condition must either retain their integrity or evolve to a coarsened structure. This behaviour might question the functionality, heat dissipation and structural support of a device's operational reliability, which is accessible (Lau and Pao, 1997; Harper, 2000; Emeka H. Amalu and Ndy N. Ekere, 2012). However, to meet the increasing reliability demand of future microelectronics, a critical study with a proper examination of the mechanical behaviour and fatigue properties of exact SJs is required to provide valuable information for new products design and assembly. Previous studies on the actual solder joints assembled with different SMT components are thus imperative and discussed under three sub-headings:

2.4.1 Previous Studies on SMT Chip Resistor SJs Reliability

The reliability of SMT chip resistor SJs despite having components with minimal solder alloy depends solely on rheological properties and the viscosity of its solder paste (Mallik et al., 2009; Amalu, Ekere and Mallik, 2011). However, solder paste unlike in PBGA SJs constitute an integral part of chip resistors solder volume (Figure 2.15) and is available in different alloy compositions. In their study (Jih and Pao, 1995) evaluated the design parameters for leadless chip resistors SJs. They found that failures in electronic packaging under thermal fatigue often result from cracking in solder joints due to creep/fatigue crack growth. However, their shear strain range based on thermal hysteresis response studied the responsiveness of various parameters. Such parameters include solder standoff height, fillet geometry, Cu-pad length, and component length and thickness. The obtained results served as guidelines (using different types of resistors) for reliable SJs design as shown in Figure 2.15.

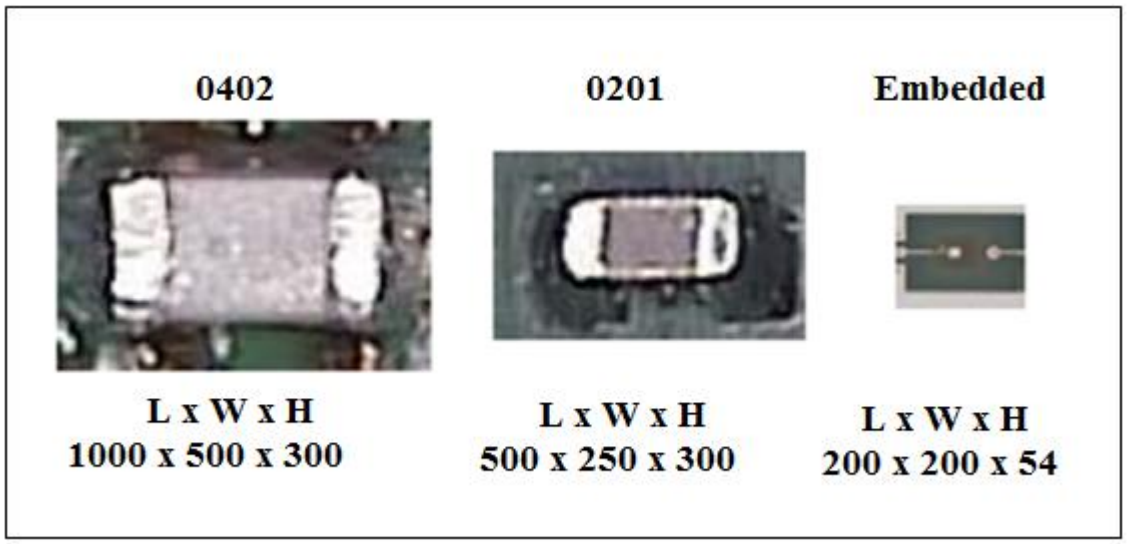


Figure 2.15: SMT and embedded capacitor size comparison dimensioned in µm

Source: ***(Lau, Rice and Avery, 1987)***

In their study, (Stam and Davitt, 2001) analysed the effects of thermomechanical cycling on lead-based (SnPb) and lead-free (SnAgCu) reflow soldering of SMT chip resistor SJs and their results show that the lead-free is a viable alternative for conventional lead based reflow soldering for this component type. They also found that the chosen ternary eutectic solder alloy of SnAg3.8Cu0.7 composition requires higher processing temperatures, which could limit the use of individual board and component models. However, Temperature dependent aspects such as solderability and mechanical behaviour of the lead-free assemblies of chip resistors, as well as the nature of the board, component metallisation and use environment can in effect significantly affect the reliability of lead-free solder joints. The resultant effect is that they could perform better or worse than their lead based counterparts (Stam and Davitt, 2001) could. The same study found that cracks in resistor solder joints could develop from beneath the component either by transgranular (lead-free) grains or along intergranular (leaded) grain boundary within lead-rich and tin-rich areas and into coarsened regions near the component finishes. Nevertheless, (Numi, 2005 and Hariharan, 2007) discovered that thermomechanical stresses and the other factors affecting SMD resistor SJs when compared with PBGA SJs might in principle behave differently. It might mean that their accelerated thermal cycling can also differ, as well as all tests conducted using different components, tests structures, and or tests conditions can also result in various tests results.

2.4.2 Previous Studies on Ball Grid Arrays' SJs Reliability

In SMT acquisition, the reliability of BGA SJs is critical under harsh environment and other control operational and safety-critical conditions, such as in automotive underhood, oil well logging and aerospace applications. Thus, solder joint reliability of a BGA component is the ability of the joints interconnect to retain functionality under use environments. In the past few decades, however, Gull Wing Leads (GWLs) have been primarily in use for high pin count packages, but because of the inherent problems they pose, BGA packages are becoming popular. BGA provides much shorter signal path compared to fine pitch but can be very critical in high-speed applications. Though BGAs according to (Prasad, 1997) "have the greatest use positives, they also have some serious problems, for example, hidden solder joints which are difficult to inspect and rework".

BGAs are not compatible with the hot bar and Laser reflow process because of hidden solder balls concealed from the heat source. Additionally, they are extremely susceptible to "moisture induced cracking". Cracking of the solder joint, caused by thermal fatigue has long, been identified as a primary failure mode in electronics packaging (Waine, Brierley and Pedder, 1982; Guo et al., 1991). Some BGAs of higher package sizes coupled with increased speed and greater density affected by an increase in power dissipation due to higher temperature and temperature gradients (Wang et al., 2013). It becomes imperative to state that the solder joints reliability of BGA components in such abnormal environmental conditions are a big issue in the electronic industry, especially now that much emphasis is on product miniaturisation, which hugely affects the joints integrity during assembly and at service condition. However, (Lall et al., 2004) conducted research on the reliability of BGA and CSP models in automotive underhood applications. They found that the CTE mismatch measured by a Thermomechanical Analyser (TMA) usually begins to change from 10-15°C lower temperatures than it is for the glass-transition temperature (Tg) specified by Differential Scanning Calorimetry (DSC). They also claimed that the variation in CTE could extend to an accelerated test range very close to 125oC. In contrast, a higher CTE in the neighbourhood of the Highly Accelerated Test Temperature (HATT) is unaffected by High Tg printed circuit boards with glass-transition temperatures much higher than the 125°C high-temperature limit. However, thermal fatigue induced by differences in thermal expansion between board and package materials (Emeka H. Amalu and Ndy N. Ekere, 2012) is probably the most common failure mode for BGA packages.A schematic of standard high pin count wire bond and flip chip BGA solder joints' configurations is shown in Fig. 2.16.

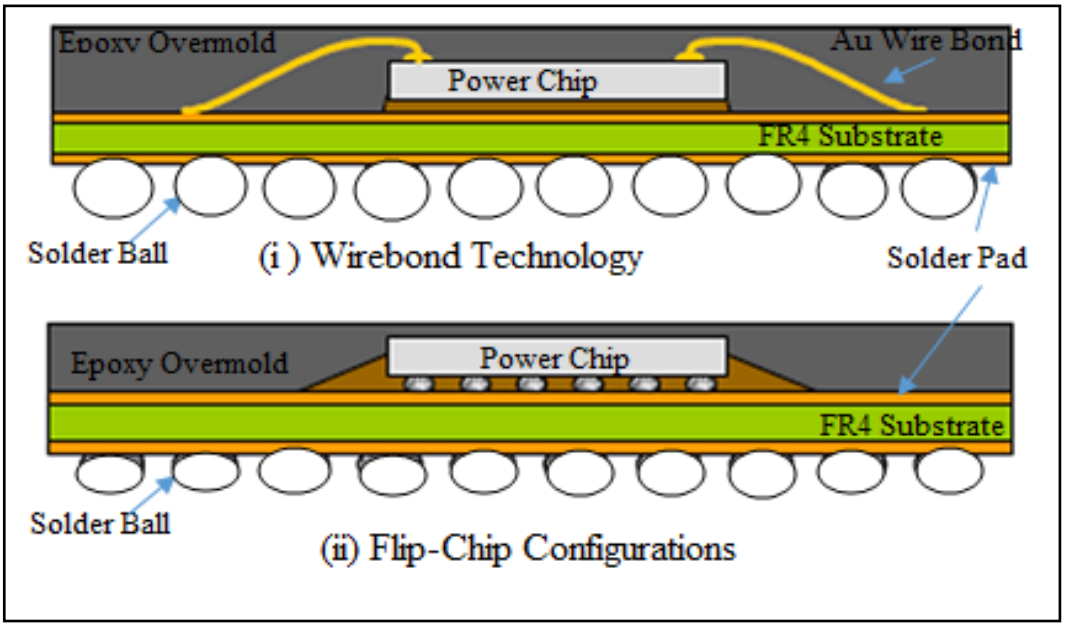


Figure 2.16: Wirebond and flip chip configurations of BGA solder joints.

Source: ***(Kim et al., 2008)***

On further analysis of BGA solder joints', (Kim and Jung, 2004) combined experimental investigation with a nonlinear finite element investigation using an elastic-viscoplastic constitutive design to study the effect of speed of ball shear on the shear forces of BGA solder joints. In their work, they also examined BGA components of two solder compositions, Sn-3.5Ag and Sn–3.5Ag–0.75Cu assembled on Cu substrate with 7μm thick, Ni barrier surface finish, enhanced with 0.5μm thick Au layer for ease of solderability and diffusion. In their results, IMC was identified using energy dispersive spectrometer (EDS) and electron probe microanalysis (EPMA); and in the two solder samples used, they found IMC particles of Ag3Sn and a few of AuSn4. They also reported among other things the presence of a continuous Ni3Sn4 layer near the interface connecting the Au/Ni plated layer and the Sn-3.5Ag.

The formation of a continuous (Ni-xCux)-3Sn4 layer and a small amount of discontinuous (Cu1−yNiy) 6Sn5 particle were found at the interface between the substrate and the Sn-3.5Ag-0.75Cu as reported. Their further results show that shear tests conducted using a shear speed of 100 to 700μm/s and a bumped shear height of 50μm linearly proportional. However, for both experimental and computational results analysis, the authors reported that the shear force also increased linearly with the shear speed and got to its maximum at the highest shear rate. In their analysis of failure mechanism of the test portions using plastic energy distribution and the von Mises stress used to predict the yield of materials under any loading condition from

results of simple uniaxial tensile tests. The mode of fracture found in the tested solder joints was ductile for all test pieces. They finally concluded that the presence of IMC in the solder joints of the tested BGA samples could enhance or temper with the structural integrity of the joints at service condition.

The reliability of BGA solder joints is inherent from a good solder reflow profile, and an optimisation of an individual assembly reflow process can enhance performance. The thermal fatigue lifetimes of assembled BGA systems depend on the specific CTE mismatch between the substrate and the PCB, the standoff height, the size of the package, type of BGA and the kind of solder used (Ning-Cheng, 2002). For a reliable solder joint achievement in the industry, thermal management, therefore, remains an integral part of reflow soldering. To this, the properties characterised with wetting and spreading of eutectic or near-eutectic solder alloys such as Sn96.5Ag3.5, Sn91Zn9, Sn99.3Cu0.7, Sn95Cu4.0AgI, and Sn95.8Ag3.5Cu0.7 as compared with SnPb solder have been studied and reported by (Jiang et al., 2007; Ožvold et al., 2008). According to them, and for all types of solder alloy compositions, wettability, as expressed, is the ratio of wetting angle and the size of wetted surfaces. More significantly, surface properties influence wettability and in correlation with solder alloy proportion. Table 2.3 presents the BGA package types popularly used in SMT while Table 2.4 shows the mechanical properties of the SMT assembly materials.

Table 2.3: Types of BGA, ***Source: (Ning-Cheng, 2002)***

BGA Types	**Construction Details**
PBGA Plastic Ball Grid Array	Organic laminate substrate. Low cost
CBGA Ceramic Ball Grid Array	Co-fired ceramic substrate. Excellent electrical /thermal properties
CCGA Ceramic Column Grid Array	More compliant joint for high temperature or high power applications
TBGA Tape Ball Grid Array	TAB-like tape packages carrier. Good fatigue life
Micro Ball Grid Array (µBGA)	High electric current density-induced interfacial reactions
'Slightly Larger than IC Carrier' (SLICC) package	Solder-bumped IC under development at Motorola. Area efficiency with a direct-chip-attach (DCA) compensates for thermal mismatch b/w the die and the substrate.
TEPBGA Thermally enhanced plastic ball grid array	For HTE.

Table 2.4: Mechanical properties of SMT assembly materials

Source: *(Amalu and Ndy N. Ekere, 2012)*

S/No	Component	Young's Modulus (Gpa)			C.T.E. (ppm/0C)			Poisson's Ratio (V)			Shear Modulus (Gpa)		
		Ex	Ey	Ez	αx	αy	αz	Vxy	Vxz	Vyz	Gxy	Gxz	Gyz
1	Die	13			3.3			0.28			51		
2	Solder Mask	4.1			30			0.4			1.5		
3	Cu Pad	13			17			0.34			48		
4	Sn-Ag-Cu	43			23			0.3			17		
5	Sn-Cu IMC	110			23			0.3			42		
6	PCB	27	27	22	14	14	15	0.17	0.2	0.17	27	22	27

The mechanical properties given in Table 2.4 help in determining the integrity of the bonded materials after assembly. Thus, the joints' integrity depends hugely on the solder alloy composition used during production. At high homologous temperatures up to 523K, Pb-free solders experience higher surface tension and higher viscosity; while as wetting time decrease with increasing temperature ambient for all alloy compositions. The review shows that good wettability is less temperature dependent and identified by the formation of good bonding system that enhances the reliability of the solder joint operation. A summary of the thermal properties of other solder alloys is in Table 2.5.

Table 2.5: Mechanical properties of other relevant metals; solder alloys and IMCs.

Source: (Amalu and Ekere, 2012; Chromik et al., 2005)

Material	Young Modulus of Elasticity, E (GPa)	Poisson's Ratio (V)	CTE (ppm/^{0}C)	Yield Stress σv (MPa)	Tensile Strength (MPa)
Sn	41	0.33	28.8	56	0.11
Cu	114	0.34	16.4	52	1.7
Sn63 Pb37	32	0.4	25	34	0.052
Sn96.5-Ag3.5	53	0.4	22	49	0.16
Sn96.5/Ag3.0/Cu0.5	51	-	23.5	-	0.05
Ag3Sn	88	0.33*	-	970	2.9
Cu6Sn5	119	0.33*	-	2200	6.5
Cu3Sn	143	0.33*	-	2100	6.2

2.4.3 Previous studies on SJR of other electronic components

The challenges in the thermomechanical reliability of the solder joints of other SMT electronic components can be of similar characteristics to those of resistor and the BGA solder joints as earlier discussed in section 2.3.1 as well as 2.3.2. However, the reliability of electronic assemblies is subject to having a good design effort, executed concurrently with the other design functions during product development stage. The solder joint reliability of such other electronic products is obtainable through consistent, high-quality manufacturing and adherence to standard guidelines for surface mount packages (Lau, 1991). For example, IPC-D-279, design guidelines for reliable surface mount technology printed board assemblies, and IPCSM-785 guidelines for accelerated reliability testing of SMT solder joint attachments developed according to (Engelmaier, 1989) for this same quality purpose.

In the context of these standards, however, reliability is defined under SMECs as 'the ability of an SMEC product/system/solder joint to function under given conditions and for a specified period without exceeding acceptable failure levels'. Based on this definition, the reliability of solder joints is challenging because of compact devices with denser interconnections and today's emerging new technologies have packages characterised by less high, finer pitch, and materials that are more complex. The challenge in meeting the ever-increasing demands for electronic products that are more durable, cheaper, compressed and performs at a higher speed is also becoming critical. This challenge is crucial because "signal propagation in high-speed and high-frequency electronic assemblies is more sensitive to interconnect degradation than it is in low-frequency electronic assemblies. Due to surface concentration; however, a small crack on the surface of solder joints can directly impact signal integrity, which may reduce the performance of high-speed electronic products" (Kwon, Azarian and Pecht, 2008). The various challenges envisaged necessitate applying appropriate manufacturing design tools such as Design for Manufacturability (DfM), 'Design for Testability' (DfT) and 'Design for Reliability' (DfR) (Chen et al., 2010); to achieve the solder joints' reliability requirements in SMT.

The reliability of electronic components can depend on the nature of the substrate/lead compliance system and the use environment of the assembly. Noncompliance of these factors and to moulding process parameters can result in solder joint failure. However, and as previously discussed, there have been health and environmental concerns associated with lead which has prompted increasing demand for lead-free solders in the electronic packaging industry since July 2006. Most prominent among the associated lead-free solders is the Sn-Ag-

Cu solder alloy, which has good potential in replacing the conventional Sn-Pb solder paste/alloy. Sn-Ag-Cu solder paste can function in many applications owing to its strength, thermomechanical fatigue behaviour and creep resistance capability when subjected to high-temperature service conditions during operation (Kim et al., 2012).

2.5 Reliability Challenges in Solder Joint Technology

Solder joint technology (SJT) encounters numerous reliability challenges and failure mechanisms during and after its manufacturing process. In the electronics industry, the assembly of weak solder joints resulting from misalignment issues; solder splattering, de-wetting, delamination, voiding, Pop-corning and cracking effects constitute among others major challenging issues currently existing in the packaging of electronic products, especially in area array packages and fine pitch technology. The understanding of why and how the assembled solder joints of microelectronics devices on PCBs or other surface-base metals fail is essential to improving R&D prognosis for product quality enhancement. Designs for accelerated thermal cycling used in the investigation of the solder joint long-term reliability, thermal conditions of BGA solder joints on a microelectronic application in the laboratory and lifetime predictions employing Coffin-Masson's equation for solder joint cycles to failure and crack initiation measurements are also part of the problems associated with SJT.

2.5.1 Reasons for Solder Joint Failure

Solder joints in electronic manufacturing refer to the solder connections between a semiconductor package and the mounted application board in which they function (Sangwine, 1994). Solder joint failures occur for various reasons. These include weak solder joint design and PCB layout, poor solder joint processing during assembly, solder material issues involved before reflow soldering and excessive stresses applied to the solder joints during processing. In general, solder joints failure classification is by the nature of the forces that caused them, including the mode in which they fail. A solder joint can sustain more than one type of stresses in a given situation and may degrade due to the occurrence of other factors such as corrosion (Sangwine, 2007). Most solder joint failures fall into three broad categories described in Sections 2.5.2 and up to 2.5.5.

2.5.2 Solder Joint Fracture Due to Stress Overloading

The fracture due to stress Overload is the type of solder joint fractures attributed to tensile rupture or to short-term weight overloading which is those experienced by components subjected to mainly gross mishandling or misprocessing, especially after mounting these elements on the application board. The fracture often occurs because of an accident, wear-out or harsh treatment. These cases bring the parts to thermomechanical stress levels that exceed the fracture strength of the solder joints, resulting in solder joint failures (Sangwine, 2007); Emeka H. Amalu and N. N. Ekere, 2012; Hu et al., 2014). The situations, which may lead to solder joint fracture due to mechanical overloading, includes accidental dropping of a device or assembled product on the floor or from a height. It could also result from applying force to an improperly loaded application board into its module or enclosure, storage, humidity, chemical contamination, mechanical/thermal shock, vibration and high-impact collisions involving a module containing an application board. These incidents can trigger off solder joints of a device to very high shear stresses. They may tend to rip them off from their metallised baseboard, and may subsequently lead to catastrophic damage or failure during operation.

2.5.3 Solder Joint Failure Due to Creep

The 'Creep Failure' in the context of a solder joint is one subjected to permanent mechanical loading and which degrades over time (to reduce the load) and eventually fail. The failure phenomenon by creep is time-dependent deformation. It is more pronounced at higher temperatures (High viscosity) (Radivojevic et al., 2007); though solder joint failures due to creep at ambient temperature condition can occur (Low viscosity). Solder joints of Chip components can experience both condensed and liquid state and time-dependent viscoelastic deformations due to overload stress, electro-migration and under-bump metallisation (UBM) during temperature cycling. Figure 2.23 (ii) presents solder joint’s failure due to creep in the form of permanent hardening (plasticity) or steady state gradual deformation. Nevertheless, at this room temperature solder already experience high-temperature gradients. For example, if the melting point of a typical solder paste at a chamber temperature of 298 K (25Celcius) is 490 Kelvin (217 Celsius), then the homologous temperature using Equation (2.1), is calculated. The homologous temperature as defined by (Ma and Suhling, 2009) is the ratio of the temperature of the material and its melting temperature in degrees Kelvin given by (Eq.2.1).

$$T_h = \frac{T_s}{T_m} \quad (2.1)$$

, where:

T_h = homologous temperature; T_s = Temperature in service condition;
T_m = melting temperature of solder and T_h = 0.61 (using (2.1).

The homologous temperature of 0.61 obtained is slightly above the critical creep value of 0.6, a potential instance for a creep fracture. Other instance of a failure mainly by creep occurs during reflow soldering and only for an insufficiently supported assembly. Subsequent soldering may lead to larger permanent board warp whereas the joints might be in an almost stress-free state. However, if this board capsized into an enclosure and firmly forced down flat, it might exert substantial forces on the joints and may cause cracks during the mounting operation (overloading) or soon after that (Yao, Qu and Sean X. Wu, 1999).

Solder interconnects suffer creep deformation arising from induced strain owing to changes in temperature ambient and CTE mismatches between the assembly solder joints which may contract or expand due to fluctuations in the temperature gradient. Different materials have different CTEs for example, an Al_2O_3 chip carrier is 6 ppm$^oC^{-1}$, silicon chip carrier is 3 ppm°C^{-1}, and an organic chip carrier is about 17 ppm°C^{-1}). The shear strain imposed on the solder joints according to (Frear et al., 2008; Tu, 2007; Borgesen et al., 2013) is determined by the relation given in Equation 2.2.

$$\Delta\gamma = \Delta\alpha\Delta T\frac{a}{h} \quad (2.2)$$

, where:

$\Delta\gamma$ = the imposed shear strain,
$\Delta\alpha$ = the difference in CTE between the assembled materials,
ΔT = the temperature change,
a = the distance from the neutral expansion point of the joined materials, and
h = the interconnect thickness (height/CSH).

From all indications, however, creep resistance to solder interconnect materials is crucial to the mechanical reliability and integrity of the solder joint, and hence solder interconnects undergo creep for the relaxation of the imposed stresses on them. In effect, therefore, Creep manifests itself by controlling the amount of stress relaxation that will take place in a given time and at a given temperature in the field or chamber. The greater the stress relaxation through creep in

the solder for instance, the greater will the mechanical damage to the solder structure become. On the other hand, high rates of strain have a significant elastic strain component and therefore a minimum effect of creep. The reason for this is that low levels of strain allow creep to play a role while maximising its plastic strain damage.

Since the solder joint (under study) is a material which after it has gone through reflow soldering and the isothermal ageing process was hardened, it is thus more challenging and harder to initiate any damage in the stress-life of the material except for situations involving shear, primary elastic deformation or creep. The component under these conditions, however, is expected to have a long life cycle time in the field. Moreover, for situations involving high stresses, high temperatures, or stress concentrations such as voids, notches or discontinuities such as circulars or circumferential grooves (stress raisers); where significant plasticity can be involved, the loading is not characterised by stress amplitude, σ_a but rather by the plastic strain amplitude, $\Delta\varepsilon_P/2$. It follows that for a given plot of $\log(\Delta\varepsilon_P/2)$ versus $\log(2N_f)$ under these conditions, a linear regression performance such as the one shown in Figure 2.17 is evident.

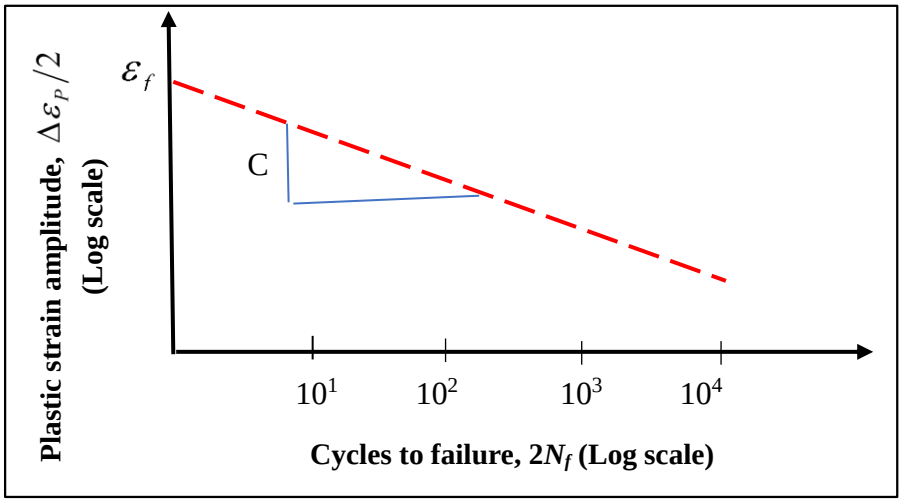


Figure 2.17: Linear behaviour of plastic strain amplitude versus reversals to failure

Source: (Manigandan et al., 2014)

The behaviour is therefore generally represented by creep properties which are an integral part of a fatigue equation proposed by Coffin-Manson, 1955 (Hariharan, 2007) as given in Eq. 2.3.

$$\frac{\Delta\varepsilon_p}{2} = \dot{\varepsilon}_f (2N)^C \qquad (2.3)$$

, where:

$\Delta\varepsilon_p/2$ is the plastic strain amplitude,

$\dot{\varepsilon} f$ is an empirical constant known as the *fatigue ductility coefficient*, (which is the strain failure for a single cycle);

$2N_f$ is the number of cycles to failure (N cycles),

C is an empirical constant known as the *fatigue ductility exponent*, (which ranges from (0.5) to (-0.7), in most cases for metals in time independent fatigue).

In the event of a cyclic loading condition, a common stress history shown in Figure 2.18 has equation parameters given in Table 2.6 and used for appropriate graph measures respectively.

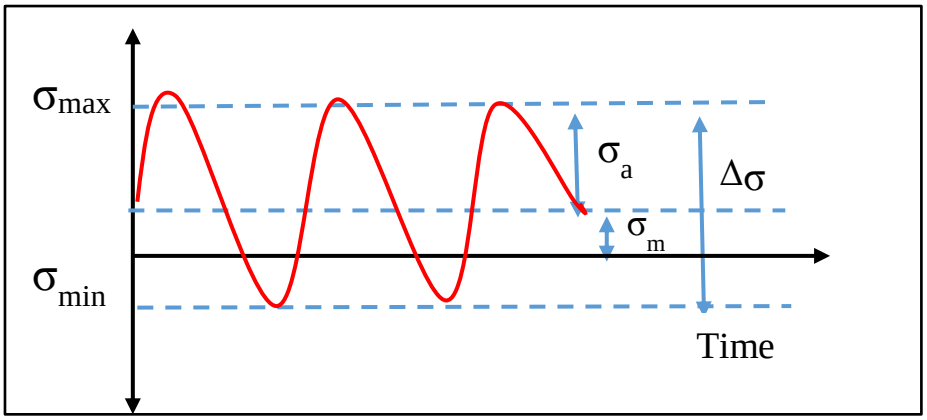


Figure 2.18: A typical time dependent stress history during cyclic loading

Table 2.6: Measurements parameters for a time dependent stress during cyclic loading

The stress range	$\Delta\sigma = \sigma_{max} - \sigma_{min}$
The stress amplitude	$\sigma_a = \frac{1}{2}(\sigma_{max} - \sigma_{min})$
The mean stress	$\sigma_m = \frac{1}{2}(\sigma_{max} + \sigma_{min})$
The load ratio	$R = \frac{\sigma_{min}}{\sigma_{max}}$

Notably, the slopes of a fatigue ductility exponent using (Eq. 2.3) can be considerably steeper in the presence of creep or prolonged environmental interactions. However, creep failure is a

'time bomb' type of failure mode as the stresses are low enough to delay the failure for hundreds or thousands of hours after the formation of the solder joint. Creep occurs most often in devices such as system connectors where there are significant torque or dead weight loading conditions. In principle, it could be a scenario where the torque might remain applied over an extended period without impedance. Certainly, the case is not different in electronic solder joints; since there is little or no relaxation in the joint and not so often that they could in practice, be easily recognised, during use condition. Nevertheless, Creep is usually observable in three stages as shown in Figure 2.19. The first is the primary stage which is in most cases short and decelerating in nature. At this primary level, it is easy to observe any microstructural evidence of creep damage from the material. The secondary stage is the steady-state creep, characterised by a constant strain rate which is taken to be the mainstream and useful life of a product or system. In this juncture, work hardening rate is balanceable by thermally activated recovery rate, coupled with individual voids which start to occur at microstructure level. The last is the tertiary stage which is categorised with unstable acceleration till rupture (if any) takes place. In principle, the solder materials experience higher strain rates at the tertiary creep region than it does at the secondary creep level. Since creep is a time-dependent deformation, and during loading under constant stress, the strain often varies as a function of time and in the manner already discussed and indicated in Figure 2.19 below. The equation, which governs the rate of steady state creep, is an Arrhenius equation presented in Eq. 2.4:

$$Creep\ Rate = \dot{\varepsilon} = A_0 \sigma^n \exp\left[\frac{-Q}{R_G T}\right] \tag{2.4}$$

, where:

A_0 *and* n, are creep constants,

Q is the activation energy for dislocation motion,

R_G is the universal gas constant,

$\dot{\varepsilon}_c$ is the creep strain rate,

σ is the applied stress, and

T is the absolute temperature respectively.

The Garafalo hyperbolic sinh and the second power equations, which cover, creep in the low to medium stress range, and which captures the dislocation glide and its mechanism are not within the scope of this work and therefore not discussed.

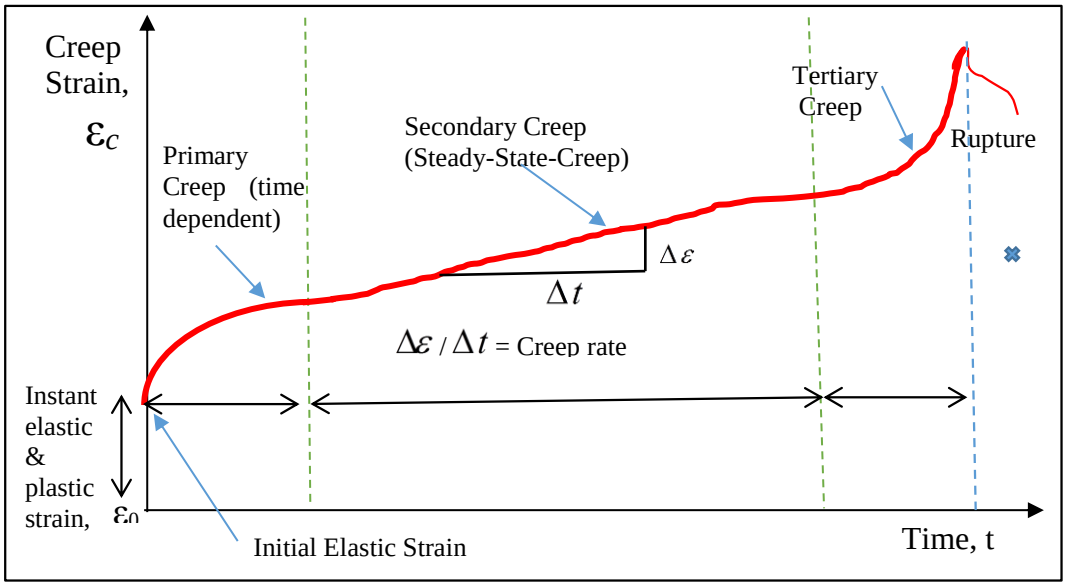


Figure 2.19: Stages of a typical creep strain curve under constant load

Source: (Perkins, A. E. and Sitaraman, S. K. (2008))

2.5.3.1 Heat Affected Zone (HAZ) and Creep Relaxation in Solder Joint

The Heat Affected Zone (HAZ) in the context of this research work refers to some structural and metallurgical changes occurring directly adjacent to the soldered region due to elevated temperatures (temperature variations and cycling) considered not high enough actually to melt the solder alloying material to effect proper bonding. The structural and material composition of the bonded interface in solder joints negatively are often, altered in this HAZ region due to high-temperature excursions they experience during soldering. During soldering with Sn-Ag-Cu solder paste, however, too much heat and too much flux could generate an HAZ region which may lead to low impact strength (or brittleness) resulting from recrystallised and coarse grain growth structure of the joint. In practice, having a long HAZ length (or HAZ with a large surface area) may lead to a low standoff height. Hence it is unwise to bend or shear the solder joint within its HAZ during the bending or destructive shear force exercise.

Research has shown that "a high-strength gold wire bond has a shorter HAZ length than a standard 4N type, which should translate into a lower looping height" (D. Liu et al., 2011). In principle, the height of this loop affected by the length of the HAZ occurring along the wire axis from the solder ball, which invariably depends on the magnitude of the conductive heat

flux along the axis of the wire during metallisation process. However, in advanced solder joint's packaging applications, and in a bid to control the machine process parameters, there are choices to be made which include the reflow soldering profile for the right solder bumped loop vis-a-vis the CSH, the right type of solder paste formulation and substrate material with a particular HAZ length.

The size and the radius of the solder joint are completely dependent upon the dimension of the HAZ. Nevertheless, since the area of the fine-grained HAZ is a critical place regarding creep strength and thermal fatigue, may need a full knowledge of the area and sub-areas of HAZ, to assess and enhance the adhesive force of the joint for reliability purposes. Thus, HAZ is often the cause of future damage experienced from many devices where soldering technology has been employed in solder joint formation, repair or rework. Other reliability concerns associated with HAZ in solder joint are also found at the bond pad interface (base metal), encompassing growth of IMCs, voids and Kirkendall effect which might lead to undue degradation of the joint's integrity and eventual failure. Figure 2.20 shows metallised solder joints formed by fusion, pressure induced soldering, and the HAZ in each case as clearly indicated.

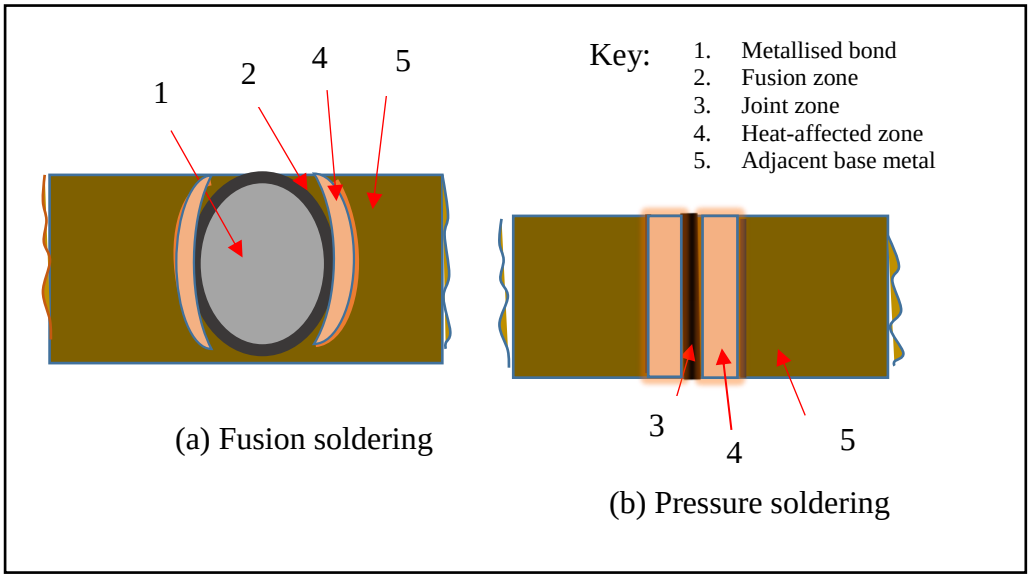


Figure 2.20: HAZ of solder joints formation

Stress relaxation measurement of HAZ is a better way of estimating solder resistance against a load after reaching a certain instantaneously applied strain. In a relaxation test, a decrease of stress in relation to time is the measured parameter, while the total flexible strain (elastic + plastic) kept constant. Stress relaxation testing is significant to a given experimental design

because of its ability to provide a large number of data points for the steady state strain rate against stress curve over a relatively compressed time scale compared with an equivalent experimental time required with constant creep test method described in Figure 2.19.

Furthermore, the relaxation rate of a solder joint depends on an initially imposed strain to it and is different for each alloy type used (Dusek, Wickham and Hunt, 2005). A typical stress relaxation graph plotted by same authors for a comparative room temperature data as demonstrated in Figure 2.21 has three alloying systems and a shear strain displacement of 0.06, typical of that for 2512-type resistor joints; while a shear strain of 0.03 would be typical of 1206-type resistor components respectively. The graph depicts that stress relaxation expressed as normalised stress in percentage (%) is equal to the real stress as a ratio of the nominal stress, and any differences in the behaviours of the three solder material joints are noticeable in the given graph.

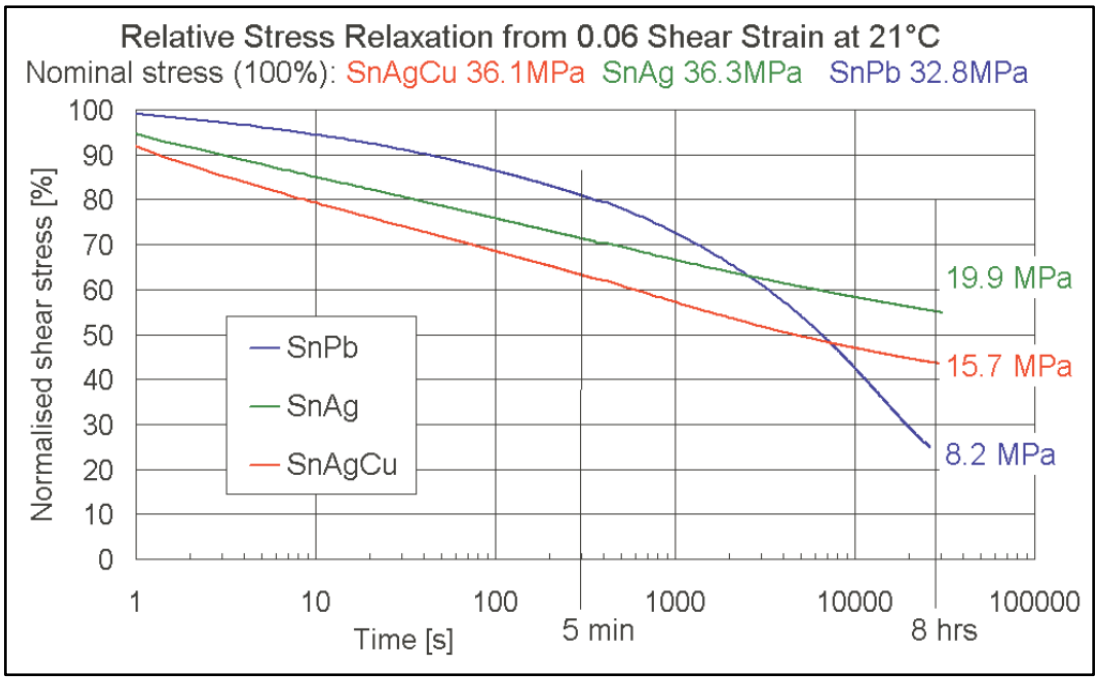


Figure 2.21: Stress relaxation from 0.06 shear strain for three alloys

Source: (Milos Dusek and Christopher Hunt, May 2005)

2.5.3.2 Hysteresis Loop

The stress-strain response of a cyclically loaded solder joint material is in the form of a hysteresis loop. Research has shown that both stress relaxation and creep occur simultaneously

in a system only at hold times when the system is neither load nor displacement controlled (Lau and Pao, 1997). However, the shape of a hysteresis loop usually reflects how time-dependent plastic deformation flows during loading and unloading due to temperature variation. In a situation where there is insufficient relaxation data at the hold time for creep properties determination, a heightened stress level or more prolonged dwell time may be required.

A hysteresis loop often is characterised for example by its stress range, Δσ, and strain range, Δε. Nonetheless, the strain range is often broken up into the elastic and plastic part as shown in Figure 2.22 respectively. The total Strain, Δε is the sum of both the elastic and plastic strains. It is no doubt that in solder joint reliability assessment, the hysteresis loops provide useful information for its engineering and statistical evaluations.

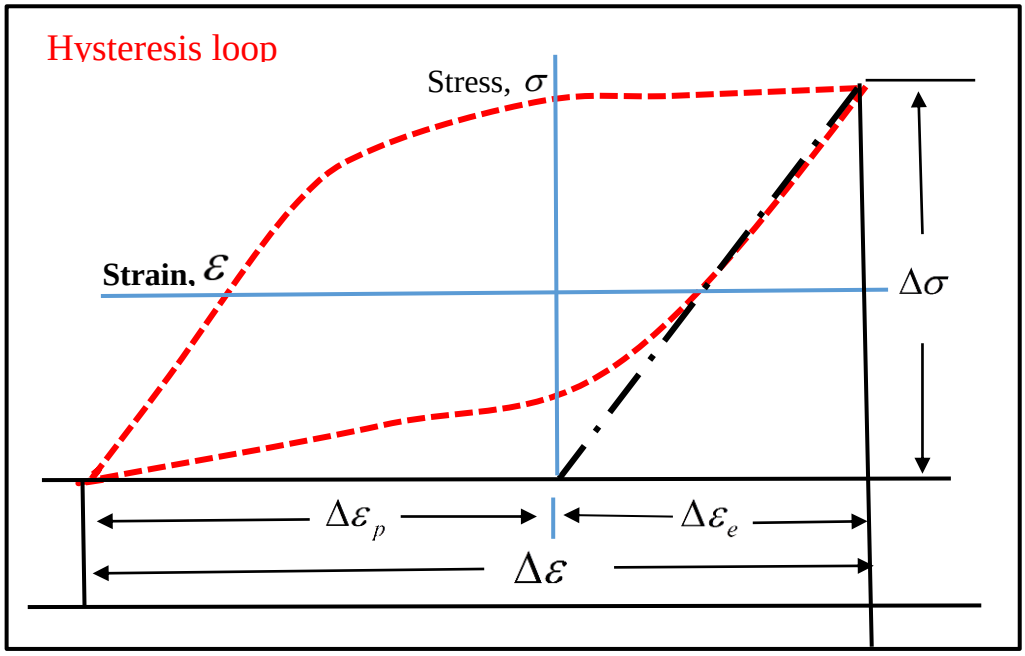


Figure 2.22: Stress-strain hysteresis loop after a second reversal

2.5.4 Solder Joint Failure Due to Fatigue (SJFF)

Fatigue, or failure resulting from the use of cyclical stresses, is the third type of solder joint mode of failure and often considered the largest and most critical failure classification. SJs fatigue failure (SJFF) attributed primarily to stresses brought about by temperature swings and mismatches between the CTEs of the mounted devices' solder joints and the application motherboard. Under these circumstances, it is possible for failure to occur at a stress level

considerably lower than the tensile or yield strength (within the elastic limit) for a static load as can be seen in Figure 2.23 (i).

During the fatigue process, consecutive metallurgical phenomena occur. As the strain in the joint exceeds the plastic limit, the solder will start to creep until spontaneous rupture occurs (Sangwine, 2007); Xu et al., 2015; Shirley and Spelt, 2009) as shown in Figure 2.23 (iii). Failure mechanisms associated with fatigue failures in real life situations, for example, include daytime powering up of equipment and turning it off at night. Next is a frequently repeated cycle of driving a car and parking it with the application board under the hood and the orbiting of a satellite that exposes it to the alternating direct heat of the sun and cold vacuum of space. Fatigue damage, however, accelerates by corrosion and it is one of the most significant menaces to the integrity of solder joints.

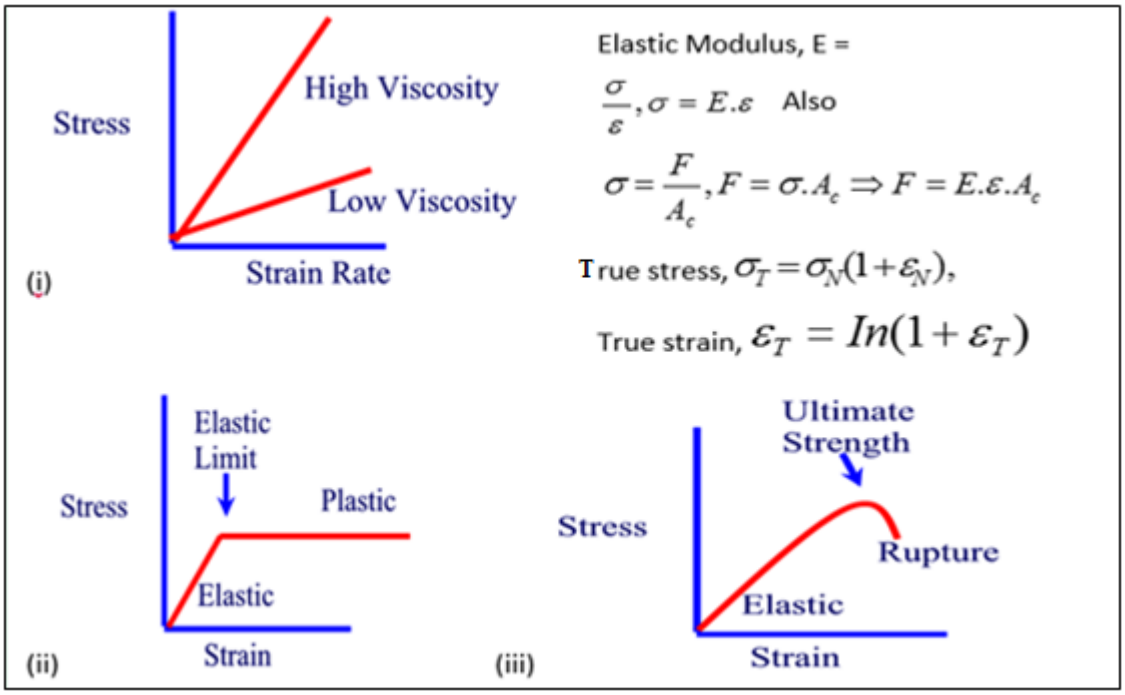


Figure 2.23: Viscoelastic deformation of solder joints & basic formulas

Fatigue damage and progression include the "start of the crack, generally under the component at the edge of the metallisation, progression of the crack to the outer surface of the fillet, first visible at the corners of the metallisation. Others include the growth of the visible cracks from the corners of the component to the middle of the joint, and sometimes, depending on the configuration" (Yao, Qu and Sean X. Wu, 1999; Xiao et al., 2013; Matin, Vellinga and Geers,

2007). The cracks may follow the interfaces between solder/component and solder/PCB. The schematic in Figure 2.24 illustrates the solder joint fatigue damage process classified into crack initiation, propagation and catastrophic failure.

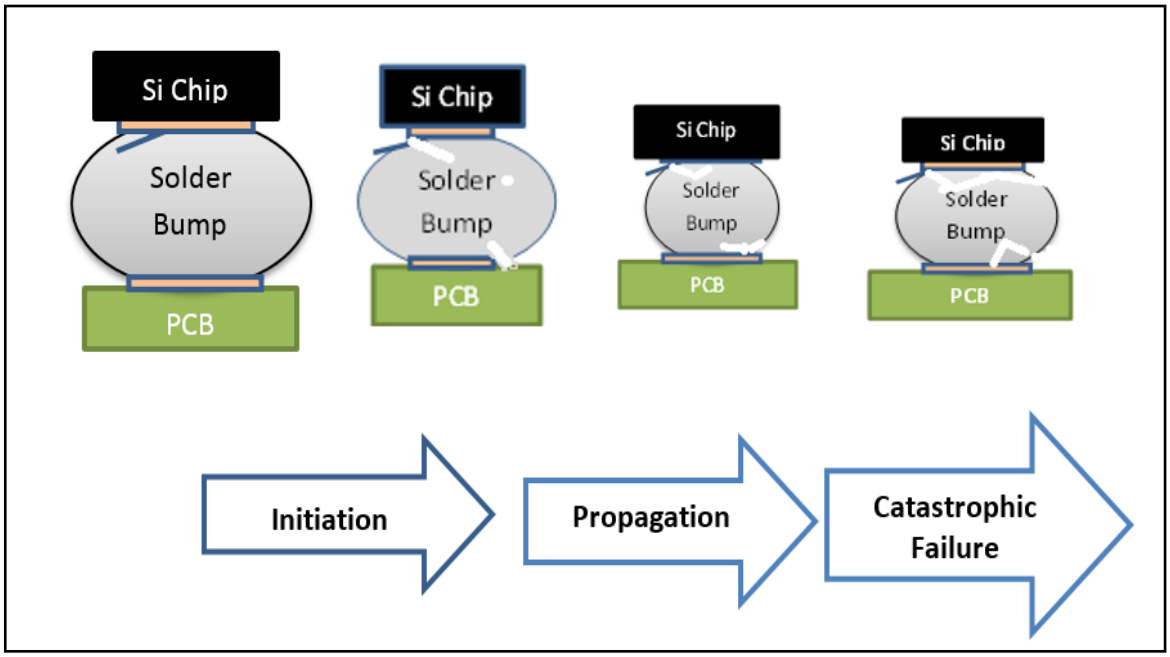


Figure 2.24: Solder joint fatigue damage process

2.5.5 Solder Joint Failure Due to Voids Formation

Voiding in BGA has been controversial. On the one hand, considered an empty stress concentration. The presence of voids as expected can reduce the impact strength, ductility, creep and fatigue life of the mechanical properties of joints. It can also make on-site heat, thus reducing the reliability of the joints. On the other hand, a gap is considered, also as a crack terminated (Lee et al., 2002). For the vibrating instrument, voids are riskier than others are because of vibration effects. Voids can cause a break and disconnect the components from the board permanently.

2.6 Types of Voids and Root Causes

Several types of voids exist such as Macro voids, Planar Microvoids, Shrinkage voids, Micro via voids, Pin Hole voids and Kirkendall voids (Ladani and Razmi, 2009; IPC/JPCA, 2000).

2.6.1 Macro Void

The macro voids generated by the evolution of volatile ingredients of fluxes and solder pastes are in Figure 2.25. The voids location are anywhere in the solder joint, precisely with 100 to 300 µm (4 to 12 mils) bond pad diameter. Macro voids are not unique to SnAgCu (LF) solder joints and sometimes referred to as "Process" voids. IPC Specs' of 25% is the maximum area targeted for Macro Voids (Otiaba, Okereke and Bhatti, 2014; Aspandiar, 2006).

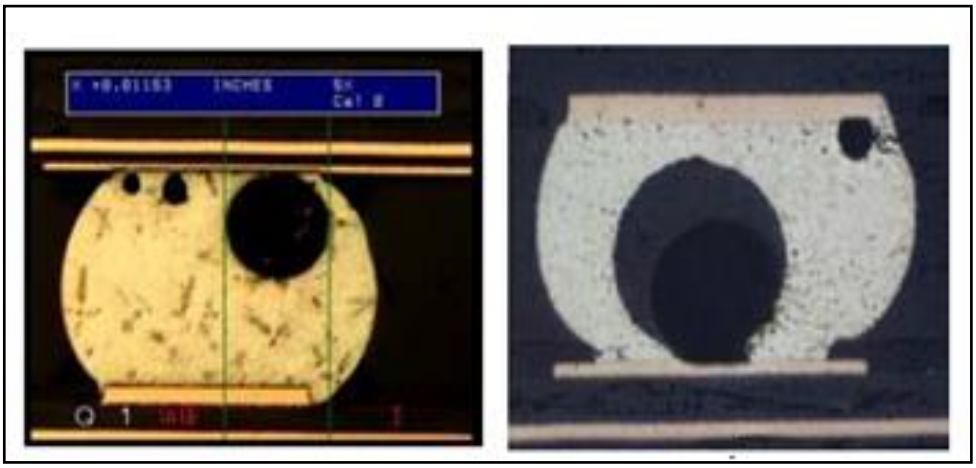


Figure 2.25: Macro Voids

Source: ***(Ladani and Razmi, 2009; IPC/JPCA, 2000; Pang, 2006)***

2.6.2 Planar Micro Voids

The Planar Micro Voids shown in Figure 2.26 could be as smaller as one to two (1-2) mils in diameter when measured. Microvoids location is found in one plane at the land to solder interface above the intermetallic compound. These Micro Voids are prone to jeopardising the integrity of the bonded materials and are responsible risk factors for reliability failures of BGA and other solder joints (Aspandiar, 2006; Pang, 2006; Chuang et al., 2012).

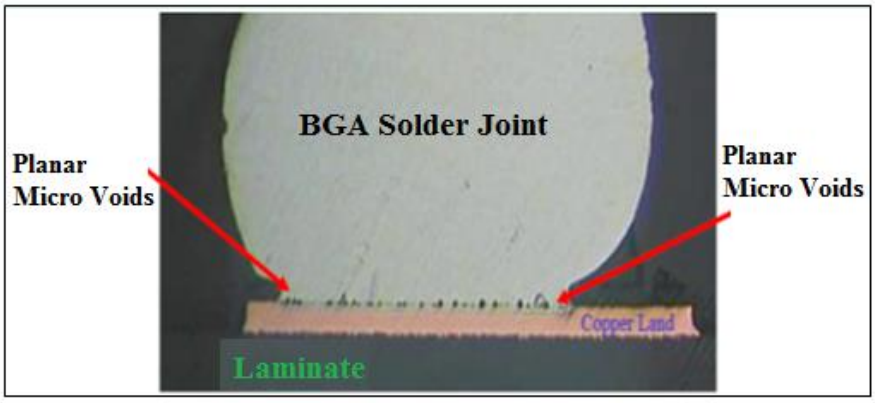


Figure 2.26: Planar Micro Voids

Source: ***(Towashiraporna et al., 2004; Said et al., 2012; Aspandiar, 2006; Pang, 2006)***

2.6.3 Shrinkage Voids

The 'Shrink-Hole-Voids' presented in Figure 2.27 are elongated voids with rough, dendritic edges emanating from the surface of the solder joints. These are not just in BGA solder joints, but also in 'Through-Hole' and 'Chip Size' component solder joints. It could be effects resulting from slow cooling of solder system. It is not a crack, does not continue to grow under thermomechanical stresses and does not affect reliability. This behaviour is called, sometimes 'sink holes' and 'hot tears' (Aspandiar, 2006).

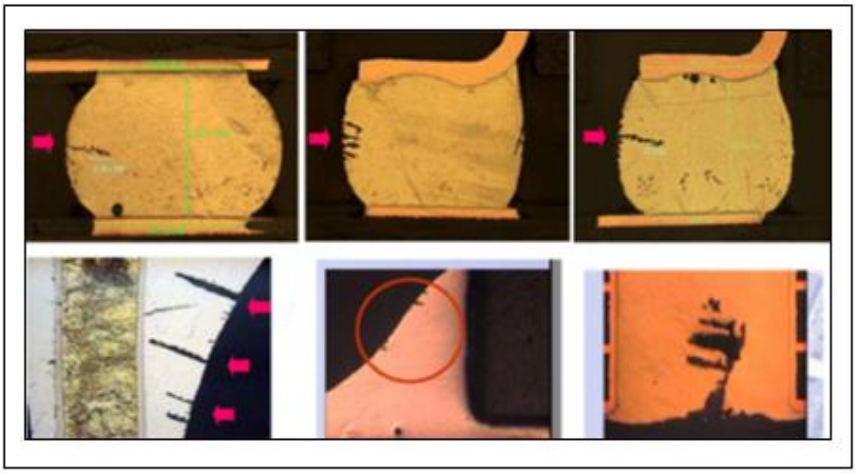


Figure 2.27: Shrinkage Voids

Source: ***(Borgesen, Yin and Kondos, 2012; Yu et al., 2008)***

2.6.4 Micro-Via Voids

These are voids generated due to the presence of a Micro via in the BGA land. Microvias incorporation is mainly into the product design boards, and their recommendation is for greater flexibility. They help to enhance or create vias or rather routeing rooms in a denser part of a substrate for component placement and interconnection of both outer and inner layers, mostly regarded as via-in-pad. This technology is one solution to the challenges mostly imposed by miniaturisation in today's electronic assemblies, especially in the interconnection between different layers of the PCB. The vias according to IPC-6012A and IPC-2315 standards (IPC/JPCA, 2000; Bakhshi, Azarian and Pecht, 2014), are considered as 'blind and buried vias', which are equal to 6 mils or 152 microns. However, quantifying Micro via voids' number and size by cross sectioning may be too small to detect by an X-Ray machine. The risks of Microvias detrimental effect on solder joint reliability is high, and one has to explore ways to reduce them by following techniques of 'double printing', increasing micro vias diameter and plating micro vias shut. Microvias are at present not used on PC desktop motherboards (Dudek et al., 2010; Ladani and Razmi, 2009). A schematic of Micro via(s) is presented in Figure 2.28 when closely observed.

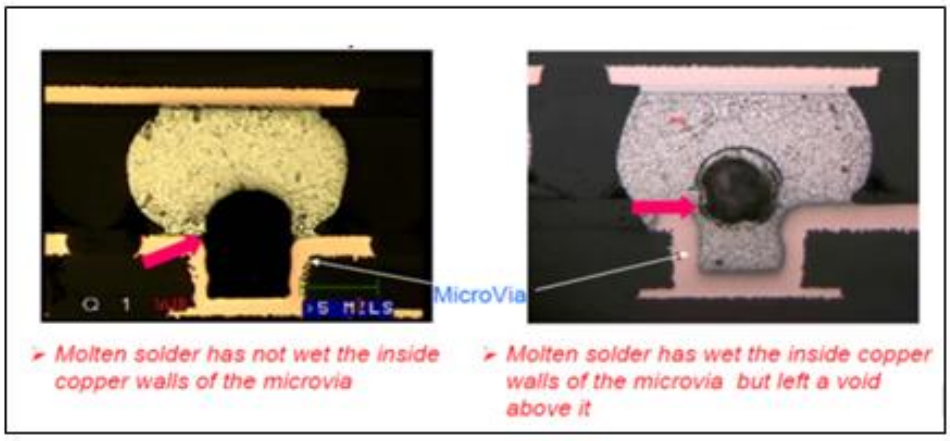


Figure 2.28: Microvia Voids (Holden, 2008; Aspandiar, 2006)

2.6.5 Pin- Hole Voids

Pinhole voids, seen on BGA land pads of incoming boards are caused by PCB outgassing through either Sn-Cu plating or voids in the plating during reflow soldering process. They are Root Causes to copper plating issues at board supplier level. Pinhole voids are a reliability risk (Aspandiar, 2006; Date et al., 2011). The plating in THT should be about 25microns to hinder

board moisture content turning into water and escaping or outgassing through the Cu wall during soldering. Figure 2.29 presents typical examples of pinhole voids.

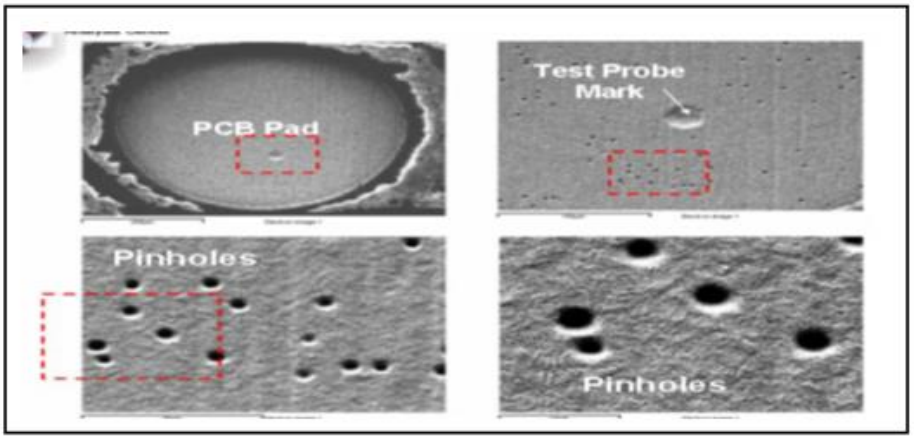


Figure 2.29: Pinhole voids

Source: ***(Aspandiar, 2006; Date et al., 2011)***

2.6.6 Kirkendall Voids

Kirkendall Voids displayed in Figure 2.30 formed within the IMC layers and typically found between solder joints and copper land pads. SAC solder joints of CSPs observed to grow these Kirkendall voids when baked at temperatures above 100^0C. The growth rate was exponential with temperature and therefore increased significantly at higher temperatures (particularly 125^0C and above) during the baking period (Pang, 2006; Kim and Yu, 2013).

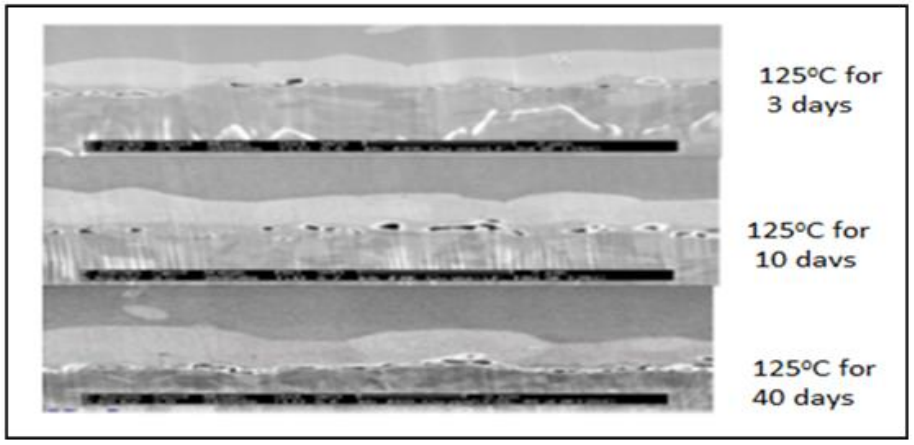


Figure 2.30: Kirkendall Voids

Source: ***(Ladani and Razmi, 2009; Njoku, Mallik, Bhatti, Amalu, et al., 2015)***

2.7 Failure Analysis of BGAs Solder Joint

The failure analyses of BGA devices has cost as its first consideration. A diagnostic test of the instrument is always required foremost at the assembly level to identify specific functional faults and their implications to the BGA assembly. The possible analysis may include non-destructive tests performable at the assembly level. Failure investigation in BGA component and those assembled on PCBs is paramount owing to their primary benefits of high I/O pins. It is highly possible to construct and constrict up to 600 pin counts to a relatively minor area due to miniaturisation of electronic products currently ongoing.

However, the investigation of BGAs solder joint failure is highly challenging to R&D personnel and overall equipment manufacturers (OEM) (Biunno and Barbetta, 1999; Amalu, Ekere and Bhatti, 2009; Otiaba et al., 2011). In an attempt to analyse more advanced approaches employable in describing several BGA failure modes, (Biunno, 1999 & Lee, 2002) used a limited number of analytical tools such as Digital Multimeter (DMM), Scanning Electron Microscope (SEM) and EDS. They identified that apart from creep or solder fatigue deformations, BGA solder joints can fail in four other different ways for example,

- **PCB Pad Damage** (pad lifting) which involves the peeling of the solder pad from its position when shear load is higher than the strength between the pad and the substrate,
- **Ductile Failure**, which exists when the shear quantity is lower than the concentration between the pad and the substrate and is less than the strength between the surface of a solder ball and the face of the pad thereby inducing a fracture around the solder bulk region.
- **Brittle Failure**, which exists when the shear load is higher than the strength between the interfacial interconnection boundaries of the solder joints, and
- **Mixed Failure**, which comprises a combination of the ductile and the brittle failures. It happens when the solder ball is in a transitional situation from plastic deformation (ductility) to brittle failure.

Other typical failure modes for a BGA solder joint included underfilling delamination, heat sink adhesive delamination and die-cracking to substrate failure. It may also involve popcorning effect, a formation of Kirkendall voids in solder joint interface, Printed Wiring Board (PWB) interconnection failure, the rapid and extensive growth of tin whiskers and IMC layers resulting from solid state ageing of solder joints, impact fracture, thermal-mechanical

stresses. However, thermomechanical fatigue is the primary failure mechanism for solder joints (Suhling et al., 2004; Menon, 2010; Popelar, 1997; Tu, 2007).

Failure mechanisms in Sn-Ag-Cu lead-free BGAs, especially the fatigue failures in hand-held consumer electronic products (e.g. computers and mobile phones) have been for decades outlived by microelectronics industry with the help of underfill introduced between the die and the epoxy substrate pads (Tu, 2007; Zeng and Tu, 2002). More concerted efforts are required by R&D engineers and other stakeholders to deal with each of these major problems in solder joint through metallographic preparations and SEM/EDS analysis of the Fractography of the joint's microstructure for the enhancement of product reliability in the field of electronics.

Improving the manufacturing process will be cost effective, and will reduce defects, increase wettability and solderability and minimise cracks in the interconnection boundaries of the solder joints or at the bulk solder. Figure 2.31 shows (a) Crack at the BGA package junction and bulk solder ball, and (b) Crack propagation through a solder bump, and Finite Element Analysis (FEA) image showing stress concentrations in the solder bump.

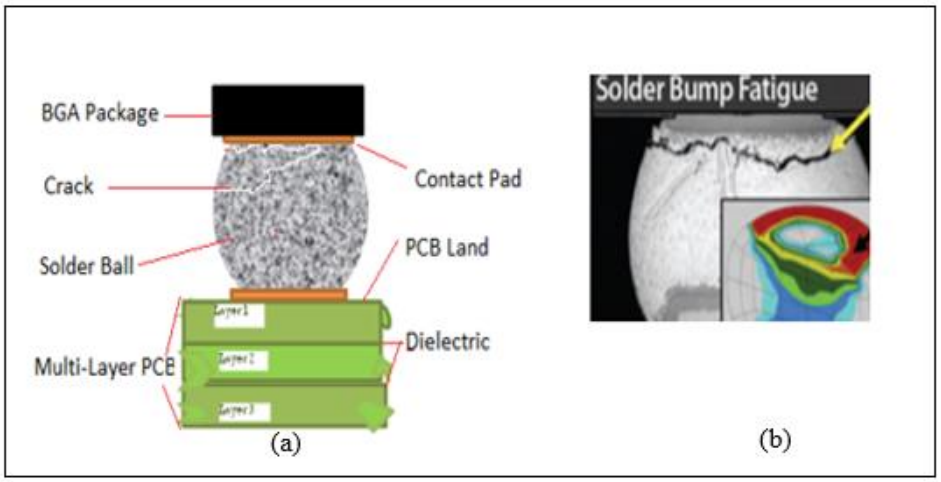


Figure 2.31: (a) Package junction crack, (b) Bulk Solder crack and propagation
Source: ***(Hariharan, 2007; Yao, Qu and Sean X. Wu, 1999; Guo et al., 1991)***

2.7.1 Fracture Surface of Solder Joints

A surface fracture, linked to the failure causes in solder joints is viewed as one of the most significant sources of information. So, the Fractography technology is used to study features that exist on a fractured surface (Quinn, 2012; Quinn et al., 2012). A fracture surface shows

four primary fracture modes as illustrated in Figure 2.32 describes dimple rupture, cleavage, fatigue, and de-cohesive rupture or intergranular fracture surface (Chan, So and Lai, 1998).

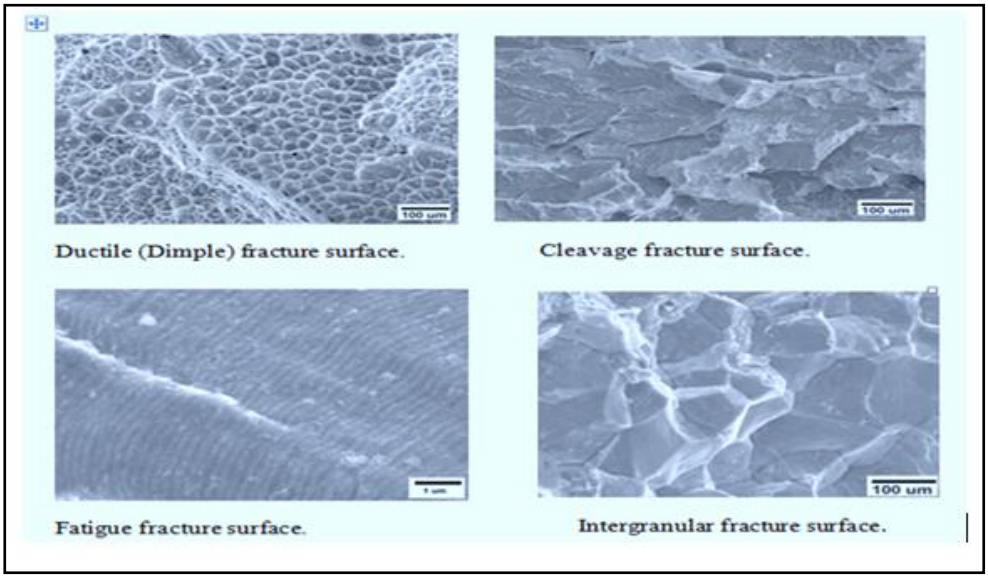


Figure 2.32: Images illustrating the various failure mechanisms

Source: (Quinn et al., 2012)

2.7.2 Strength of Solder Joint

In other to find out the power of a solder joint, it is necessary to fracture it first by applying stress at a particular strain rate, and the type of fracture it has gone through after sharing can thus be analysed. Shear force to implement a given 'Stress' varies with the strain rate; the larger the strain rate, the smaller the latter will be since this is relying on the fracture which is taking place at the cleavage. Theoretically, in the same environment at low strain rates, a ductile fracture is typically observed; but with an increased strain rate, brittle fracture is observable. However, solder joints elastically deform when sheared at low strain rates, and it breaks instantly without going much into elastic deformation when the strain rate is high (Kanekawa, 2005). The claim on strain rate behaviour serves as part of the experimental work for investigation in this thesis. Nevertheless, an inference from literature showed that strength of the joint at lower strain rate also depends on the solder, owing to the ductile behaviour observed in the fracture mode, originating from the ductility in the alloy itself. At high strain rates, however, brittleness was noted in the overall fracture due to the presence of IMC layer which is itself brittle (Johnson et al., 2004). It is confident that the marked shifts observed in the

dynamic shear strength come from the changes in the microstructure of the solder and thickness of intermetallic layer formation in the joint. Figure 2.33 presents the chart showing the effective solder joint strength as controlled by the bulk solder shear strength at low strain rates and by the effect of intermetallic layer strength at high strain rates (Yazzie et al., 2012).

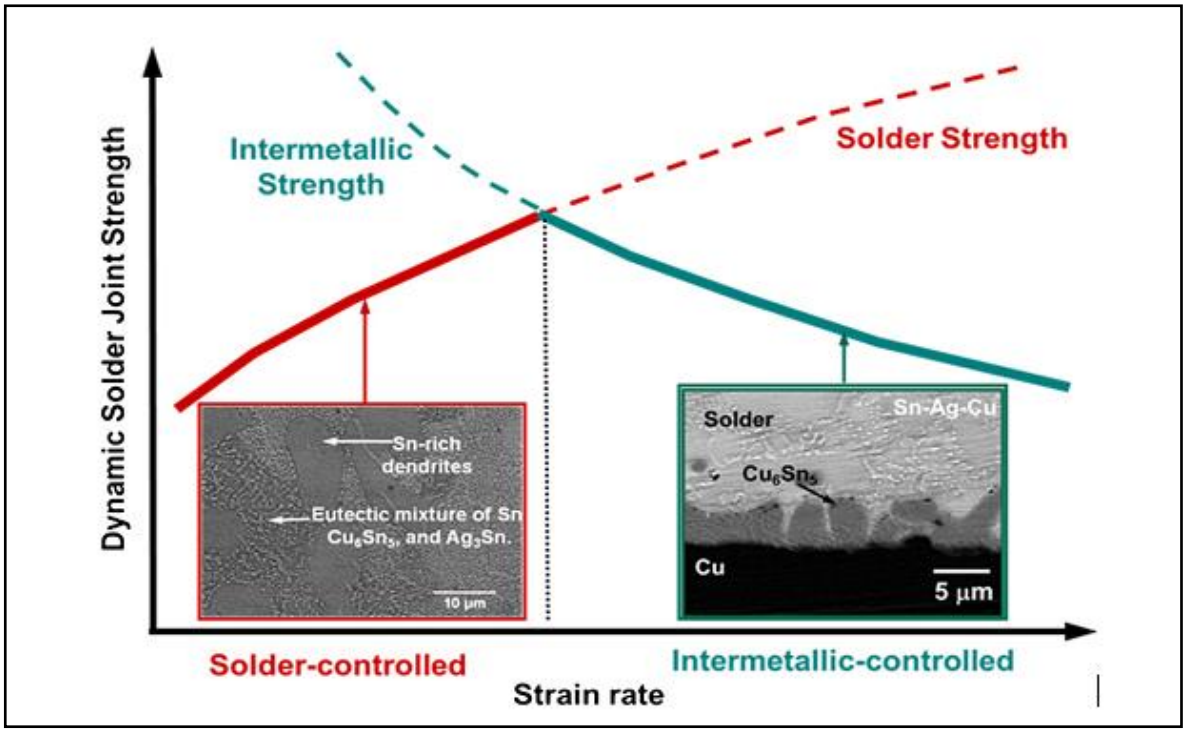


Figure 2.33: Chart of IMC and dynamic solder joint strength vs. strain rate

Source: (Kanekawa, 2005; K. E Yazzie et al., 2012; An & Qin, 2014; K. E. Yazzie et al., 2012)

In the paragraph mentioned above, popular opinion held that IMC layer was responsible for the brittle fracture in solder joints at high strain rates, whereas at low strain rates solder paste is liable for the ductile fracture. The claim is not just because IMC layer has higher Young's Modulus than the solder; it is more because of the bonding, which joins the constituent elements of IMC layer. The bonding responsible for giving IMC layer its brittle characteristic is 'metallic bonding'. The metallic bond forms between metals at high reflow temperatures when metals share their electrons to complete their outer orbits and form bonds. In solder rich regions, metallic bonding is visible but bonds form only between atoms of one element which is the solder metal and comparatively it is not as strong as the IMC layer which forms by sharing of electrons between two or three metals during metallisation process. The behaviour

of these metals and their alloys in the microstructure of solder joints is obtainable from their phase diagrams and is thus imperative for reliability purposes and assessment.

2.7.3 Previous Studies on Microstructure of SnAgCu Lead-free Solder Alloy

The microstructure of SnAgCu (SAC) lead-free solder alloy is of tin-rich dendrites structure comprising of Ag_6Sn_5 and Ag_3Sn IMCs which are found located in various regions of the metal plate or solder joint.The location of these IMCs is usually at the Sn-grain boundaries; the later usually observed as large plates or voids at the interfacial intermetallic. Like the alloying system, the solids of the solder joints are not continuous media, but they are rather micro-composite materials possessing complex microstructures of which their deformation process can only be predictive and observed at microscopic levels. The microstructures of the binary eutectic solder composition stand for the low phase bonding. An approximated value of 95.5Sn-3.8Ag-0.7Cu and 95.5Sn-4.0Ag-0.5Cu (wt. %) have gained popularity in the industry and are widely acceptable. This candidate alloy constituted part of the alloying materials used in this research and, though the exact ternary system of these alloys is yet unknown. For this reason more concerted research efforts have been prompted with more publications from (Yazzie et al., 2012; Shekhter et al., 2004; Pecht, M. and Anupam, C., 2007); and Borgesen et al., 2012). A sound knowledge of the phase equilibria of solder/alloy and solder/substrate interface systems provides the basic roadmap, which may help to the initial selection of candidate solder and also may contribute to the understanding of solder wetting and spread mechanism. The phase diagram for the SnAgCu solder alloy and the near eutectic point magnification liquidus surface shaded with suitable freezing ranges in the Sn-rich region are shown in Figures 2.34 and 2.35 respectively.

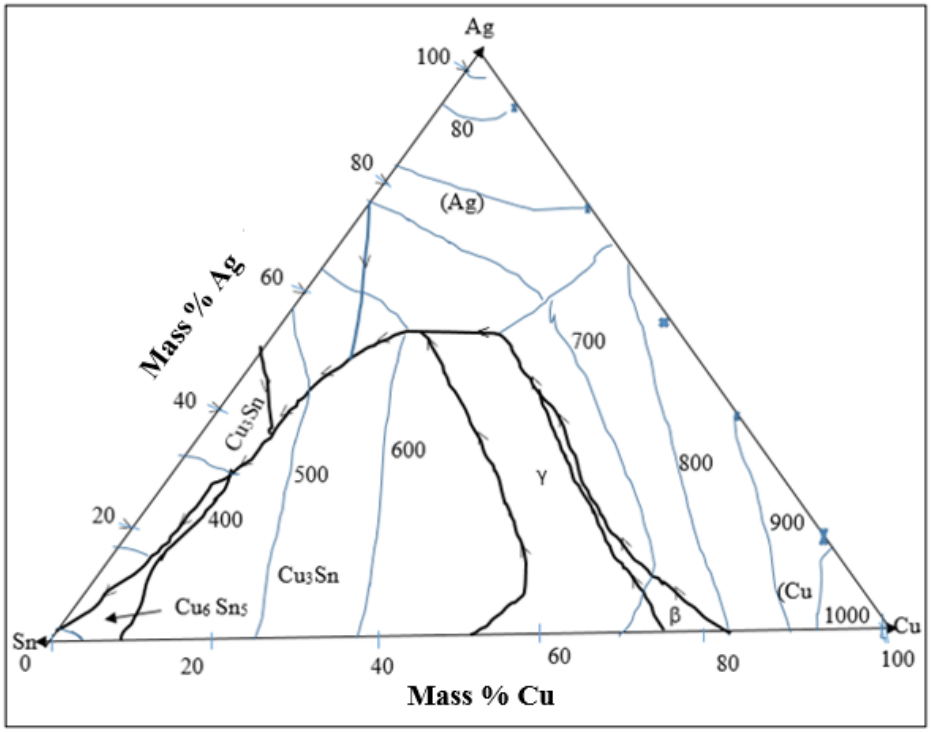


Figure 2.34: Phase diagram for liquidus projection of the SnAgCu Alloy system

Source: (Moon et al., 2000)

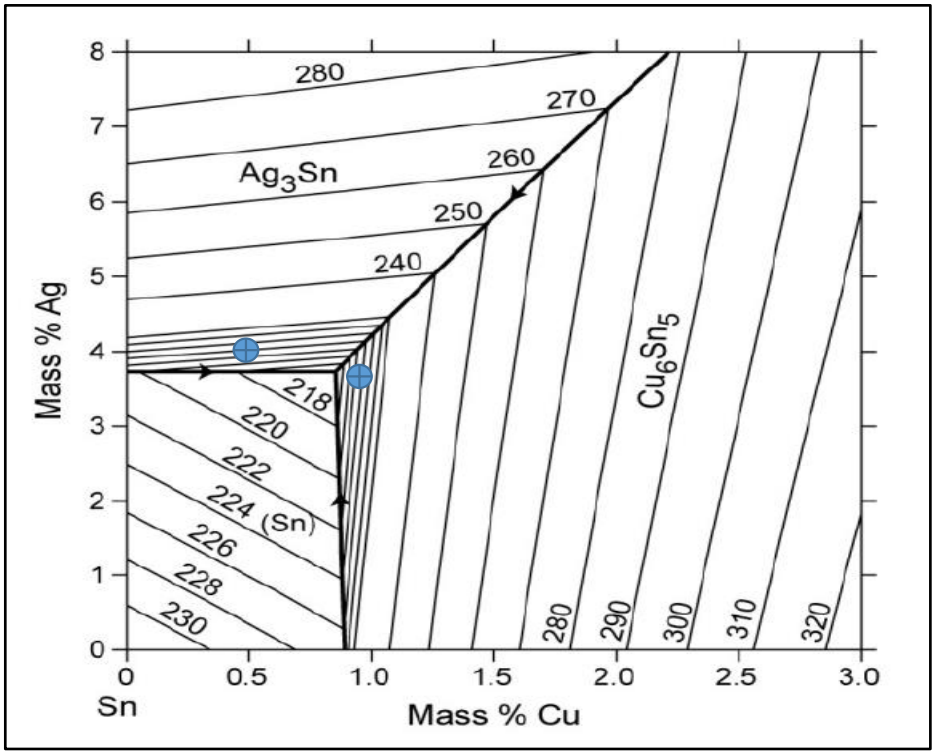


Figure 2.35: Phase of magnified liquidus surface in the Sn-rich corner

Source: (Moon et al., 2000)

The report of an experiment conducted by Gebhardt and Petzow in 1959 (Moon et al., 2000), showed no initial report of ternary phases by anyone and that solid phases have fairly small ternary homogeneity ranges than the tin-rich corner which was first reported to be non-eutectic. However, a more recent work by (Moon et al., 2000) showed that the invariant reaction is eutectic with a temperature of 217 ± 0.2°C, whose liquid decomposes into (Sn) and to binary intermediate compounds of Ag3Sn and Cu_6Sn_5. Although there was disagreement on the composition of the liquid phase at the eutectic temperature and the authors further confirmed this as xAg, = 0.035 and xCu = 0.009. During soldering of the Pb-free SnAgCu solder paste joint, contrary to Sn-Pb phenomena, a small variation in Ag or Cu can tremendously alter the melting point and the solder paste range used to some extent as seen in Figures 2.29 and 2.30. For this purpose, the careful control of Ag and Cu becomes evident to avoid unwarranted growth of impurities such as tin whiskers.

Notably, Sn remains an inclusive element in SnAgCu solder alloy to boosts the formation and growth of intermetallic in the Sn or Cu base metals. On the other hand, Ag and Cu enhance the physical property of the metallic bond for mechanical and electrical connectivity that proactively improves the reliability of the solder joint. There is no doubt that the microstructure of SnAgCu phase equilibria data would provide not only information about the liquidus and solidus temperatures of a candidate solder alloy; but also information about possible phase formation and transformation above liquidus temperature from β-tin to α-tin intermetallic. The phase reaction happens either within the solder during solidification or in response to the substrate material by a combination of isothermal solidification and solid-state reaction. Nevertheless, the phase diagram analysis of SnAgCu solder alloy microstructure into binary, ternary, quaternary or higher component systems is not within the scope of this study. However, it is crucial in assessing the long-term durability of a solder joint about its device integrity and reliability which will benefit the electronic manufacturing industries and the niche market.

2.7.4 Previous Studies on Intermetallic Compound Formation

Intermetallic is interfacial reaction products between the solder and the substrate pad interface. Intermetallic compounds are the chemical reaction products formed between the base metal and the solder components during the reflow soldering process (Ning-Cheng, 2002; E H Amalu, Lui et al., 2011). When the formation of the transition region brings into contact metals, which have a chemical affinity, they can react and form compounds called IMCs. Such

compounds distinguished themselves from alloys because they have a fixed stoichiometric composition whereas the composition of an alloy changes within a small range without significant change of the crystal structure. The formation of intermetallic can be faster if the base metal is soluble in the liquid filler. A solder joint with an intermetallic layer formation signifies a solid bond, and an investigation of the chemical composition across the joint by the electro-microbe can show a region of fixed structure between the base metals and the solder alloy.

However, IMC layer formation is characteristic of copper (Cu) base metal pads and tin (Sn) base solder alloys formed from the action of molten tin on copper at reflow and ageing temperatures (Glenn et al., 2006; Tsai, 2012). Also, they observed that IMC layer forms both the mechanical and electrical flow of the solder joint and serves as its integral part. Clearly, and because the nature of the IMC thickness affects the reliability of the solder joint. Apart from its electrical integrity to the joint, IMC has higher strength than the solder and assures for good bonding between the solder and the substrate.

In another study conducted by (Alam et al., 2007), the ball shear test is the most preferred test methods used to carry out the reliability of solder bond strength for ball grid array packages. They further described it as an attempt to determine the mechanical robustness of the solder joint to show the relationship between the shear behaviour and the products interfacial reaction. As further gathered in their experimental findings through Finite Element Analysis (FEA), the IMC formation at the solder interface plays a significant role in the BGA solder bond strength and fatigue life. In Figure 2.36, the greyish part marked in between Cu and the bulk solder with Cu_6Sn_5 shows the intermetallic layer. It is clearly visible that the layer forms on the surface of the substrate and this proves the point that electricity conducts through the IMC layer by the component. Table 2.7 presents the common base metals of solder with their constituents and solubility intensity.

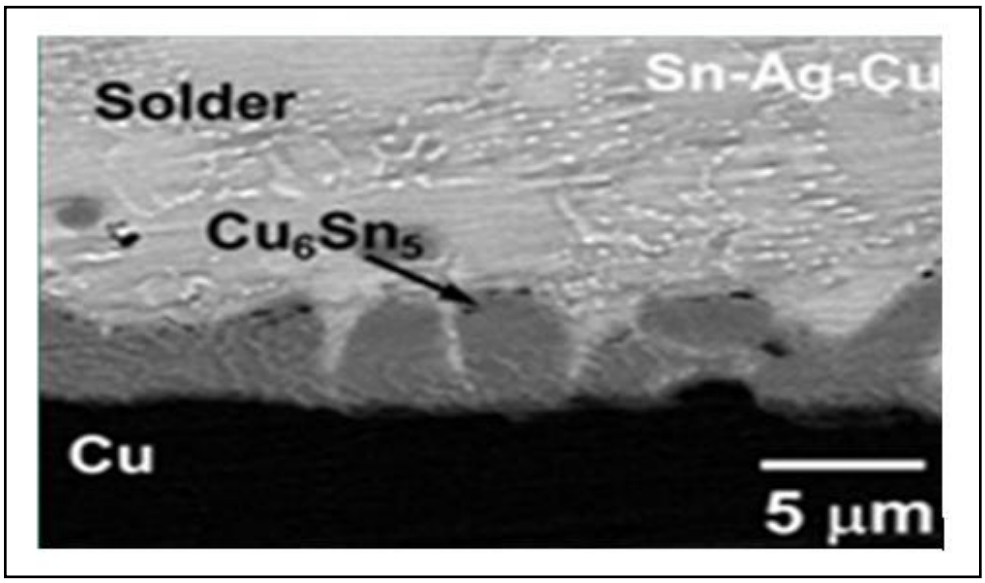


Figure 2.36: Micrograph of SnAgCu solder joint with Cu_6Sn_5 intermetallic
Source: (Glenn et al., 2006)

Table 2.7: Major IMC Base Metals and Tin-based Solder Alloys
Source: (Leonida and Leonida, 1981).

Base Metal	Intermetallic Compounds with Tin (Sn)	Solubility
Aluminium (Al)	None	None
Antimony (Sb)	SbSn	Fair
Arsenic (As)	None	Low
Bismuth (Bi)	None	Fair
Cadmium (Cd)	Intermediate phase which decomposes below the melting of solder	Low
Copper (Cu)	Cu_3Sn; Cu_6Sn_5	High
Gold (Au)	AuSn; $AuSn_2$; $AuSn_4$	High
Indium (In)	In_2Sn; $InSn_4$	Fair
Iron (Fe)	Fe_3Sn; Fe_2Sn	None
Magnesium (Mg)	Mg_2Sn	Very low
Nickel (Ni)	Ni_4Sn; Ni_3Sn; Ni_3Sn_2; Ni_3Sn_4	Very low
Silver (Ag)	Ag_6Sn; Ag_3Sn	High
Zinc (Zn)	None	Fair

Also, (Kim, Huh and Suganuma, 2003) pointed out that the thicker the IMC layer, the lower the joint integrity between the solder component and the base metal. Despite having such immense importance, IMC layer still carries the biggest threat to the reliability of a solder joint, and this is due to its brittleness formed as a result of its enhanced crystal structure. The

brittleness in the crystalline layer of a solder joint is capable of continuous growth with an associated volume increase during the working period of the component. Device layers with high brittle intensities at their service conditions are prone to weaker solder joints as their IMC layer becomes thicker than those with tensile properties. It means that solder joint, overall, could wear out and become more prone to fracture if the environment in which the component is operating is not suitable. However, it is an essential criterion to control the IMC layer growth; conditions for this pre-planning must be before the design of the electronic assembly package. Factors which encourage IMC growth have been analysed in several studies (White, 2008; Guerrier et al., 2000). In their study, (Amalu and N. N. Ekere, 2012) discussed that electronics solder joints exposed to lengthy high thermal energy would continually experience IMC growth. This increase occurs because of the continuous reaction between the material properties of the solder alloy and the copper bond pad.

There is a further necessity, however, to understand the intermetallic formation, structure and its impact on the reliability of solder joints in lead-free BGA assemblies. If intermetallic grows to sufficient thickness, the fracture can occur during handling, shipping or service. The growth rate of intermetallic compounds indicates no significant differences due to the paste metallurgy, the ball metallurgy or the peak temperature of the reflow process (Ning-Cheng, 2002; E H Amalu and Lui et al., 2011). The cause of the decline observed in the shear strength of the solder ball was primarily by the formation of IMC layers, together with the microstructure coarsening. The failure mode was found to have gradually changed during the ageing process from a ductile rupture in the solder to brittle fracture at the interface between the solder and IMC; and between two intermetallic compound layers (Lee et al., 2002).

According to (Toh et al., 2007), BGA pad finishes and solder composition are some of the many factors that can influence intermetallic compound formation at the interface. The IMC growth controls the strength of BGA solder joint. From their report, the formation of excessive brittle intermetallic and weak interfaces can result in solder joint reliability issue leading to the BGA package failure. The growth of Kirkendall voids and IMC significantly weaken the SJs interface during the thermal cycle. Pang, 2006 observed that drop impact crack location switched from the inside of IMC toward the IMC/Cu interface, and this phenomenon is likely, linked to Kirkendall void formation. The intermetallic compound growth, as well as the crack formation subject to isothermal and thermal cycling ageing, was responsible for the long-term solder joint reliability performance (Pang, 2006).

In a report delivered by (Chiu et al., 2004), the Kirkendall voiding at the Cu to Cu_3Sn interface was the primary mechanism for solder joint strength degradation under thermal ageing. There was no significant variation observed in the shear strength as the ageing time increased. Theoretically, at the local equilibrium solubility, IMC starts to form at the interface between the pad and the solder. This bonding process highly intensified under increased ambient temperatures on the solder joint resulted in the growth of unwanted intermetallic compounds. The presence of IMC weakens the solder joint strength because of their weak and brittle nature. IMC thickness also has a strong influence on the solder ball strength. Increasing the storage temperature and dwell time leads to increasing the IMC layer thickness. Conversely, the ball shear strength observed to decrease with increasing thickness of the IMC layer. After significant ageing, the IMC layer grew, and the interface between the IMC layer and the bulk solder became smooth. However, an adhesive strength came mostly from the bonding strength of the IMC/solder interface which might significantly influence the integrity of solder balls in BGA packages (Yoon, Kim and Jung, 2004).

In a research carried out by (Chan et al., 2001), the result of the experiment shows that the formation of the Ni_3Sn_4 intermetallic compound during soldering process provides a good metallisation and bond between the solder and the substrate which tends to affect the solder joint strength thereby resulting in mechanical failure. Following their observation on the relationship between the solder bond fatigue with nickel-tin intermetallic compound thickness and the heating condition, optimising the reflow profile is recommended. It would help to maintain and control with caution, the soldering performance. However, (Shin, 2000 and Alam et al., 2007) examined in their research work the shear strength of BGA solder joint on the impact of IMC layer thickness formed between the Sn-Cu solder balls interfaces and Cu bond pads. In their investigation, they found that the copper-containing solder alloy help to stimulate the growth of IMC layers as well as the interface roughness between the IMC layers and solder joint during the process of soldering. Hence, the shear strength of the solder ball joint is dependent on the IMC layer thickness.

Thus, it is an essential criterion to control the IMC layer growth; conditions for this requires pre-planning before the design of the electronic assembly package. Factors which encourage IMC growth have been analysed in several studies (White, 2008; Guerrier et al., 2000). In their study, (Amalu and N. N. Ekere, 2012) discussed that electronics solder joints exposed to lengthy high thermal energy would continually experience IMC growth. This increase occurs

because of the continuous reaction between the material properties of the solder alloy and the copper bond pad. An image of IMC layer shown in Figure 2.37 (a) indicates that IMCs at the interface of the copper bond pad and a Sn-4Ag-0.5Cu ball after 32 days of ageing at 150^0C are obtainable experimentally, and analysable through micrographic examination using SEM/EDS. Figure 2.37 (b) presents for clearer vision, a magnified view of the IMC.

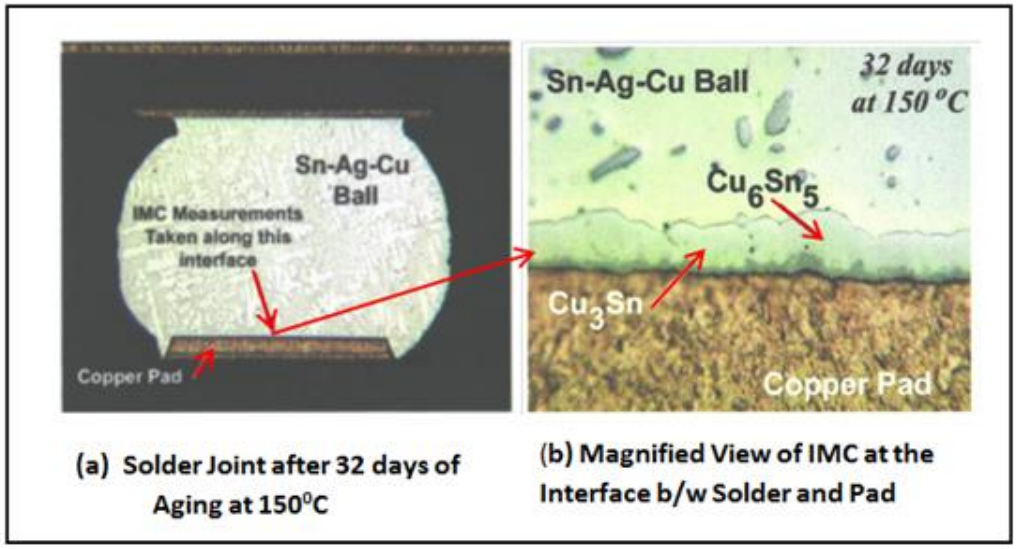


Figure 2.37: (a) Solder Joint after ageing. (b) Magnified view of IMC

Source: (Roubaud et al., 2001)

2.7.5 Factors Affecting IMC Layer

2.7.5.1 Temperature

Temperature is one major part of the environment, which has the greatest impact on the growth of IMC layer. It is Preferred, to kept the temperature of the environment where components operate lower because IMC layer grows rapidly when the temperature is high. There is Low-temperature prescription because of more metallic bonds which form between the metals at high temperature and hence making the IMC layer thicker. Thus higher temperature in general increases brittleness in the solder joint and makes it weaker (Barajas et al., 2008). The verification of this instance in this experimental work was by noting down the shear forces for aged and non-aged samples for comparison. Moreover, as projected, the shear force to cause a fracture in the non-aged sample would be comparatively higher than the shear force causing a

fracture in the thermally aged samples. A schematic presentation of the relationship between IMC layer thickness in micrometre and ageing time in seconds is in Figure 2.38.

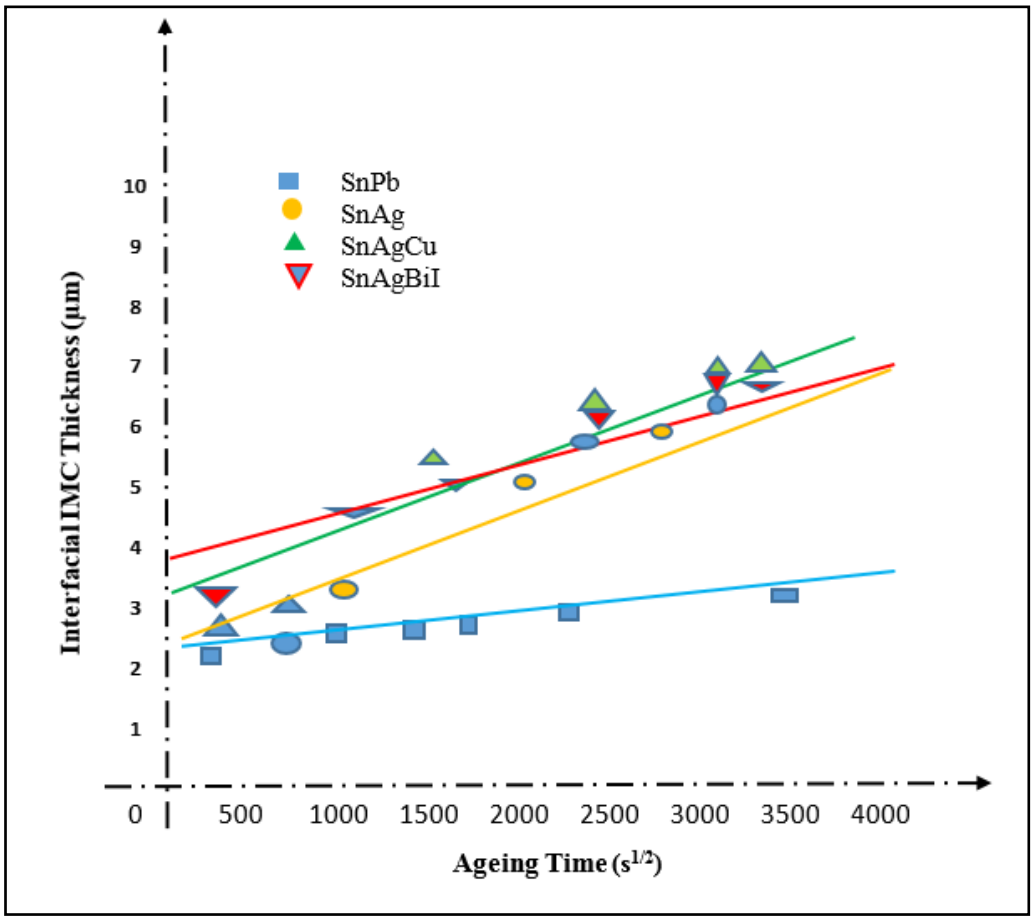


Figure 2.38: Graph of Interfacial IMC thickness and ageing time at 150^0C

Source: (Benini and Giovanni, 2002; Yoon, Chun and Jung, 2008)

2.7.5.2 Surface Finish

Sometimes 'Surface Finishes' help to increase the durability of a substrate. Finishing done with a less reactive metal would help to save the substrate from corrosion. Due to the presence of another material, the IMC layer forms between the solder and finishing material itself and this is because the copper pad on the substrate or the substrate itself never gets the chance to react with the solder to form the IMC layer. In their study, (Benini and Giovanni, 2002; Yoon, Kim and Jung, 2004) carried out an experimental study to find the effect of isothermal ageing on the interfacial reactions between solder and substrate. Sn-0.4Cu solder and two substrates were

used, one of the substrates is uncoated Cu, and the other is Cu coated with Electroless nickel immersion gold (ENIG). In the case of Cu substrate, two intermetallic compounds (Cu_6Sn_5 and Cu_3Sn) produced at 150°C and 250h ageing exhibited no cracking in the joint. At 150°C and 1000hr, a crack showed in the interface between the Cu_3Sn intermetallic compound and Cu substrate. In the case of (ENIG) substrate, at 150°C and 24h ageing, a duplex structure of $(Cu\text{-}Ni)_{6}\text{-}S_{n5}$ and $(Ni\text{-}Cu)_3Sn_4$ appeared at solder/ENIG interface (Benini and Giovanni, 2002; Mallik, Ekere et al., 2008). Because the aim of this experiment was to analyse the effects of isothermal ageing, it is thus imperative to use two different substrates, one with the coating and the other one without it, which would reveal clearly the effect of surface finish when observed with SEM. However, the authors confirmed that if the substrate has a finishing material on it, then the IMC layer will form between the finishing materials and the solder bump to produce the metallic bonding called solder joint, with strength, which depends solely on the surface finish used.

2.7.5.3 Solder Volume

Many studies exist to review if the solder volume affects the formation of IMC layer in any way or not. It was in expectation that significant amount of solder would result in excessive formation of the IMC layer, but results analysis showed that the volume does affect the formation and growth of IMC layer but not as much as the surface finish and environmental temperature (Meyyappan, 2004). However, Amalu et al. (IPC/JPCA, 2000) stated that the thickness of the IMC layer at the solder/Cu joint's interface increases with decreasing standoff height for as-reflowed solder joints. The resulting effect may have been from molten solder splatter caused by heat convection and electro-migration during reflow soldering or thermal ageing.

2.7.5.4 Solderability

Solderability in electronics manufacturing is the tendency of a surface to form a good joint when connected to another surface using a soldering process. It provides an indication of how to make a good joint easily if the operational parameters are appropriate. Solderability and Reliability of printed electronics were studied by (Salam, B., Lok, B. K., 2008) using two types of printed conductors to determine their effects. The metal particles of the studied printed

conductors consist of a 6 x 25 mm FR4 coupon test vehicle made from copper and silver surface finish pads and bound with phenol resin. Test results revealed that printed boards with silver surface finishes leached severely indicating poor solderability and the wetting balance test on printed copper board studied also indicated poor solderability. However, the surface roughness measurement with microstructure observation confirmed that the poor solderability of printed copper was due to its surface roughness and heterogeneity (mixed copper and void) which universally affected the reliability of the bonded outer metal particles of the printed interconnects. They also discovered that the IMC layers of the aged printed interconnects were thicker than those of the as-soldered samples were.

In general, "A reliable solder connection must have a solderable surface to form a good metallurgical bond between the solder and the joining components. An understanding of the phenomena of metallurgical bonding may require proper grasping of soldering principle. According to (Prasad, Ray 1989), it requires knowledge of "phase diagrams, the concept of leaching, surface finish (already discussed in section 2.7.5.2), wetting, and oxidation of metallic surfaces" some of which will not be discussed here for the purpose of the research scope.

2.7.5.5 Wettability

Wettability is the ability of a liquid to wet a surface with which it is in contact. During reflow soldering, the wettability allows the wetting of a base metal by the molten solder. If the liquid solder does not wet a surface, the surface would be difficult to solder, as the wettability of a surface is the essential ingredient or qualification for its solderability. The qualification and acceptability of a component solder joint package demands an existence of a no non-wetted or de-wetted surface area. However, the electronic component and manufacturing industries have settled on an allowable maximum of 5 to 10% non-coverage, hence achieving a 100% wetting is a difficult task for the suppliers.

From the expression given by (Jiang et al., 2007 and Ožvold et al., 2008), and for all types of solder alloy compositions used in the packaging of electronics components, wettability is the ratio of wetting angle and the size of wetted surfaces. On the other hand, the size can be relatively be quantified from the observed contact angles and from practical indications. A simple methodology to account for the influence of the different rough surface on wetting and

contact angle measurements may be required during processing. More significantly, surface properties influence wettability in correlation with solder alloy proportion. Wettability is, therefore, a surface phenomenon involving only a few atomic layers at the surface of the wetted solid. It is also influenced, to a large extent by the presence of small traces of contaminants. Wetting according to Ray Prasad (1997) begins as soon as solder specimen on a test vehicle or in a solder bath heats to activate the flux chemistry, which causes the slope of the curve to move upstream, and flattens as wetting continues until its exit. The time it takes to reach the maximum force at F2 or maximum wetting distance defines the wetting time, which by industry standard is less than 1 and 2.5 seconds to reach T_0 and F_1 respectively. Figure 2.39 provides a typical wetting force curve generated by a wetting balance test. The contour of the meniscus follows a mathematical law, described and calculated by Wassink, Klein R. J. (1994). However, the calculation of the total wetting force is by subtracting the buoyancy force (exerted by the displaced solder from the immersed substrate volume) from the surface tension force as given in Eq. 2.5.

$$F_W = P\gamma_{LF}Cos\theta_C - \rho gV \tag{2.5}$$

, where:

F_W = *the* wetting force,

P = *the* perimeter of the submerged substrate,

γ_{LF} = the solder surface tension in contact with flux,

θ_C = the contact angle of bumped solder joint

ρ = density of the solder

g = the acceleration due to gravity and

V = the volume of the immersed substrate

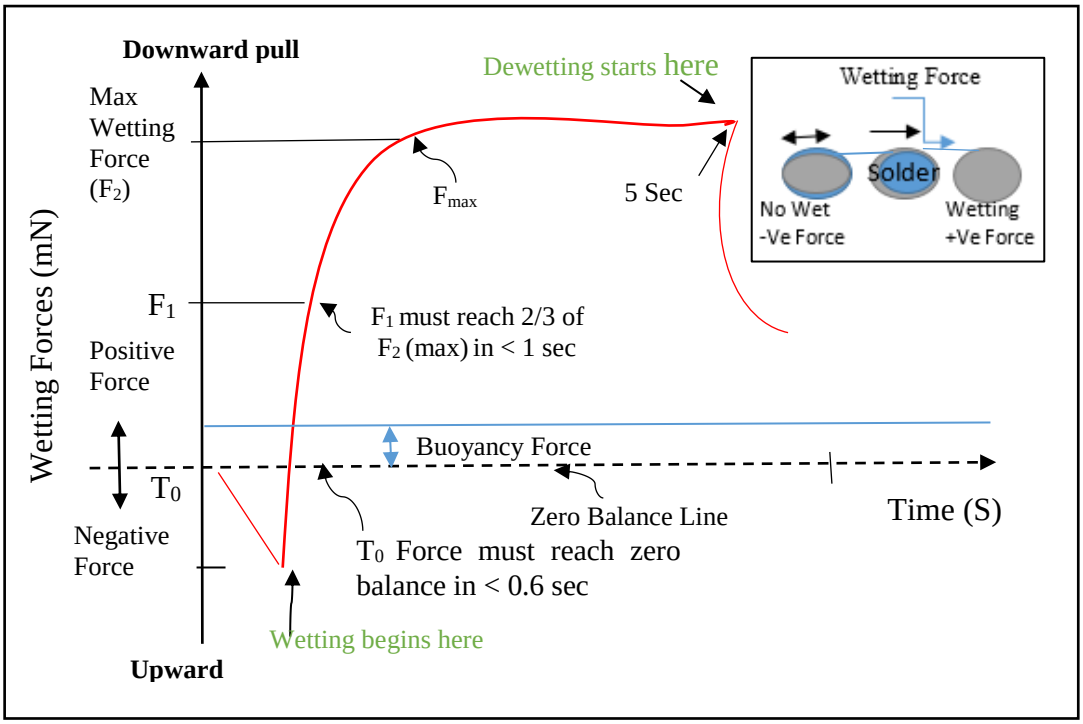


Figure 2.39: Standard IPC-S-805 wetting force balance curve as a function of time.

Source: (Prasad, Ray, 1989)

The wettability of a clean surface by molten solder mainly depends on:

- The nature of the base metal and the solder.
- The temperature of the base metal and the solder.
- The surface tension of the solder, which is temperature dependent.
- The roughness of the surface (on a microscopic scale).
- The mutual diffusion of atoms of the base metal and the solder contact angle (θ), with a possible formation of intermetallic compounds.

In reflow soldering, each base metal and solder combinations used in a test piece, has a critical temperature profile below which wetting does not occur or takes place only to a slight extent. In most cases, this temperature is 20^0C to 50^0C higher than the melting point of the solder used (G. Leonida, 1981). During paste formulation, the use of flux activators and oxide removers would help to ease wettability. However, the use of solder oxide remover and flux activators can significantly improve the electrical properties of solder joints interconnect assemblies. Flux activators are chemicals such as resin, water-soluble bases, and isopropanol alcohol. They are usually added to solder fluxes to remove oxides from metal surfaces, improve wettability, and

thereby to allow them to join with flux residues as shown in Figure 2.40 to form solder joints of strong metallurgical bonds (Mackie, 2009).

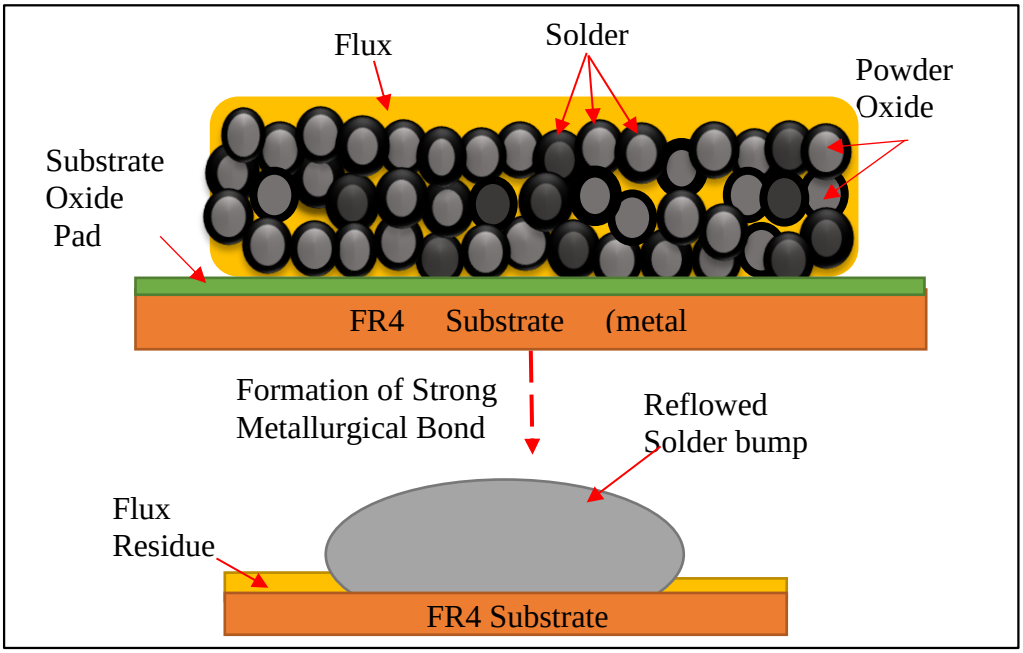


Figure 2.40: Wettability of solder paste and formulation of a strong metallurgical bond

Source: ((Mackie, Andy C. 2009)

2.7.6 Previous Studies on Solder Joints' Component Standoff Height

CSH is a term used in surface mount technology to describe the distance between the top of the substrate (PCB) and the bottom of a surface mount component mounted on it (Glenn et al., 2006). However, experimental findings from (Blish, Natekar and Devices, 2002; Njoku, Mallik, Bhatti, Amalu, et al., 2015) described CSH of a solder bump as the distance between the material interfaces as shown in Figures 1.2 and 3.14. Also, (Clech, 1996) reported that the design parameters with the greatest impact on BGA assembly reliability are pad diameter, laminate thickness, die size and thickness, and solder joint height; and that there is little effect from solder paste or flux, board finish and the assembly processes.

The results of research works by (Amalu and N.N. Ekere, 2012; Amalu and Ndy N. Ekere, 2012) indicate that the thickness of the IMC layer at the solder/Cu interface of a BGA solder joint after reflow soldering increases with decreasing standoff height. The authors stated that the shear strength of the joints strongly depends on the standoff height, solder volume, and pad

size. Nevertheless, the fracture mode of the joint could change from a location near the interface gradually to the middle of the solder matrix as the standoff height of the joint decreases (Xun-ping et al., 2010). A schematic showing the Flip Chip SJs model with the interconnection boundaries and other constituent parts is in Figure 2.41as provided.

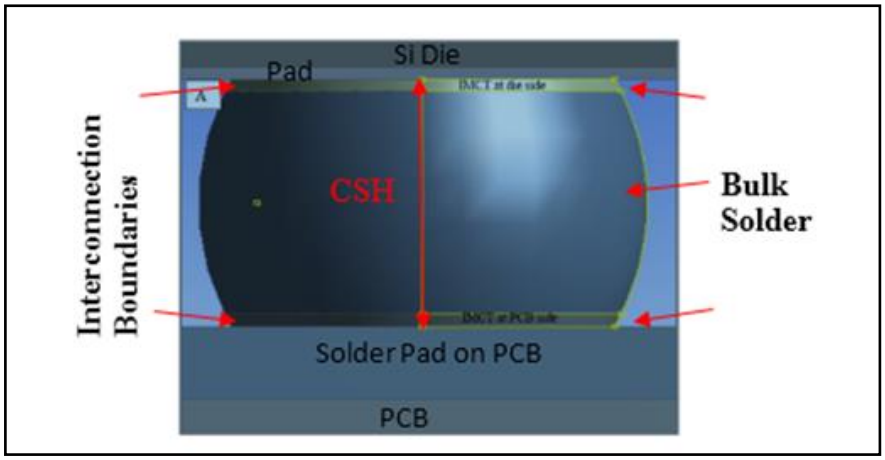


Figure 2.41: Model of Solder Joint CSH, Interconnections and other parts

Source: *(Amalu and N.N. Ekere, 2012; Amalu and Ndy N. Ekere, 2012)*

Numerical simulation was the method adopted by (Lo and Lee, 2008) with the aid of 'Surface Evolver' to predict the solder joint geometry where the simulation and the experimental results conform to each other. They also used numerical simulation for different bond pad geometries to calculate the maximum and minimum standoff heights. However, solder joint reliability depends on the thermal- mechanical behaviour of the solder, the geometry of the solder ball, the material of the package, and a higher standoff height of the solder ball which provides better reliability characteristics for an area array package under the same configuration (Shin, 2000). Their results showed clearly that a solder joint with higher standoff has the highest fatigue lifetime, while low standoff solder joint has the lowest fatigue life prediction. The authors concluded from their experimental results that the crack propagation time of SJs is determined mainly by their standoff height (Liu and Lu, 2003).

The microstructure and composition of SJs change significantly with reducing Component Standoff Height (CSH). These changes tend to affect the mechanical properties and application reliability of SJs ultimately. At reduced standoff height, the ultimate tensile strength of SJs decreases, with a fracture mode transition from ductile to brittle nature (Wu, Zhang and Mao,

2009; Jang and Greer, 2010). The effect of standoff height on the microstructure and tensile strength of individual solder joints with given standoff heights was studied. Also, (Jang and Greer, 2010) reported that the proportion of IMC thickness to standoff height increases with decreasing standoff height which will have an adverse impact on the reliability of solder joints.

A report from (Ladani and Razmi, 2009; Wu et al., 2009; Peng and Marques, 2007) also revealed that the BGA solder joint reliability increases with decreasing PCB pad size. Their research work also confirmed that increasing the solder joint standoff height could increase the solder joint reliability of the BGA package. The effects of Component Standoff Height (CSH) controlled by the relationship between the diameter of PCB bond pad and diameter of die bond pad on the high-temperature reliability of flip chip lead-free solder joint was studied using the Finite Element Method (FEM) tool. The survey conclusion shows that the reliability of a solder joint in flip chip assembly decreases as CSH decreases. That low CSH promotes fatigue cracks at interconnects between IMC at the die side and solder region and that the reliability of solder joints operating at elevated temperatures is dependent on CSH, the thickness of IMC and solder volume (Amalu and N.N. Ekere, 2012; Amalu and Ndy N. Ekere, 2012). However, the authors noted that the shear strength of solder joints is affected, not only by CSH but also by the wettability factor of the solder balls and the contact angles/areas between the solder ball and the substrate's bond pad diameter.

2.7.6.1 Effects of solder ball curvature in connection with contact angle and CSH

In electronic packaging and component assembly, the curvature of the solder balls is crucial in determining the bond pad diameter and height of the solder joint because of its affiliation with the contact angles between solder and substrate, used in characterising the quality of the joint's interconnection. (See Figure 2.42). However, a small contact angle entails a suitable wetting lattice by the solder alloy, which usually results in a mechanically reliable interconnection and vis-à-vis the bonding interface. Wetting begins at an angle below 0^0 while de-wetting which suggests poor contact strength occurs at an angle above 90^0.

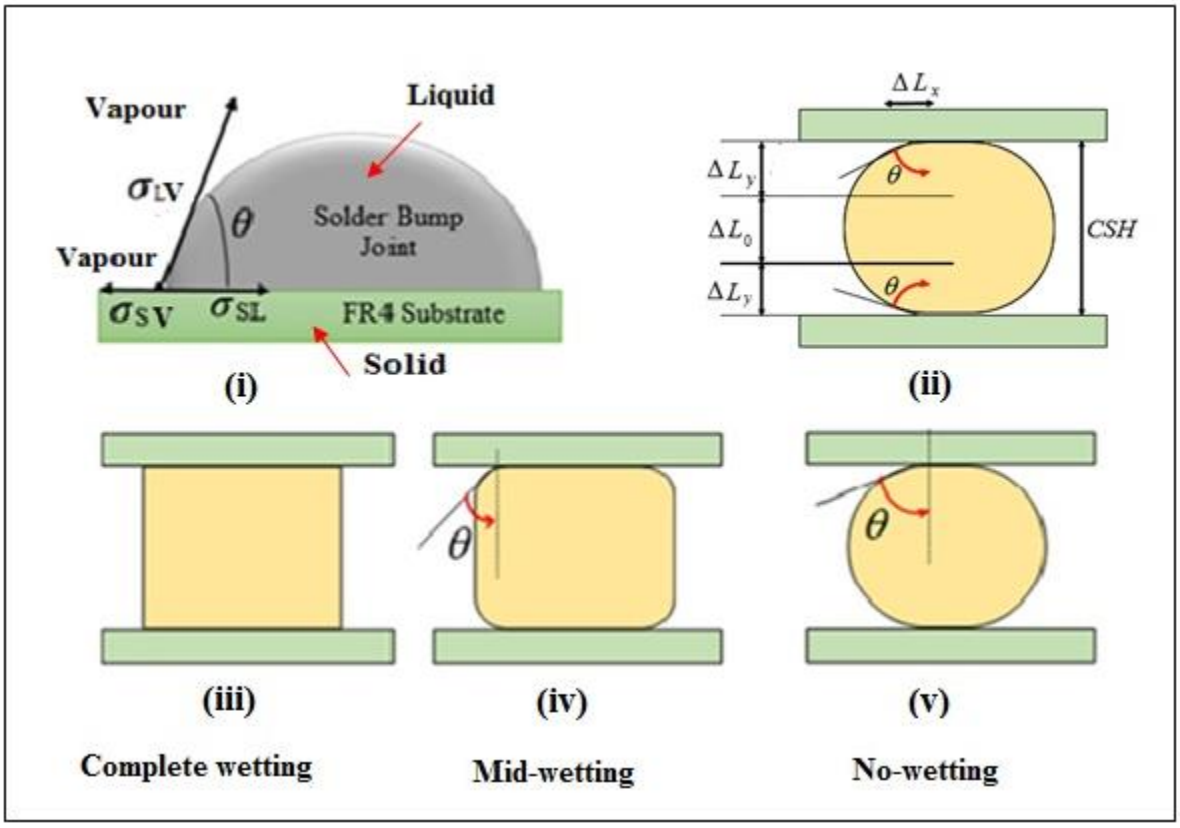


Figure 2.42: Wettability and contact angles of a liquid with related surface tensions

Following the above description and a close look at Figure 2.42 (i), it is imperative to note that the contact angle (θ) at the triple point is determined by the balance between the surface energies (σ_{SV} and σ_{LV}) of the solid (substrate) and the liquid (solder bump alloy) vapour phases; and the interfacial energy, σ_{SL} between the substrate and the liquid solder respectively. By considering Young's equation, which describes this interrelation of the intermediate oxide layer or the mutuality of the bonded interfaces, has a surface tension with a contact angle calculated using Eq.2.3.

$$Cos\ \theta = \frac{\sigma_S - \sigma_{SL}}{\sigma_L} - \tag{2.3}$$

Consequently, and from the balance of forces between the solid and the liquid solder, the surface tension can be resolved using Eq. 2.4:

$$\sigma_{SL} = \sigma_{SV} - \sigma_{LV} Cos\theta \quad (2.4)$$

, where:

σ_{SL}, is the surface tension between the solid and liquid

σ_{SV}, is the surface tension between the solid and vapour phase

σ_{LV}, is the surface tension between the liquid and vapour phase and

θ, is the contact angle of the liquid droplet on the surface of the solid

Equation 2.4 is known as wetting or Young's equation which shows that $0 < 90^0$ and invariably corresponds to $\sigma_{SV} > \sigma_{SL}$, indicating an imbalance in surface tension (surface energy) which provides the driving forces that spread the liquid over the solid surface. Nevertheless, Fig.2.42 (ii) shows the CSH and the curvature of a solder ball with its contact angle both of which influence the wettability and hence the shear strength of the solder joint. The lower the contact angle is, the greater the tendency for the solid to be wetted by the liquid; and the larger the contact angle, the poorer the wettability will be. It implies that for a complete wetting to occur the surface tension of the liquid interface should rather be less or equal to the critical surface tension of the substrate (σ_{SV} - σ_{SL}) during processing.

Thus, a solid surface with complete wetting has a contact angle occurring at $\theta = 0$ and $Cos\theta = 1$ (Duncan et al., 2005). However, if one considers a linear elastic shear response of the solder at small strains, the relationship between shear strength and CSH can be compared. Based on Figure 2.42 (iii), (iv) and (v) above; and by using Eq.2.5, given the shear modulus of the solder ball as G_S, then:

$$\text{Shear stress, } \tau = G_s \gamma \quad \Rightarrow \quad \tau = G_s \frac{\Delta L}{L_o} \quad (2.5)$$

, where *Lo* is the gauge length; which comprises the CSH and projections drawn from the wetting angle.

Also from the Figure 2.42 above, one can distinguish three scenarios from (iii) no-wetting, (iv) mid-wetting and (v) complete wetting of solder joints with the substrate or pads. Based on what

level of wetting, the effect of shear length, *Lo* will be different and the effect of the contact angle will come into the equation thus:

- No wetting: Lo = CSH (independent of contact area).
- Mid-wetting: Contact angle is small.
- Complete wetting: contact angle tends towards infinity (depends on both CSH and contact area).

Thus, the relationship between shear stress (at small strains), gauge length and contact angles becomes:

$$\tau = G_s \gamma \qquad \Rightarrow \qquad \tau = \frac{G_s \Delta L \tan\theta}{\left(2\Delta\, L_x + \Delta\, L_o \tan\theta\right)} \tag{2.6}$$

The implication of Eq. 2.6 is that the shear stress is inversely proportional to CSH and directly proportional to the wetting angle, θ. Therefore, as wetting angle increases, the shear strength should increase while a decrease in CSH will increase the shear strength, τ of the solder joint.

2.8 Long Term Reliability of Lead-free Assembly Solder Joints

2.8.1 Previous Studies on Designs for Accelerated Thermal Cycles

When solder joints assembly on PCBs, are subjected to thermal cycling conditions, information and a statement about their quality after specific periods in the field, will be required for reliability assessment. Due to the nature of occurrence of temperature, cycles in the field, thermal cycling/accelerated ageing used in the investigation of the solder joint long-term reliability. In their research (Chow et al., 2011) discovered that wear-out failure mode causes the thermal mismatch between solder and bump pad during the temperature cycling condition. This failure mode consists of crack in the bulk solder joint, which is close to the package interface (Yin et al., 2010; Liu, 2001).

Nonetheless, to identify the critical solder joint during thermal cycling, all solder bumps are originally designed using elements with identical mesh pattern and refined mesh density at both the top and bottom solder interfaces (Liu, 2001). However, during this temperature cycling test, consequently, when the calculated volume averaged values are over the critical solder layers, the maximum amplitude of creep has a lower bending stiffness with the PCB deformation behaviour, which makes the package more yielding. The component will be permanently damaged when it experiences cyclic stress and strains due to the occurrence of fatigue failures (J. Liu et al., 2011). In FPGAs of BGA packages, solder joints do experience an increasing fatigue damage (Yao, Qu and Sean X. Wu, 1999; J. Liu et al., 2011).

The crack propagated in a solder joint, and materials nucleation induces the rate at which it grows fatigue leading to corrosion and delamination wear (Fleming and Suh, 1977). The crack propagation rate, which, increases with increasing coefficient of friction are also influenced by the change in stress intensity factor and use environment, which is harsh. The cracking mechanisms and the rate of crack growth can be detrimental to the lifetime of the component. Analysis of fracture mechanisms can clearly demonstrate the important role in characterising the behaviour of the joints' crack in some cases where visible cracks form and extend (Stam and Davitt, 2001). The research by (Park and Feger, 2009) studied, showed that the complexity of thermal fatigue experiments is high. The application of chamber heat convection induces thermal fatigue stresses to obtain low- cycle fatigue (da/dN) versus factor plots of the thermal stress intensity. This phenomenon is described in actualised packages as the fatigue-crack growth behaviour of an underfill. The number of cycles to failure, however, depended strongly

on the thermal loading (Menon, 2010; Stam and Davitt, 2001). Between T_{max}, 150^0C and T_{min} 200C, the growth rate of the underfill crack under thermal fatigue was characterised using the 'TENT' fatigue method (Stam and Davitt, 2001). Hence, in studying the reliability of a chip, its appearance and the growth of cracks undermined due to the effect of thermal cycling and humidity (Menon, 2010). Figure 2.43 presents a representative assembly under temperature cycling/vibration environment.

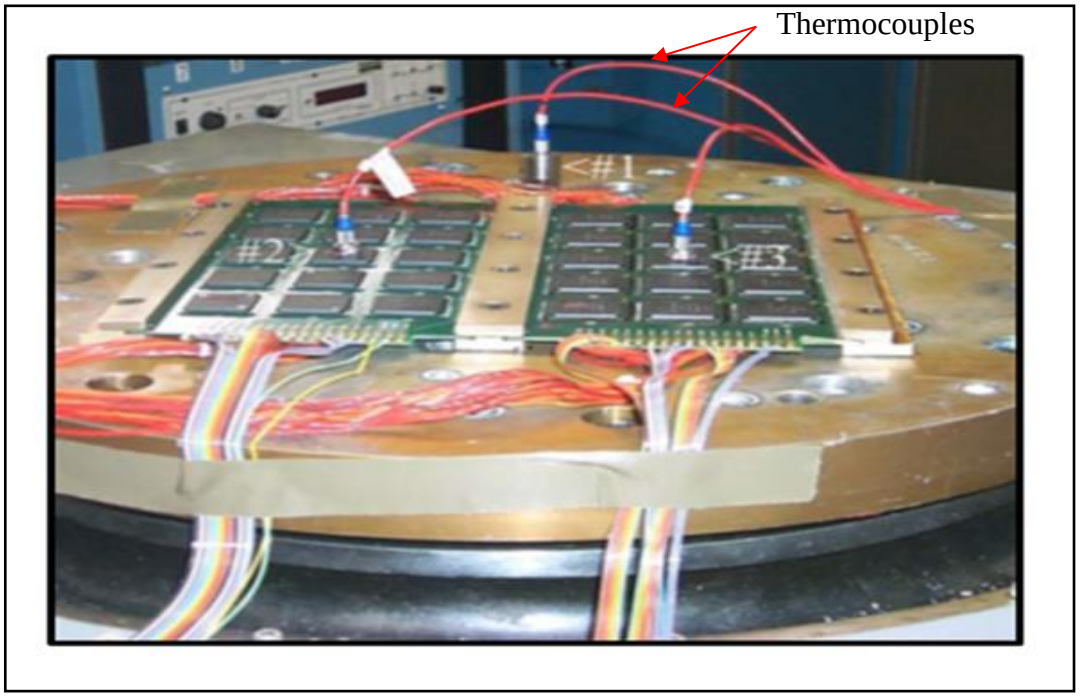


Figure 2.43: Temperature cycling/vibration environment with Thermocouples

Source: ***(Qi, 2006)***

Also, presented in Figures 2.44 and 2.45 are the schematics of both externally and internally generated applied heat during an Accelerated Thermal Cycling (ATC), and Power Cycling Test (PCT) in an environmental chamber for thermomechanical fatigue respectively.

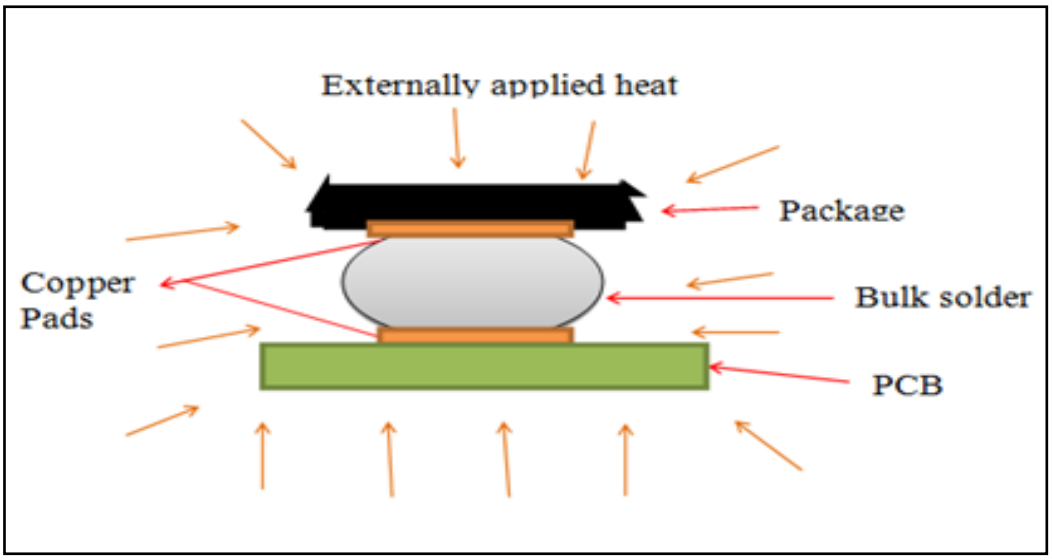


Figure 2.44: Schematic of Externally Applied Heat during ATC Test

Source: ***(Stam and Davitt, 2001)***

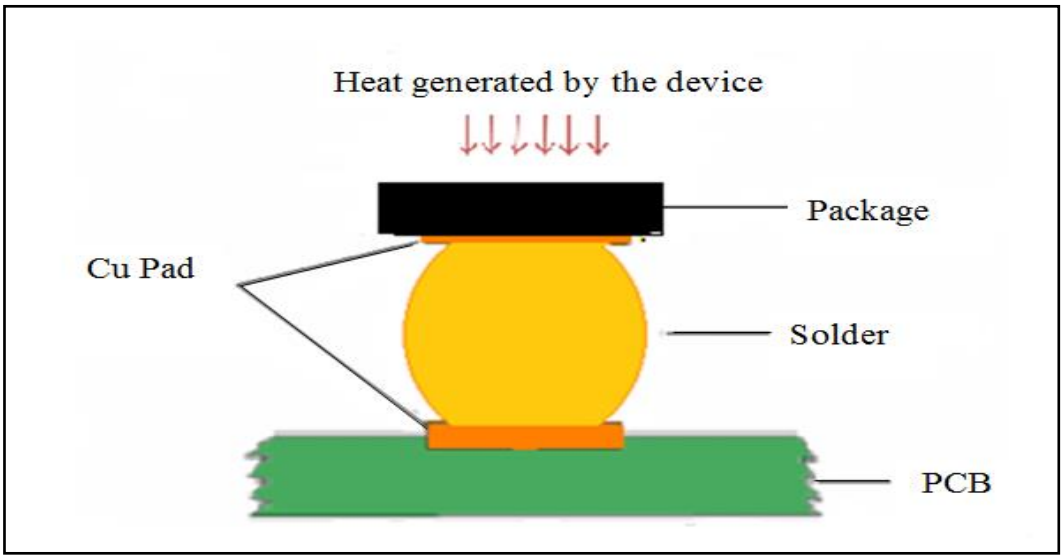


Figure 2.45: Schematic of Heat Generated/Applied during Power Cycling

Source: ***(Stam and Davitt, 2001)***

2.8.2 Test Time Prediction and Coffin- Masson's Equation

Test Time Prediction (TTP) determines the right BGA Solder Joints (SJs) life. However, SJs of BGAs assembled on PCBs is subjected to temperature cycling in relation with their acknowledged survival lifetime in the field. The lifetime is larger than 2500 cycles as estimated using experimentally energy-based method (Zhang et al., 2007). However, with a temperature range of 0°C to 100°C, BGA can survive a life cycle of up to 3000 to 8000 cycles, while QFP > 10,000 Cycles and BTC/QFN 1000 to 3000 cycles. Hence, an Acceleration Factor (AF) would be needed; thus, to calculate the acceleration factor, an equation must be utilised which is called the Coffin-Manson Equation. Coffin-Manson is the law bounding the number of cycles and crack initiation in solder joints which are related to the inelastic strain range using the results obtained from either FEM, experimental or analytical approaches of the BGA test pieces and the thermal fatigue test (Hariharan, 2007). The Coffin-Manson predict failures under longest-term use conditions, predictions usually acknowledged as being "conservative" or pessimistic. Nevertheless, and because they are strain based, have the existence of low cycle fatigue and nature of plastic deformation, they are preferred to Paris law, Milner's rule or Goodman's relation which are predominantly known for their high cycle fatigue damage mechanism.

A systematic approach such as ATC is used to establish a realistic evaluation of a thermal fatigue life of a solder joint (Yao, Qu and Sean X. Wu, 1999). ATC apart from being mainly applied to board level reliability, it also allows for precise temperature control, minimal thermal gradients and the ability to apply rapid ramp rates (20ºC/minute) for more manageable cycle times. It also helps in the identification and analysis of crack initiation and propagation of a solder joint, as it is hard ordinarily to explain or propose the difference in the fatigue life or failure rate of a quantified solder joint (Waine, Brierley and Pedder, 1982). Lifetime prediction of a solder joint is evaluated through a thermal cycle regime, employing ATC, which is useful in precipitating potential failure modes and generating failure time distributions in a reduced amount of time.

The life assessment duration can be made shorter using Coffin-Manson's acceleration factor (Mallik and Kaiser, 2014; Vasudevan and Fan, 2008; Dauksher, 2008), expressed mathematically in Equation 2.7.

$$AF = \frac{N_{field}}{N_{test}} = \left(\frac{F_{field}}{F_{test}}\right)^{-m} \cdot \left(\frac{\Delta T_{field}}{\Delta T_{test}}\right)^{-n} \cdot \left[e^{\frac{Ea}{K}\left(\frac{1}{T_{\max\ field}} - \frac{1}{T_{\max\ test}}\right)} \right] \quad (2.7)$$

, where:

AF = acceleration factor

Ea = the activation energy in electron-volts (eV)

K = the Boltzmann constant given as 8.617×10-5 eV/K

e = the base of the natural logarithm given as 2.71828

F_{field} = the cycle frequency in the field (a cycle/24 hours);

F_{test} = the cycle frequency in the laboratory

ΔT_{field} = the field temperature difference in use

ΔT_{test} = the laboratory temperature difference in use

$T_{max,\ field}$ = the maximum field temperature employed, and

$T_{max,\ test}$ = maximum test temperature while m and n are decay (fatigue) or Coffin-Manson exponent (Mallik and Kaiser, 2014).

The AF is a practical way of predicting a lifecycle of say 25 years of a device within a short duration of say ten days of chamber accelerated thermal cycling condition. However, to assess both the accuracy and the applicability models of AF is thus, a daunting task. It is because most of the models come with errors, or have their limitations regarding conditions to which they apply. Nevertheless, the AF expressed in a simple form in Equation 2.8 is directly proportional to the number of field temperature cycles and inversely proportional to the number of test temperatures (Mallik and Kaiser, 2014).

$$AF = \left[\frac{N_{field}}{N_{test}}\right]^{-m} \quad \text{or} \quad AF = \left[\frac{N_{test}}{N_{field}}\right]^{m} \quad (2.8)$$

, where:

N_{field} = Number of field temperature cycles and

N_{test} = Number of test temperature cycles in the lab while

m = Fatigue or Coffin-Manson exponent.

Alternatively, however, and for clarity, $AF = N_{use} / N_{test} = C(\Delta T_{use})^{-n} / C(\Delta T_{test})^{-n}$, where: ΔT_{use} is the difference between the maximum and minimum temperatures that the device will see in the field within one 'cycle of operation'. Moreover, ΔT_{test} is the difference between the maximum and minimum temperatures used in temperature cycling in the thermal chamber and *C is* the material constant. In practice, if a product undergoes 5daily temperature transitions for example, from 20°C to 65°C while it is usually in operation or use condition, then: (ΔT_{use} = 45°C). If the same product thermally cycled is at an elevated temperature of say 130°C and a low temperature of -20°C, then, (ΔT_{test} = 150°C). By assuming a typical Coffin-Manson exponent of 3, the resulting acceleration will occur: $AF = (150 / 45)^3 = 36.3$.

Furthermore, the product test at 1000 temperature cycles, using the same accelerated thermal testing conditions, would amount to approximately 20 years of life, for example: (36.3 X 1000 cycles) / ((5 cycles per day) (365days per year)) = 19.89 years (to two decimal places). To avoid error and prevent failure mode, both the upper and lower temperatures used must not exceed the temperature limits of the product. The test conditions chosen must be appropriate and done with care to avoid some of the limitations encountered during temperature cycling.

2.9 Chapter Summary

The review of literature carried out in this section is vital to analysing issues related to thermomechanical reliability assessment of solder joints in surface mount electronic assembly. In consideration to the review, the thermomechanical reliability of solder joints in microelectronics depends hugely on the standoff height of the components used in their manufacture. New trends in more advanced and speedy technology with high I/O pin counts also induced the use of highly miniaturised components. Miniaturisation of electronic products operating in harsh environments as identified is one biggest issue menacing the industry. There is much desire for the solder joint of a miniaturised component to run rapidly and reliably in this environment and this has formed the basis for choosing small BGAs and chip resistors for this study. The review on the effect of reflow soldering profile showed that the focus of the studies was on understanding the importance of specific parameters such as the preheat slope, peak temperature, time above Liquidus and cooling rate. There is the need to identify which of these parameters has the greatest impact on the reliability of the joints and how to control it.

Leading causes of solder joints failure was also reviewed, and this information has helped in the choice of proper reflow profile for peak solder temperature, pick and place machine to help in resolving component alignment and precision issues, including the selection for the right lead-free solder alloy in this study. The review includes a report on the effect of extended operations in different temperatures on the integrity of SJs in the assembled components while identifying the failure site and mode in the joints using analytical models, which lacks experimental basis. However, experimental data is required to validate the theoretical claims. It is in this background that the objectives of this study lie. The review also identified various ways solder joint reliability challenges occur, and the knowledge served as the basis for understanding and undertaking a critical analysis of solder joint failure criterion and damage mechanism in this work. Issues of solder joint formation; shear strength, and lifetime predictions under accelerated thermal cycling conditions with emphasis on 'Acceleration Factor' using Coffin Mansion equation already discussed in this chapter.

For applications requiring high-reliability operations, an accurate measurement of the thermal resistance is imperative to provide the user with knowledge of the SJs operating temperature, to make more accurate life estimates. In general, many factors determine the reliability of the solder joints in area array packages mounted on a PCB using solder alloy or flux. During the

manufacturing process, the mismatches in the CTE of the different bonded materials in the assembly were according to this review reported to account for stress inducement during temperature variations/cycling; and thus is the primary driving force on thermomechanical failure and reliability study for investigation in this work. The literature reviewed also showed that fragile nature of IMC affect the chip-level safety of HTEs, and information on the morphology of the material microstructure would be required to analyse the failed surfaces/joint. The literature search has identified the following gaps as outstanding areas of research because of lack of understanding and scarcity of data:

- ***Optimisation of reflow profiles parameters***

The optimised parameters of the reflow profile help to minimise maximum stress on solder joint and promote maximum reliability of the device. There is the need to 'Optimise' the reflow process parameters in this research work to achieve the required solder joint for optimal performance.

- ***The relationship between the impact and the mode of solder joint failure***

It is still not clear how the fracture mode (brittle or ductile fracture) changes with the rate of impact, especially after ageing the solder joints at a high temperature of up to 150- 175 ^{0}C. The strain rate for a chosen solder joint is determined to check for this behaviour.

- ***The impact of CSH and IMC on solder- joint shear strength reliability***

There is still no benchmark for the fair value of CSH for a reliable solder joint (for area array type of packages, such as ball grid array and CSPs).

- ***Solder joint failure due to voids formation***

Voiding in BGA has been controversial. On the one hand, it is an empty stress concentration. It is in expectation that the presence of voids can reduce the impact strength, ductility, creep and fatigue life of the mechanical properties of the joints. The actual percentage of a vacuum created in a joint (void) that can impact on the reliability of SJs has to be known and how to avoid or reduce them are in high demand by component manufacturers.

- ***The long term reliability of lead-free solder joints***

The lead-free solder was only introduced in 2006, and it is still very unclear how these solder alloys will behave in the long term. ATC is a proper tool to monitor and check this behaviour.

Chapter 3: Experimental Methodology, Equipment and Materials

3.1 Introduction

Chapter three presents an overview of the experimental methodology and materials used in the study reported in this thesis. The first part of the chapter shows the method, the experimental details and a description of the test vehicles used in carrying out the study. The second part describes the innovative materials, equipment and procedure employed in this work. The third part presents the manufacturing process of solder joints stencil printing used in the study. The fourth section concerns a description of the reflow profile for the formation of solder joints and the thermal ageing processes respectively. The fifth and last part present the metallographic preparation of test samples for the measurement of CSH and IMC, and for the microstructural analysis of solder joints.

3.2 Methodology, Experimental Details and Description of Test Vehicles

3.2.1 Methodology

The method used in this investigation is the scientific and experimental approach. It comprises of Experimental Details, Test Vehicle Preparation/Assembly Procedure, Equipment and Materials. The process of innovative design as a method involving both quantitative and qualitative techniques is in principle, adopted in the data analysis. The experimental data was validated using results from the literature. Figure 3.1 presents the flow chart of the experimental methodology used in this work.

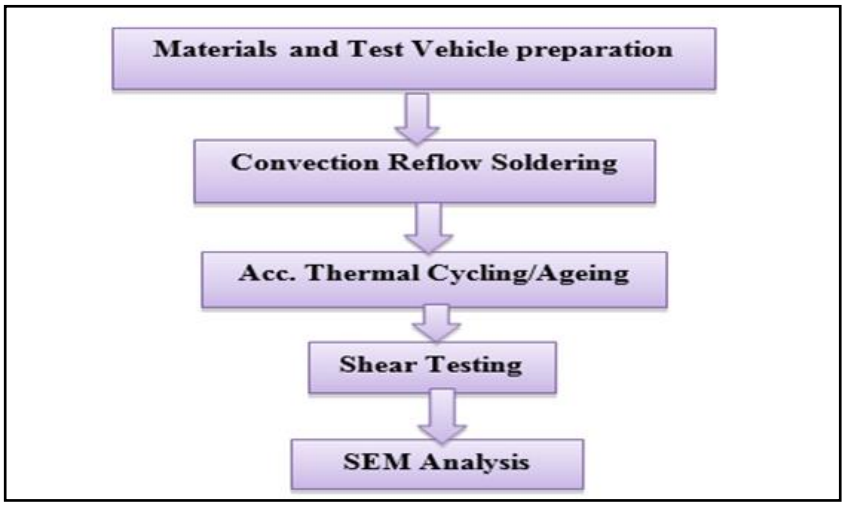


Figure 3.1: Flow chart of the experimental methodology

3.2.2 Experimental Details

This section presents a description of the experimental details. Figure 3.2 illustrated in the form of a shuttle card flowchart gives an overview of the pictorial representation of the entire chapter ranging from experimental set up to the conclusion. The significant points include for example test vehicles, used in a sequential manner to achieve the results reported in this thesis. Test vehicles with Sn-Ag-Cu lead-free solder paste and component chip resistors are prepared using the Benchmarker II stencil filling apertures shown in Figure 3.3. The experimental details, however, affords the reader an opportunity to have at a glance of what is contend in the overall chapter without necessarily going through all. All the experimental tools and equipment used in this study are located at the Engineering Science and Manufacturing Systems Laboratory of the University of Greenwich at Medway, UK.

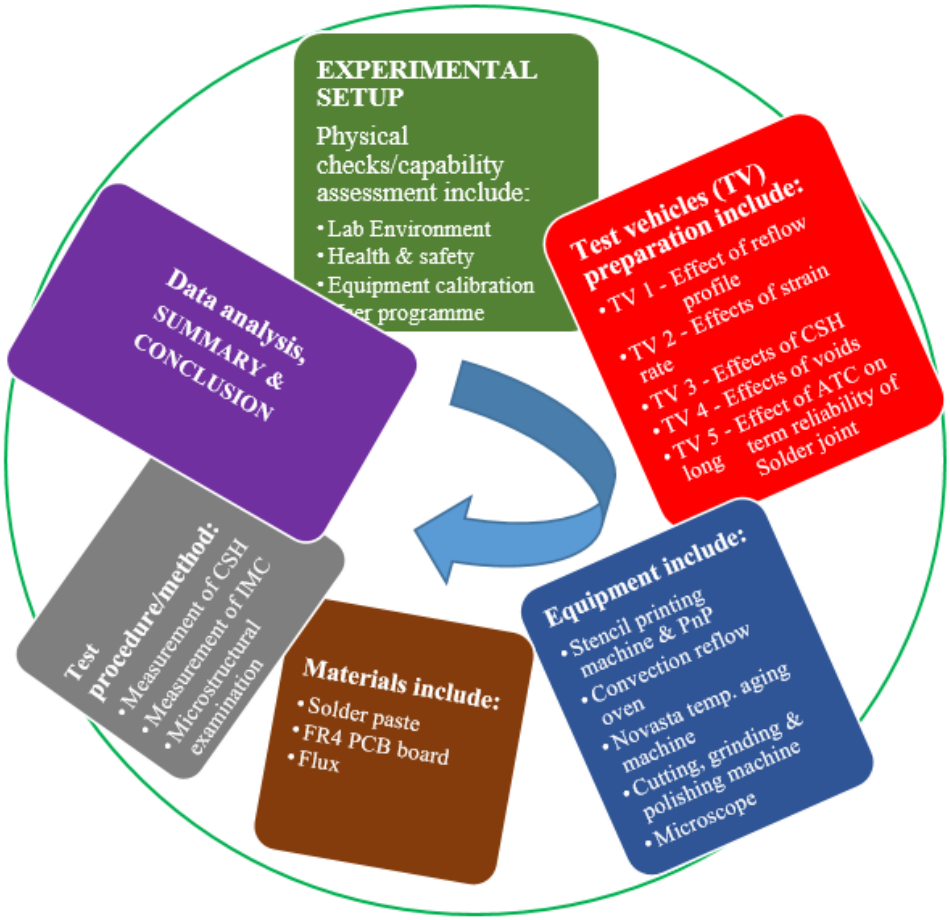


Figure 3.2: Experimental details

3.2.3 Test Vehicles Description

In this study, five types of test vehicle designs were made in-house using SMT materials commonly utilised in the manufacture and assembly of electronics components. Cu and Sn-plated (surface finishes) substrates were used to fabricate the test vehicles. The test vehicles were designed using half-automated stencil printing machine or done manually by using Benchmarker II stencil as presented in Figure 3.3. Details of the experimental test vehicles are shown in Figures 3.5, 3.9, 3.12, 3.13, 3.14, and Figure 3.16 respectively.

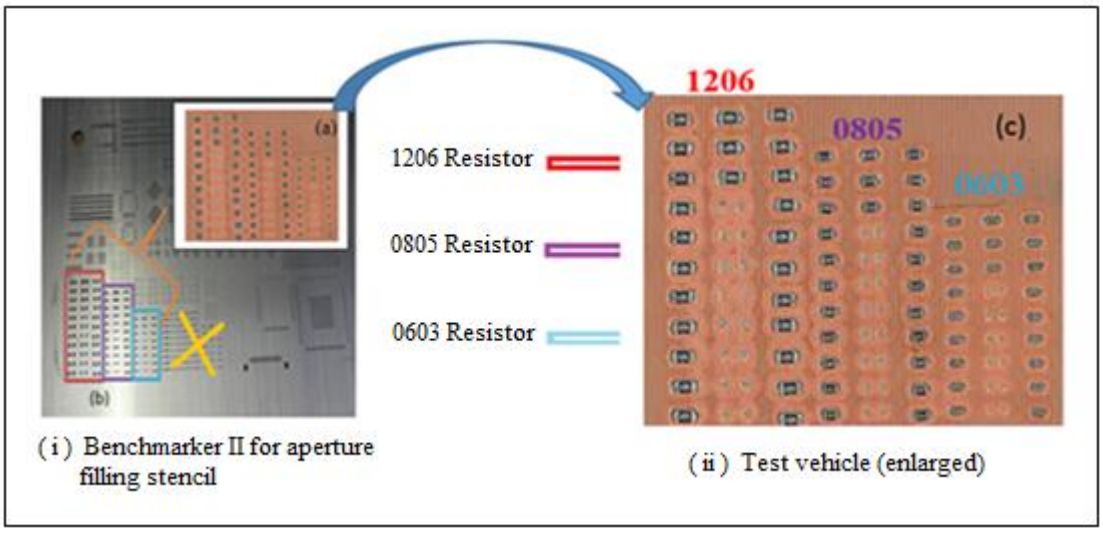


Figure 3.3: Benchmarker II showing areas of interest & enlarged test vehicle

3.2.4 Test Vehicle 1: Effect of Reflow Profile Verification

Test vehicle 1 (Figure 3.5) was designed to verify the effect of reflow profile parameter setting on the shear strength of solder joints in SMT chip resistors assembly. The test vehicle consists of a fabricated single sided 100% copper clad FR4 board strips with a thick film metallisation and a substrate dimension of (80 x 120 x 1.6) mm. Lead-free solder paste with alloy composition of 96Sn-3.8Ag-0.7Cu was used to complete the fabrication with the help of Benchmarker II stencil printing apertures (Figure 3.5 (i)). Three different pad sizes replicating pad sizes of typical SMT component resistors were used, these include 1206, 0805 and 0603 resistors. The experimental test Procedure in Figure 3.4 is for the ‘non-aged’ and ‘thermally aged’ samples. It comprises of five steps plus one additional step for the isothermally aged samples.

The steps employed in the experimental procedures include:

- Cleaning the substrates with isopropanol and placing them under the stencil strapped over with solder paste; such that it could stick to the substrate in the same pattern to form solder pads.

- As soon as the model of the solder paste was formed, and stencil removed, components were then, picked and placed. The placement uses a needle-like pen, which dips in the adhesive flux to have enough grip for picking and placing the components.

- Finally, substrates were used to assemble the three different types of components to form the test vehicles employed in this study.

- Steps 1 to 2 repeated to replicate five substrates each with 71 IC components. This same process was used to achieve the experimental results from test vehicle 2.

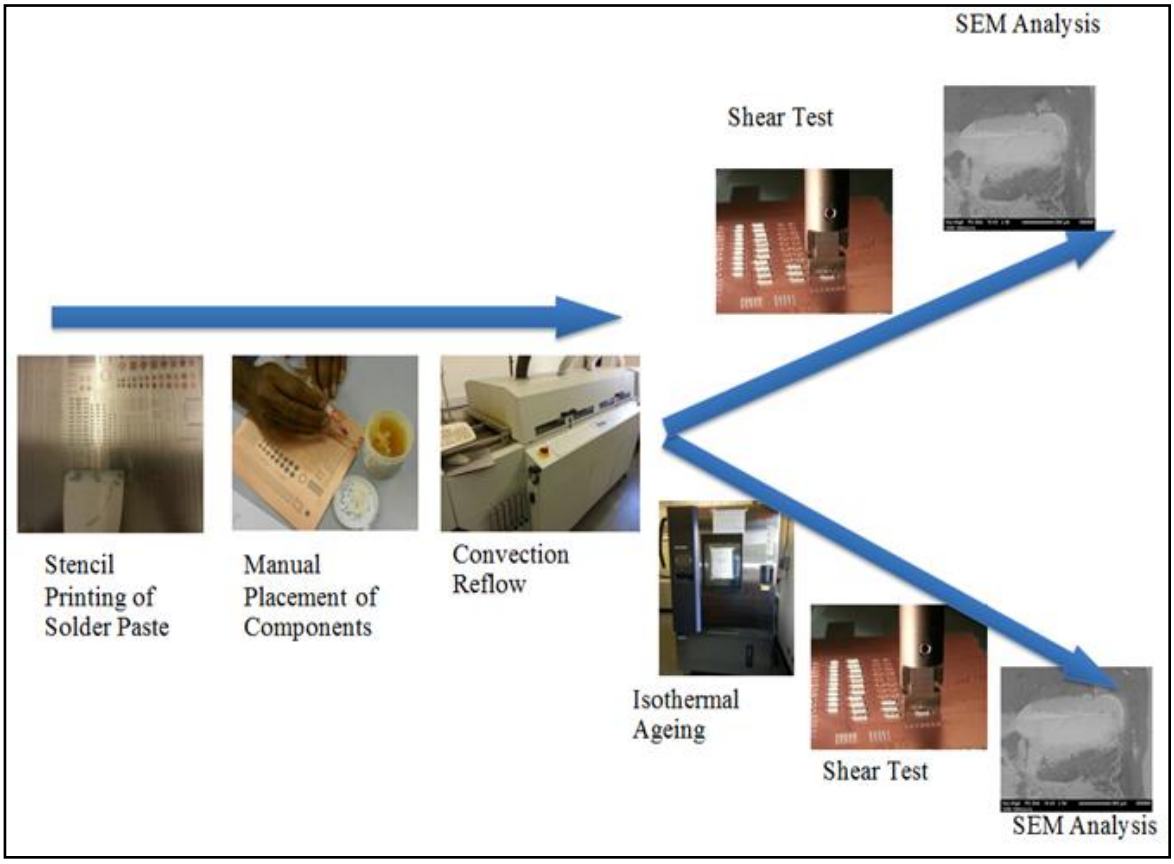


Figure 3.4: Experimental procedure of test vehicles

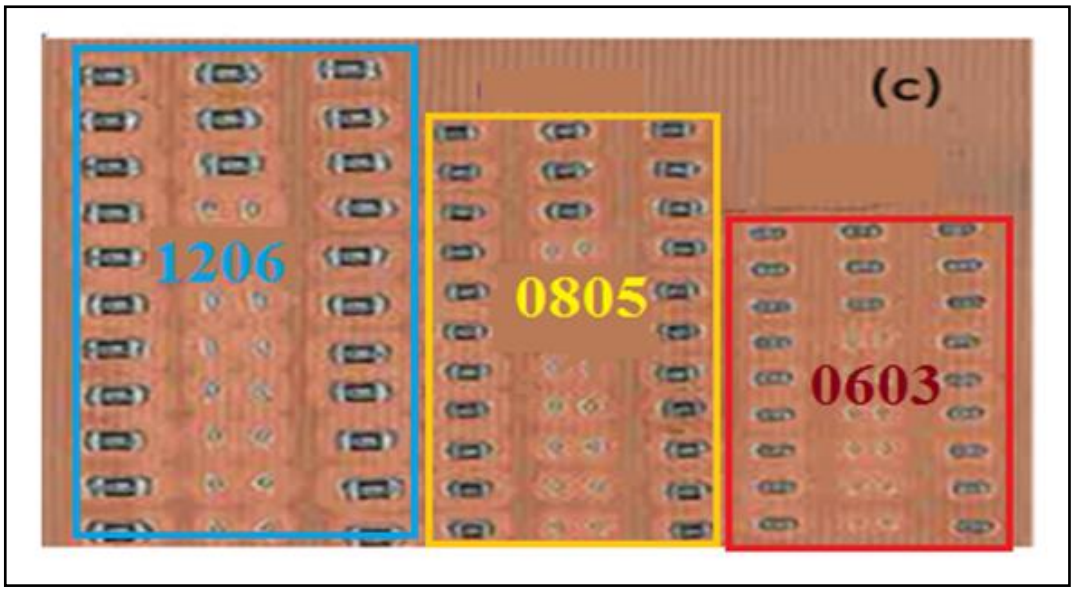


Figure 3.5: Test Vehicle 1 used for the effect of reflow profile parameter setting

3.2.5 Test Vehicle 2: Effects of Strain Rate Verification

Test vehicle two was for the effect of strain rate on the Thermomechanical Reliability (TMR) of surface mounted solder joints in electronic manufacturing.

Figure 3.9 shows test vehicle two which consists of three different types of surface mount chip resist*ors* (namely '1206', '0805' and '0603') as in test vehicle one shown in Figure 3.5. The resistors are reflow-soldered on the copper substrate according to the parameters shown in Table 3.1. The assembled surface mount components used five bare Cu boards for their fabricated substrate.

Two of the test vehicles were 'aged' isothermally for 24 hours at 150°C and a constant humidity of 35% RH. Each substrate contains 142 components for 'non-aged' samples used. The samples comprised of 50 components of 1206, 50 of 0805 and 42 of 0603 resistors. For the thermally aged specimens, the same number of components (as the non-aged) were used. A populated thermally aged Cu board at the ageing temperature of 150^0C for ten days is presented in Figure 3.6. A schematic of a standard SMT chip resistor is in Figure 3.7. The SMT resistors are widely used in automotive applications (Lau, 1991; De Gloria, 2014; Johnson et al., 2004; RS Components for Automotive, tape recorders, 2014; Middelhoek, 1994; Otiaba, Okereke and Bhatti, 2014).

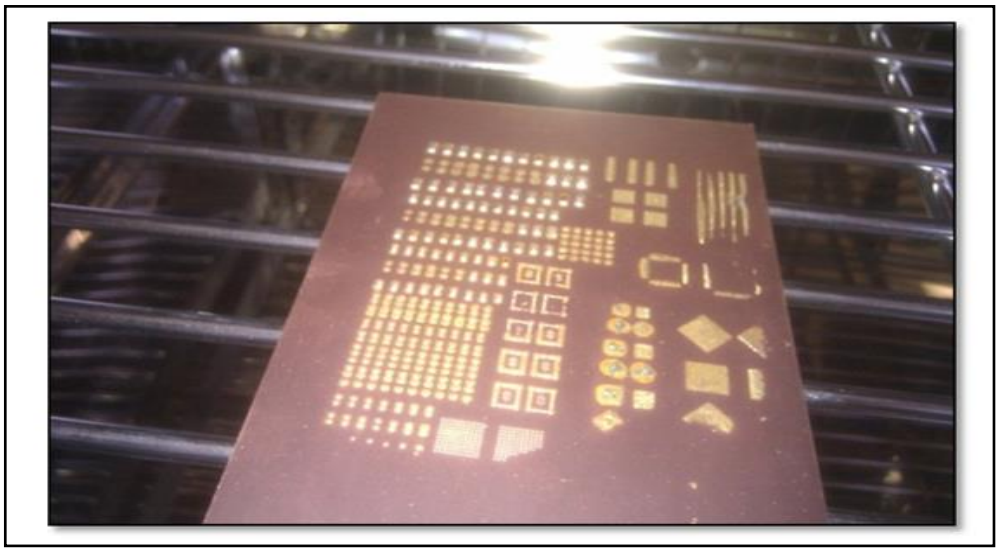


Figure 3.6: Cu PCB Sample with SMT Components Aged at 150^0C for 10 Days

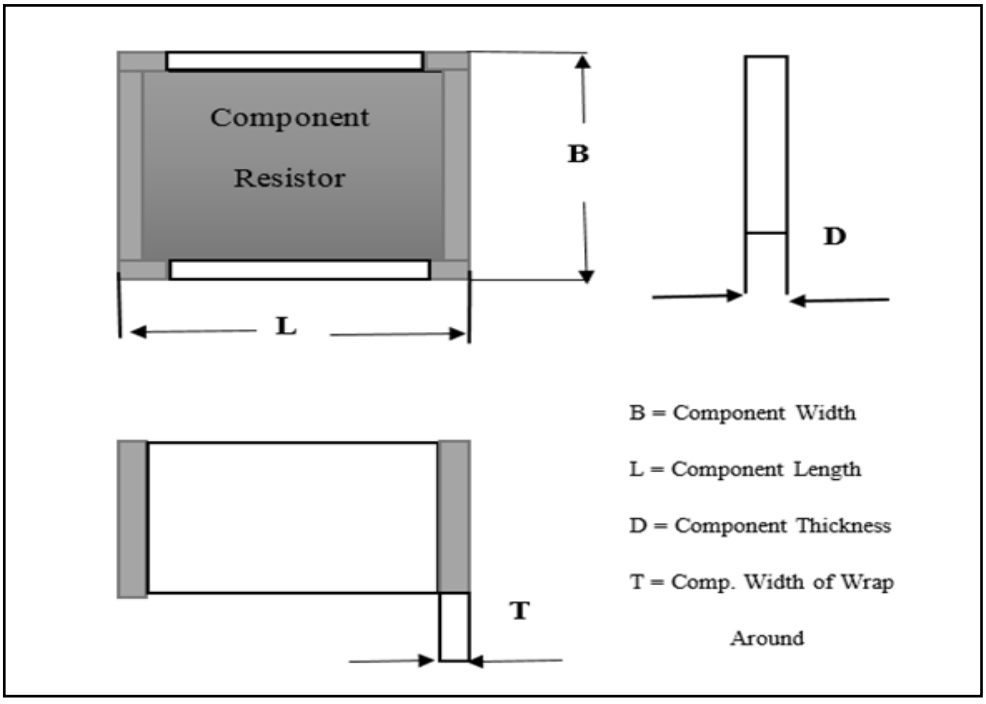


Figure 3.7: Schematic of a standard SMT chip resistor

Source: (RS Components for Automotive, tape recorders, 2014)

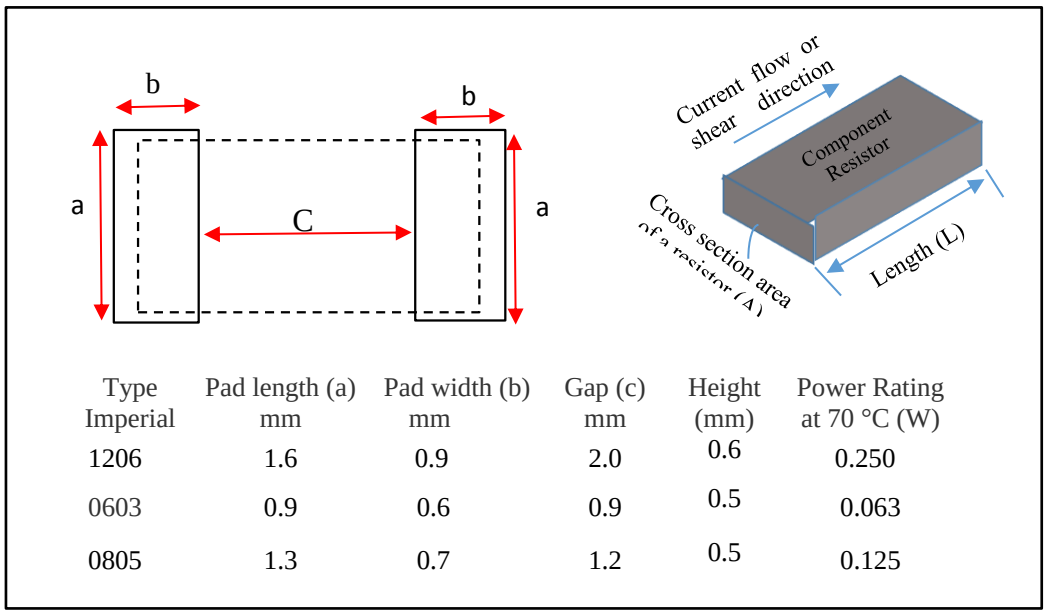
Table 3.1: Dimensions of the chip resistors (in mm)

Source: (RS Components for Automotive, tape recorders, 2014)

Type	Length, L	Width, B	Thickness, D	Width of wrap around, T	Weight (g) (1000pcs)
1206	3.10 ± 0.10	1.55 ± 0.10	0.55 ± 0.10	0.50 ± 0.20	8.947
0805	2.00 ± 0.10	1.25 ± 0.10	0.50 ± 0.10	0.40 ± 0.20	4.368
0603	1.60 ± 0.10	0.80 ± 0.10	0.45 ± 0.10	0.30 ± 0.20	2.042

3.2.5.1 Solder pad land pattern, size chart and shear area

The design of an SMT component uses the right solder pad size and land pattern upon which the shear area depends. During reflow soldering, however, the land width must be smaller than the chip resistor width to control the solder volume properly. For this purpose, usually the land width is set at 0.7 to 0.8 times (W) of the width of chip resistor while for reflow soldering solder size can be adjusted with a land width set to 1.0 to 1.3 times chip resistor width (W). These settings and land pattern measurements vary according to manufacturers' specifications and use environments (found from their data sheet) and which might differ slightly from the information provided in the chart given in Figure 3.8.



Type Imperial	Pad length (a) mm	Pad width (b) mm	Gap (c) mm	Height (mm)	Power Rating at 70 °C (W)
1206	1.6	0.9	2.0	0.6	0.250
0603	0.9	0.6	0.9	0.5	0.063
0805	1.3	0.7	1.2	0.5	0.125

Figure 3.8. Solder land pad and size chart of SMT chip resistors used

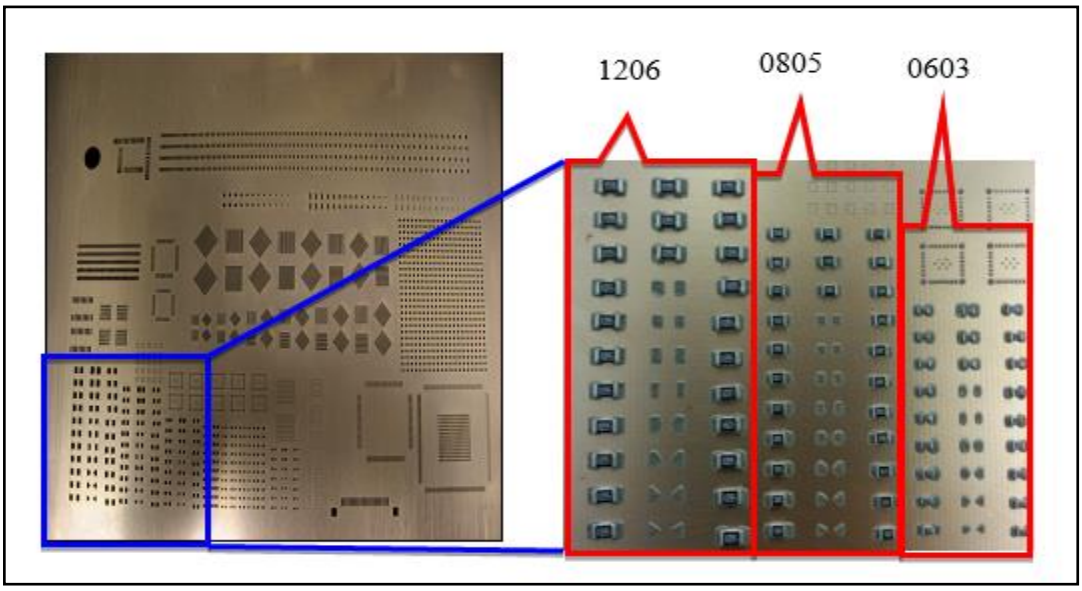


Figure 3.9: Test vehicle 2 utilised for the effect of strain rate on TMR

3.2.6 Test Vehicle 3: Effects of CSH Verification

Test vehicle three (3) was used for the effect of CSH on the thermomechanical reliability of BGA solder joints. Two experiments were conducted to check for the effect of pad size and temperature variation on solder joint reliability. Also, a third test was performed using a copper surface finish (CuSF) pad with board area dimension of 23 × 23mm and 1.55mm thick. It was prepared using surface mount assembly process shown in Figure 3.10.

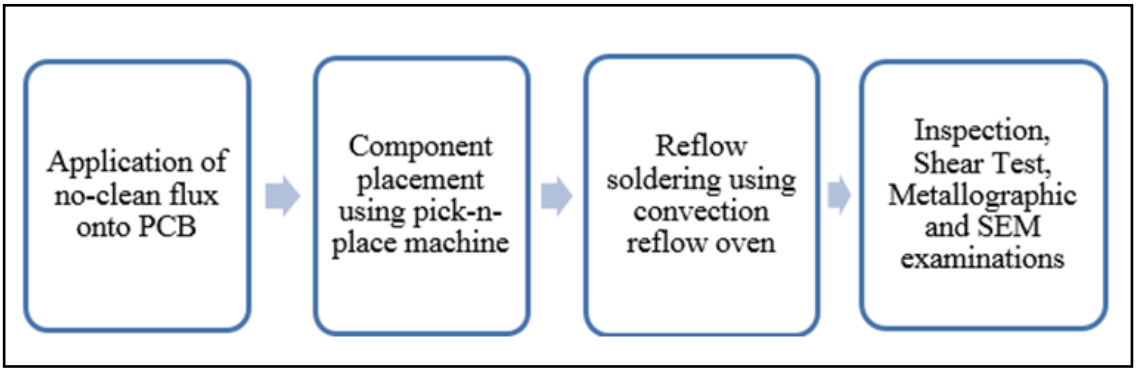


Figure 3.10: PCB Test vehicle assembly process

3.2.6.1 Test Vehicle Preparation (BGA81)

180 BGA81 components and 10 FR4 PCBs of (101.78 x 138.58 mm^2) size are used. Four BGA components of Sn-Ag-Cu solder alloy composition; 1.00 mm pitch dimension and 0.36 mm ball diameter are placed on each of the six different pad sizes: 19, 20, 21, 22, 23 and 24 mil diameters with two different surface finishes of Sn and Cu. The assembly process comprised of application of flux on PCB, component placement by pick-n-place machine for alignment of the BGA Die, reflow soldering of the assembly using a convection oven at a peak temperature of 235 °C and finally, visual inspection was carried out. The study design for CSH is given in Figure 3:11.

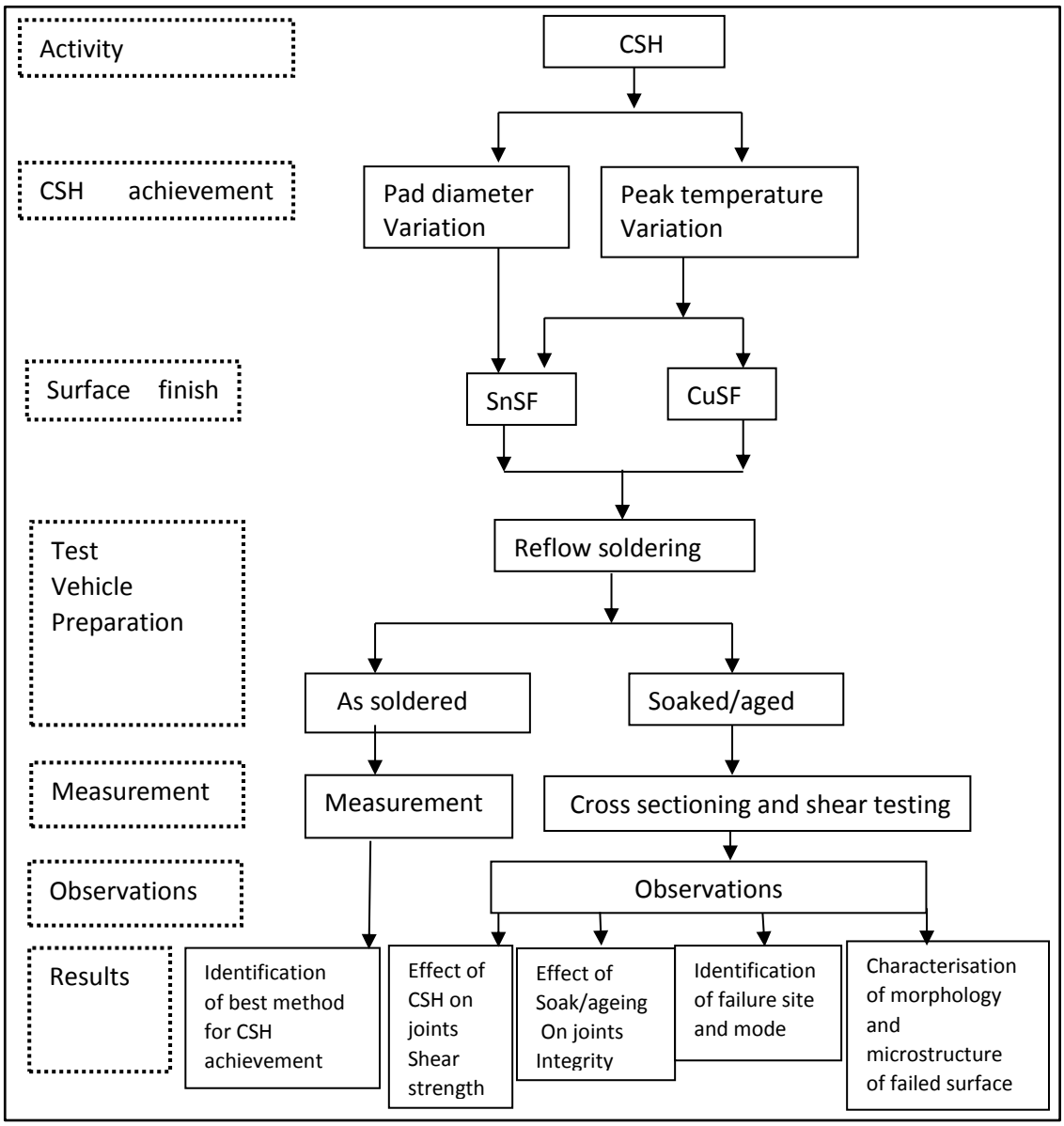


Figure 3.11: Research design for step- by-step CSH characterisation

The test samples for isothermal ageing placed in the environmental chamber operated at a temperature of 150^0C and relative humidity of 35% for '2, 4, 6 and 8' days respectively. The chamber program was to operate for 200hrs. Ten test vehicles were made in-house, five 'as-soldered' samples are used for shear tests, other five samples, which were 'aged', were cross-sectioned, and metallographic prepared for the measurement of CSH using SEM. Just as mentioned in section 3.2.6.1, Figure 3.11 presents also a step- by-step method of measuring the CSH; while Figure 3.12 (i) and (ii) represented the assembled test vehicle, and the BGA81 component used.

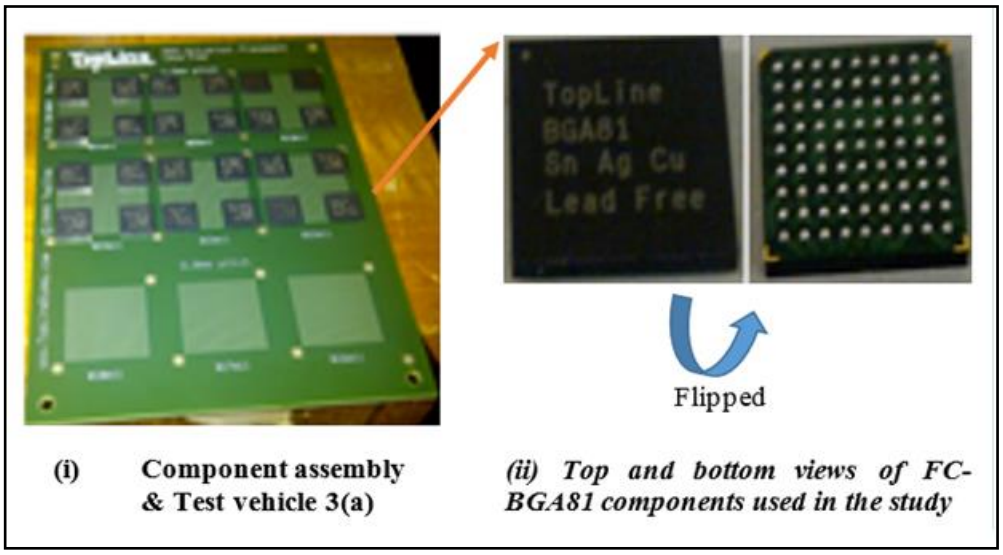


Figure 3.12: Test vehicle 3(a) - for effect of BGA81 CSH on TMR of SJs

3.2.6.2 Test Vehicle Preparation (BGA169)

For producing the test vehicles with BGA169 components, a similar process was followed (as prescribed earlier for BGA81 components). The main difference here was to use a constant pad size and different reflow peak temperatures (to achieve different CSHs).

3.2.6.3 Reflow and Ageing of BGA169 Assemblies

The assembled packages shown in Figure 3.13 were then reflowed using convection reflow oven (Novaster 2000 NT) described in section 3.4.3, which enables uniformity in the transfer of heat across all areas of the assembled packages. The purpose of the reflow process was to allow the convection heating of the solder alloy substance to attain a temperature which is a

little above the melting point of the alloy itself to enable soldering of the BGA169 solder balls onto the substrates to establish mechanical and electrical bonding of the assembly. Care was taken not to use temperature profiles, which could totally melt the solder alloy causing it to flow and causing bridging across the boards. Ramp-to-spike reflow profile at 225°C, 235°C, 245°C, and 255°C Peak temperatures with a tolerance level of ±5 was used to reflow the BGA169 devices for a duration time of 480s.

The soldered assemblies are separated into two halves, and one part was subjected to isothermal ageing at 150°C for 200 h (8 days) in an environmental ageing chamber (Espec ARS-0680), while the other halve was kept for comparison. The ageing of the test vehicles at the same isothermal temperature and time duration was carried out to ensure that IMC growth is constant across all the test vehicles.

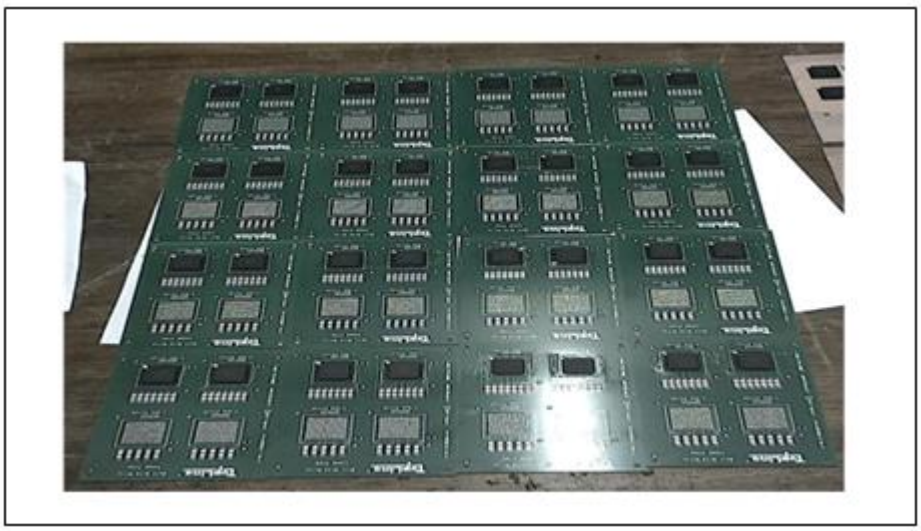


Figure 3.13: Test vehicle 3(b) - BGA169 on FR4 SnSF board for CSH.

3.2.7 Test Vehicle 4: Effect of Voids Verification

Test vehicle 4 presented in Figure 3.14 was fabricated to determine the effect of solder type, reflow profile and PCB surface finish on the formation of voids in BGA lead-free solder joints. The effect of surface finish on the PCB is the factor under investigation and two different pad surface finishes, Ni and copper boards were used to determine its effect on the formation of voids in the BGA solder joint.

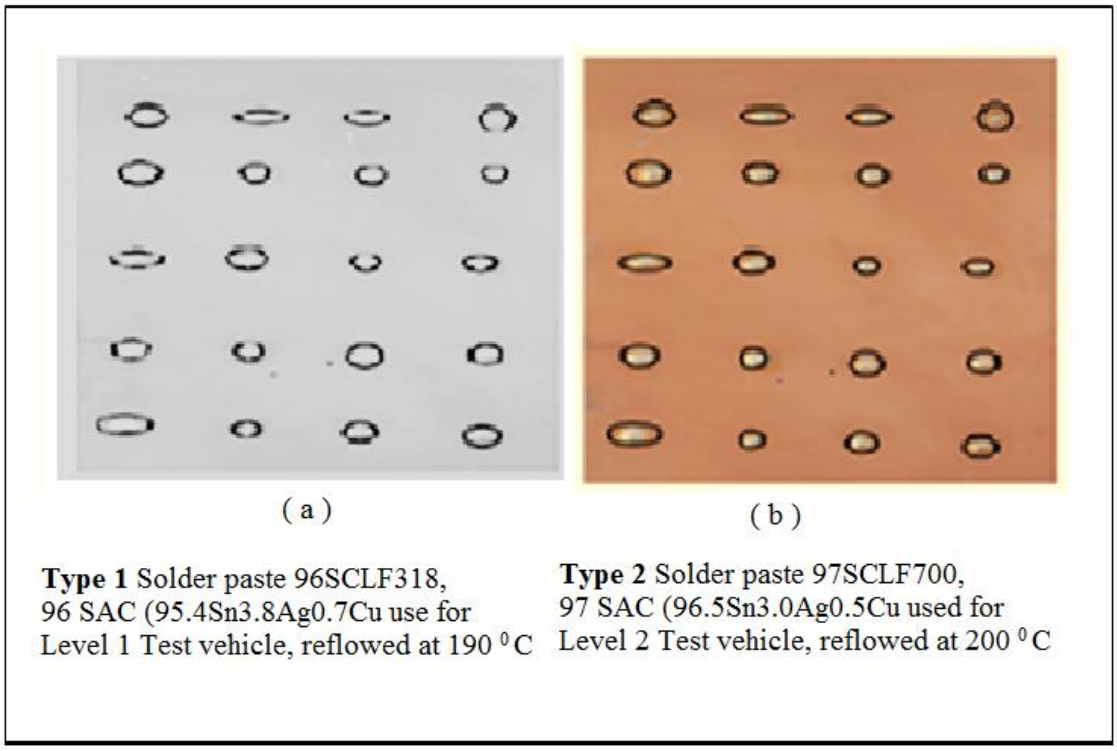


Figure 3:14: Test vehicle 4- for SB x-ray analysis on effects of voids in SJs

The Test vehicle four (4) board's dimension is (80 x 120 x 1.6) mm and each board consists of 20 soldered bumps. The boards were cleaned using Methylated spirit and Isocline Isopropanol to increase wettability and minimise voids formation. The same two-stage cleaning process was employed to clean the stencil and squeegee utilised during solder printing process. The paste types are 96SC LF 318 and 97SC LF700. The former is level 1 while the latter is level 2. Also, the nickel (Ni) PCB pad finish used was tagged level 1 and copper (Cu) is level 2. The third factor is the reflow profile, only one parameter of it was under consideration, and this is the activation energy. Activation energy identified as a critical element of this investigation has its effect on the formation of a quality solder joint. During activation stage of reflow profile, the flux in the solder paste and other soluble contents was driven off. It has been reported by (Beddingfield and Higgins, 1998) that the amount of flux including other solvents matter in the solder paste mix determines the percentage by volume of voids in the solder joint. The activation temperature has a direct influence on the degree to which the flux matrix is driven off the paste mix. Thus, two different activation temperatures are used for the reflow profile. Level 1 is a 190°C, and level 2 is a 200°C centigrade temperatures. Table 7.1 presented in Chapter 7 section 7.3 the designated solder paste as A, reflow profile as B and PCB surface finish as C. It also shows the levels, as '1 and 2'. The experiment was conducted using full

factorial design. Stencil printing/bumping of the solder paste on the pad surface was the next process, followed by component placing and formation of the solder joint through reflow soldering process described in section 3.4.3. The reflow profile used is presented in Chapter 7, Figures 7.3 - 7.6.

3.2.8 Test Vehicle 5: Effect of ATC on Long Term Reliability of Solder Joint

Test vehicle five (5) was used to investigate the effect of Accelerated Thermal Cycles (ATC) on the long-term reliability of solder joints. The test vehicle was prepared by manual placement of BGA solder balls on flexible substrates with the aid of halide flux, which serves as adhesives and oxide remover. The solder ball is lead-free, 0.76 mm in diameter and has alloy composition of Sn-4.0Ag-0.5Cu (SAC405). The board consists of electroplated Au/Ni-Cu pad. A total number of 100 pads were used to achieve this work. The assembled boards are divided into five groups with one kept for 'as-reflowed' sample and the rest thermally cycled for 33, 66, 99 and 132 hours. The parameters and the temperature profile used for this investigation are selected according to JEDEC standard, JESD22-104D (JEDEC, 2009). The test condition for the temperature cycling and the thermal chamber was set to operate at 43 minutes per cycle and has a temperature range of 0^{o}C to 150^{o}C with a ramp rate of 3.5^{o}C/minute (150^{o}C/43mins) resulting in a dwell time of 10 minutes, ramp down and ramp up of 11.5 minutes each respectively. The parameters and the temperature profile are made available in Table 3.2 and Figure 3.14 respectively. The flexible substrate test vehicle and materials for its preparation are shown in Figure 3.15, while the same test vehicle, equipment and experimentation processes are presented in the form of a flow system illustrated in Figure 3.16.

Table 3.2: Thermal Cycling Parameters

Low Temperature	High Temperature	Ramp Rate	Dwell Time	Cycle Period
0^{0}C	150^{0}C	11.5^{0}C/ min	10 min.	43 min.

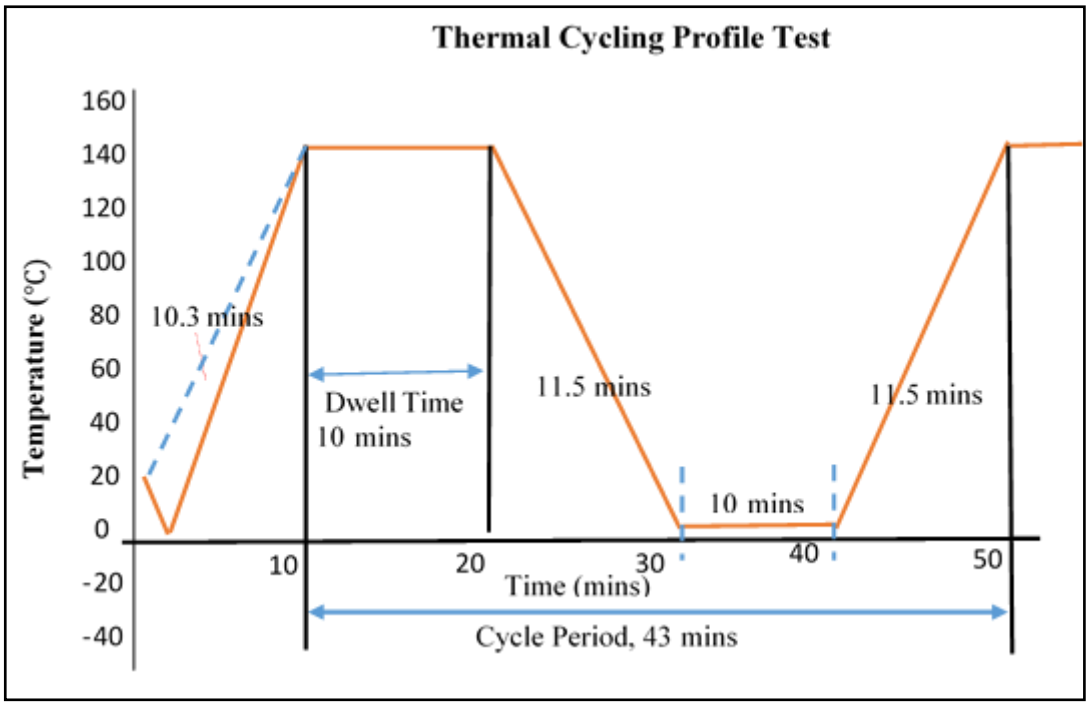


Figure 3.14: Thermal Cycling Profile measured for 43 mins per period

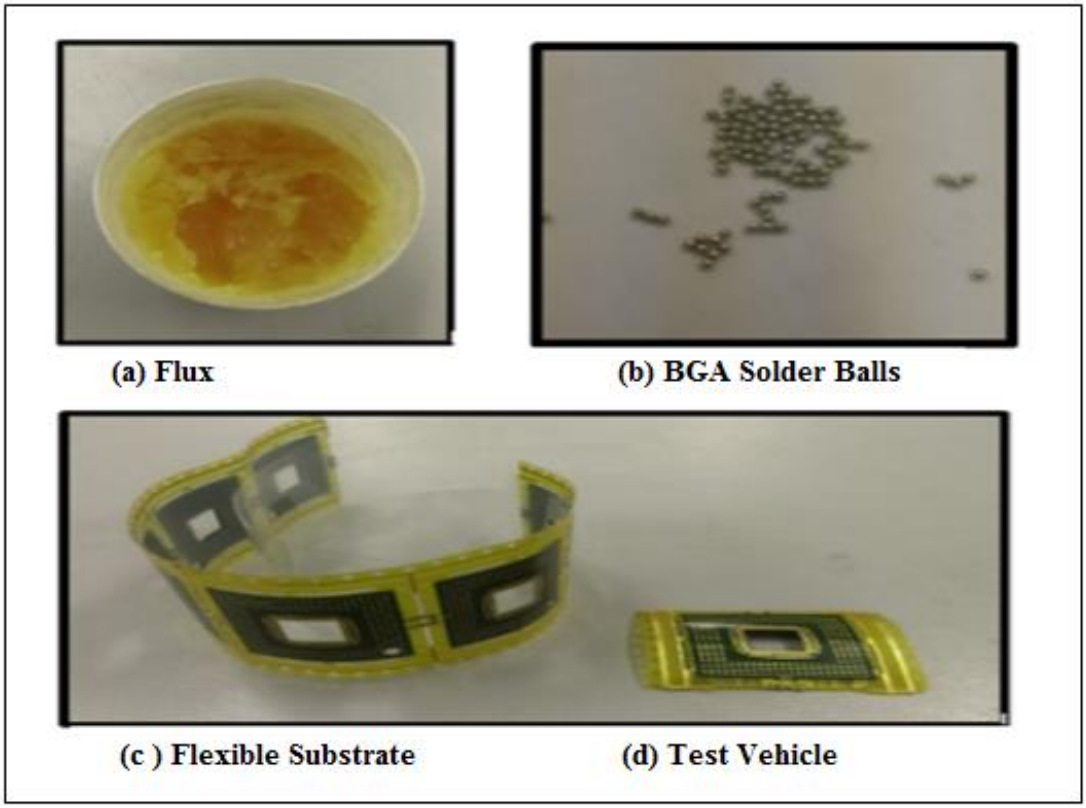


Figure 3.15: Test vehicle 5 - showing its material constituents from (a-c)

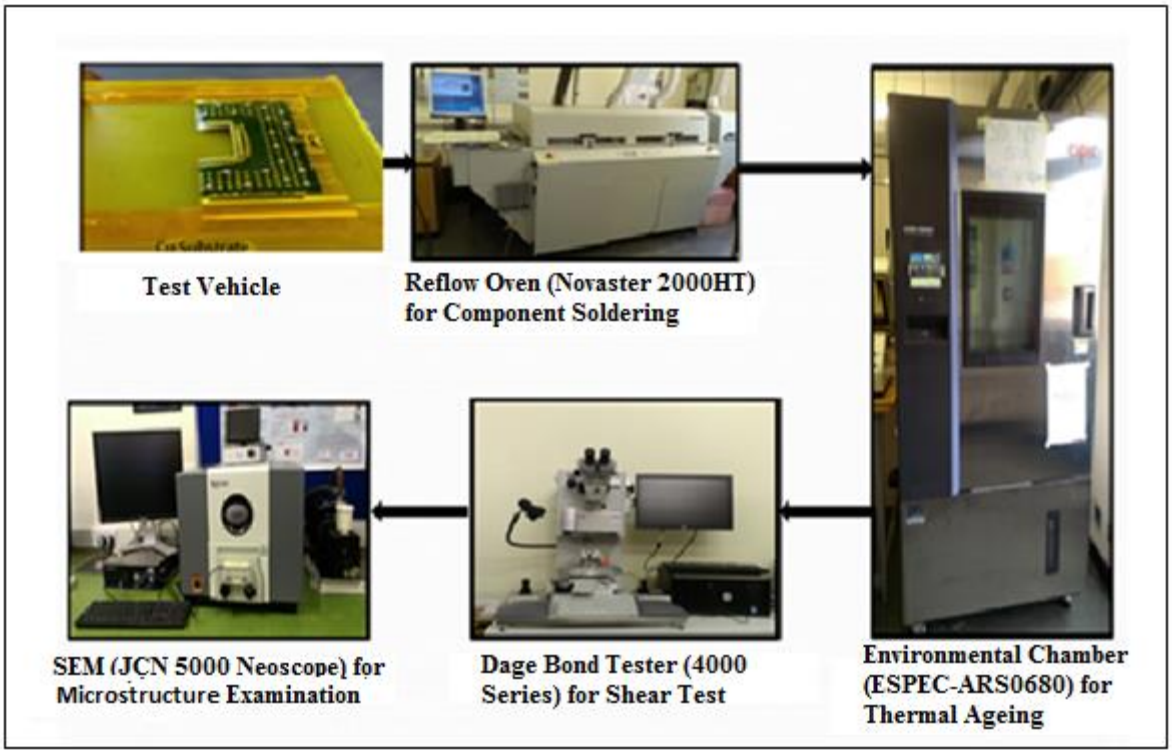


Figure 3.16: Test vehicle, equipment and processes used in the study

3.3 Materials and Processes

The key materials used in this investigation most of which were discussed in the previous sections consist of three different sizes of surface mount chip resistors (R1206, R0805 and R0603). They include multicore Sn-Ag-Cu lead-free solder paste, FR4 copper substrate, BGA components, halide flux, conductive bakelite powder and monocrystalline diamond suspensions, and only a few will be discussed here.

3.3.1 Sn-Ag-Cu Lead-free Solder Paste

A commercially available Tin-Silver-Copper lead-free solder paste sample with type 3 particle size distributions and alloy composition of (95.5w%Sn-3.8w%Ag-0.7w%Cu) weight percent (as previously discussed) are used in this investigation as the jointing material. It has a metal content of 88.5% by weight, and a melting point of 217^0C. The paste and its container are represented in Figure 3.17, while the dimensions of the chip resistors are given in Table 3.1 above. The particle size is acquired from the manufacturer's data sheet, and the paste sample is stored in a fridge at -4°C. The details of the respective samples are provided in Table 3.3. It

can be observed from the table that the size of the R1206 is the largest while that of the R0603 is the least. The size variation is introduced to study the impact of miniaturisation of electronic components and devices on the thermomechanical reliability of their solder joints. Other materials used for achieving the required research studies in this thesis are found in the chart provided in Figure 3.21.

Figure 3.17: Lead-free solder paste consisting of 95.5Sn 3.8Ag 0.7Cu alloy

Table 3.3: Solder paste details

Materials	**Content**
Solder Alloy	95.5Sn-3.8Ag-0.7Cu
Particle Size Distribution, µm	25-45
Metal Loading, weight %	88.5
Flux Type	No-clean and Halide-free

3.3.2 Universal FR-4 Board and BGA Flexible Substrate

The Universal FR-4 PCB is commercially available and lead-free components compliant. Three types of the FR-4 PCBs plus the flexible substrate are used in this study. Two of the FR-4s and the flexible substrate have surface finishes made of Tin while the other was made of copper. The first of the two has a tin-plated surface finish (Figure 3.19) with different pad diameters ranging from 19mil to 24mil for the sole purpose of the research findings and design. The substrate aims to mount up to twenty-four BGA81 components per side with pads having 1.0mm and 0.8mm pitches. However, the 1.0 mm pitch pad sizes were used for the experiments.

Four (4) components are placed on each of the different pads. Altogether, a total number of ten boards were used for the BGA81 CSH experiment as earlier described. The second is also a Tin Surface Finish (SnSF) FR-4 board with dimensions of area and thickness of 23x23 mm and 1.55 mm, respectively. Its pitch is 1.5 mm while the diameter of its pad is 0.584 mm (23 mils).

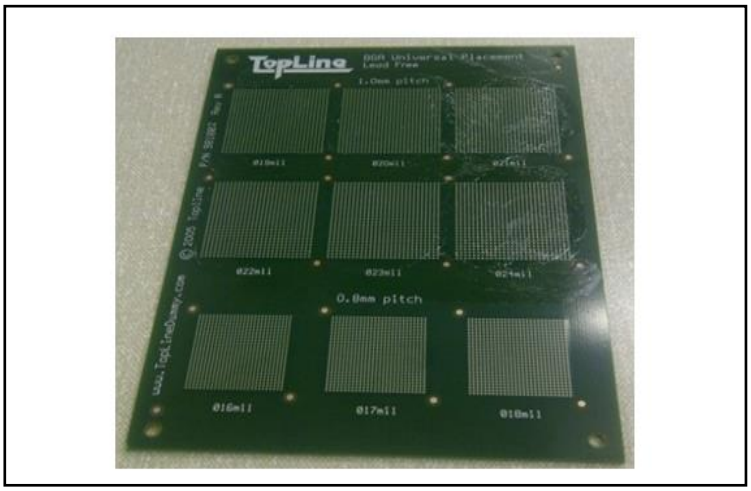


Figure 3.18: Image of the lead-free universal FR4 BGA printed circuit board

Similarly, the Copper Surface Finish (CuSF) board has an area of 23x23mm and thickness of 1.55mm. The flexible substrate was designed mainly to provide solutions to more fragile and highly miniaturised electronic components and integrated circuits. It is a technique, which greatly simplifies the making of interconnections between various planar portions of an assembly. The use of flexible substrate may include compact packaging configurations that enhance dynamic performance and ensure a cost-effective production part. Flux application precedes the component placement on PCBs and test vehicle preparations; or by stencil printing of solder paste on the tin-plated surface finish board, (or on bare Cu boards as was required). The components were mounted on all four types of (substrate) PCBs to form the test vehicles used. The two types of FR4 PCBs with SnSF and CuSF and the flex circuit described in the preceding discussions i s given in section 3.3.3. The full description of the Benchmarker II is in a chart shown in figure 3.21.

3.3.3 Benchmarker II Laser-cut Stencil

A stencil provides the openings for all the components on the board or substrate so that the printing of paste can be through the apertures. The number of openings on a stencil matches the number of openings required for the surface mount components on the board. Stencils are uniquely made to match specific PCB designs and may not be necessary for others. As shown in Figure 3.19 (a), a laser-cut stencil with a thickness of 0.125 mm was applied in this study, while Figure 3.19 (b) shows a close view of the Benchmarker II discussed earlier.

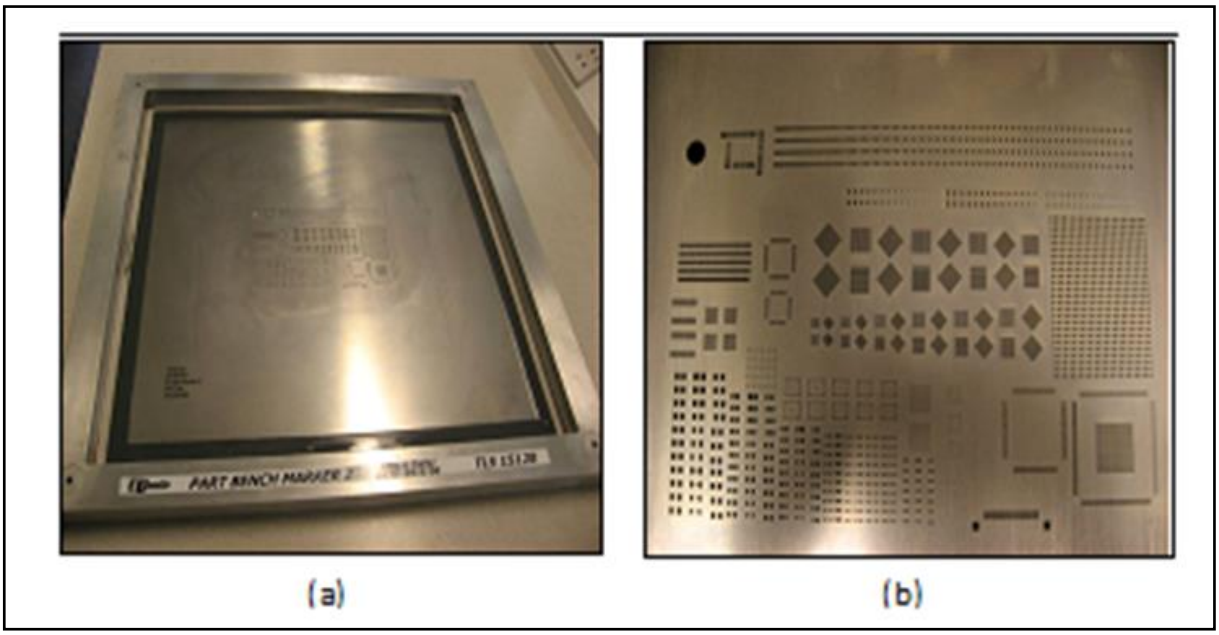


Figure 3.19: (a-b) Benchmarker II laser-cut stencil

3.3.4 Solder Flux

Flux acts as a temporary adhesive, holding the component in position before reflow soldering process. The solder flux utilised for this experiment is the no-clean type either rosin or halide flux (Figure 3.20 (d)), which is applied directly onto the surface of the printed circuit board during 'Test vehicle' preparation. The rosin flux is comprised primarily of refined natural resins extracted from the Oleoresin from pine trees. However, Rosin fluxes are inactive at room temperatures but become active when heated to soldering temperatures. The melting point of the resin is 172^0C to 175^0C. Rosin fluxes are used purposely to reduce solder balling and bridging, as well as aid proper solder paste flow and increased wetting of desired areas (Prasad,

1989; Ning-Cheng, 2002; Xun-ping et al., 2010). Another type of flux commonly in use in the laboratory for conducting the experiments in solder joints is the Halide flux. However, in electronic packaging and solder interconnect, halide flux whose content is of halogenated compounds, usually from bromides or chlorides have been in use for years to reduce metallic oxides. In previous years, there was great concern that ionic halide left on the PCB as residues could cause corrosion or dendritic growth in the solder joint of assembled components, and for this reason, the packaging industry of electronics solder alloy has begun to use covalently bonded halides, which are much more reliable and profitable.

3.3.5 Other Materials Used

3.3.5.1 Conductive Bakelite Powder

The conductive Bakelite (Figure 3.20 (e)) is a moulding powder developed specifically for use in thermal mounting processes. The powder comes in different colours and is particularly useful for electron microscopy, with sufficient electrical conductivity to provide a real solid earth leakage from the specimen (Azeem and Zain-Ul-Abdein, 2012; Muir Wood et al., 2003).

3.3.5.2 Monocrystalline Diamond Suspensions

The monocrystalline diamond suspensions (Figure 3.20 (f)) used for the specimen's metallurgical preparation are those of 6 microns and 1 micron respectively. The suspensions are applied onto the grinder via a nozzle or injection system before diamond polishing of the specimens. This suspension provides a chemo-mechanical polishing (CMP) action that significantly increases removal rates, reduces subsurface damage and improves surface finish (Muir Wood et al., 2003; Tighe, Worlock and Roukes, 1997).

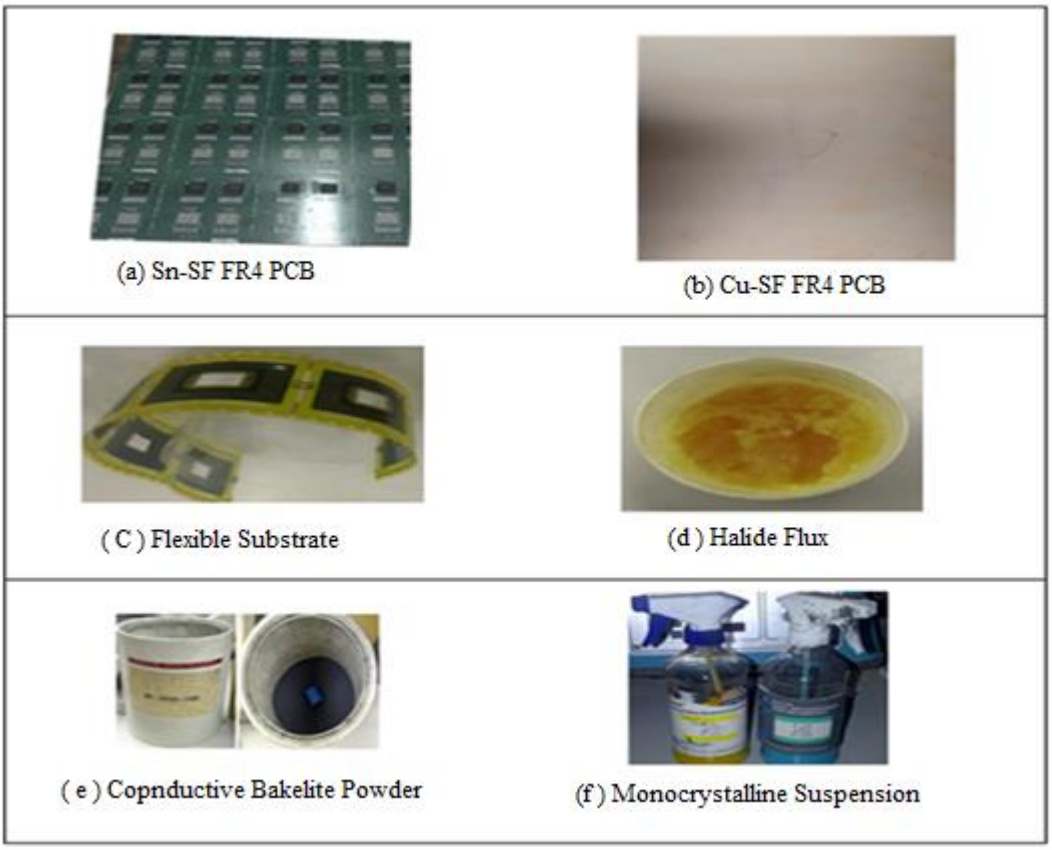


Figure 3.20: SMT materials used for the studies carried out in this thesis

3.3.6 Ball Grid Array Components and Their Geometric Representations

The BGAs employed in this work are of two types: BGA81 and BGA169. For a full description, the BGA 81 has 9x9 full matrix array, 10x10mm in size and 0.36mm/0.46mm bottom/top ball diameters. Its pitch is 1.0 mm while the composition of its lead-free solder alloy is 95.5%Sn-3.9%Ag-0.6%Cu (SAC405). The other component, BGA169, consists of 13x13 full matrix arrays and is 0.76mm in diameter. It has 1.5mm pitch dimension and the same composition of solder alloy as the BGA 81 component. Figure 3.21 (a) and (b) presents the lead-free BGA components while (c-d) show for example design settings for typical BGA81 and BGA169 components.

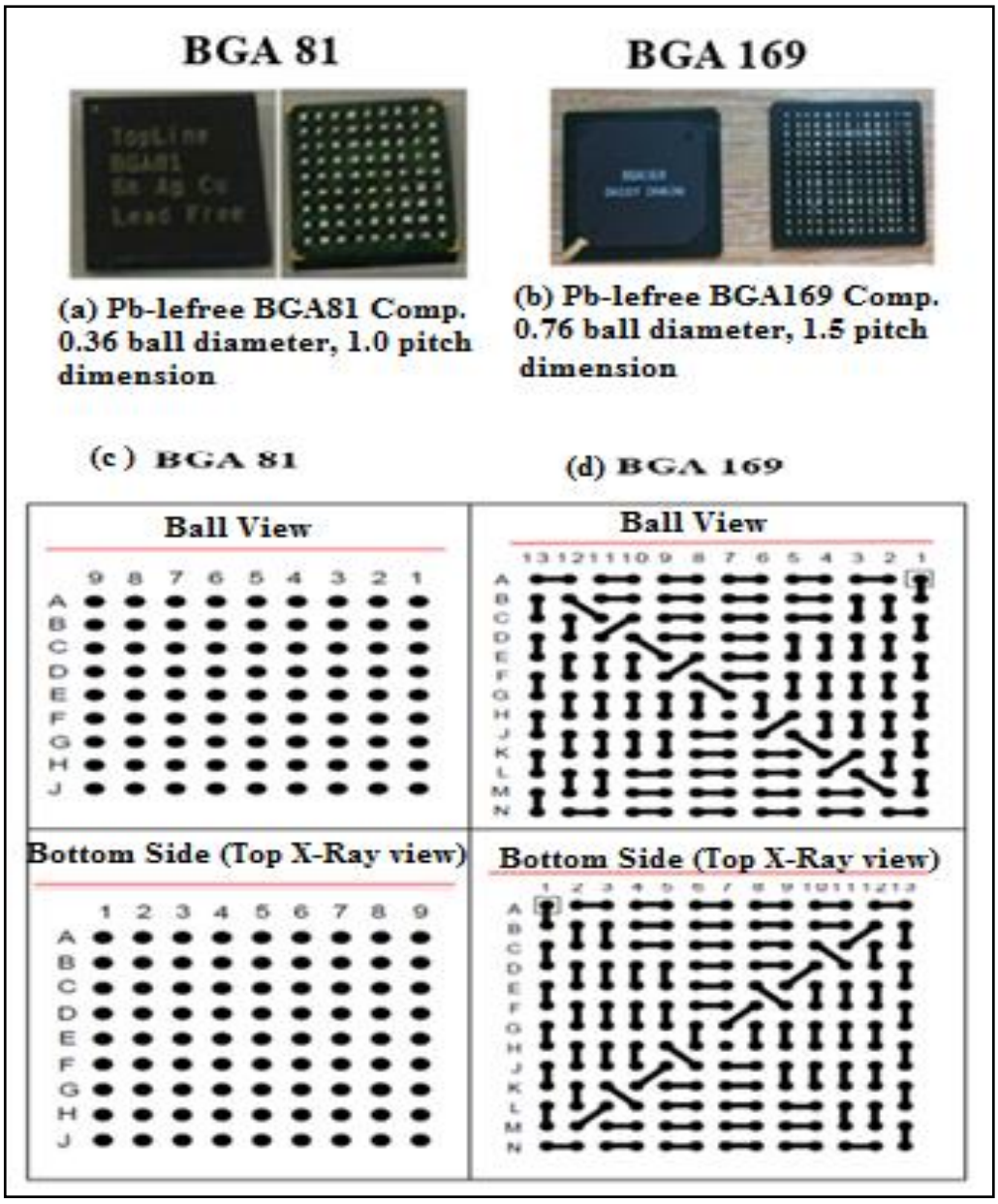


Figure 3.21: Pb-free BGA81 & 169 displaying (a-d) Top and bottom Side View

Nevertheless, Figure 3.22 presents the design configurations of BGA81 & 169 top and bottom ball view. Component manufacturers employ the configurations during assembly.

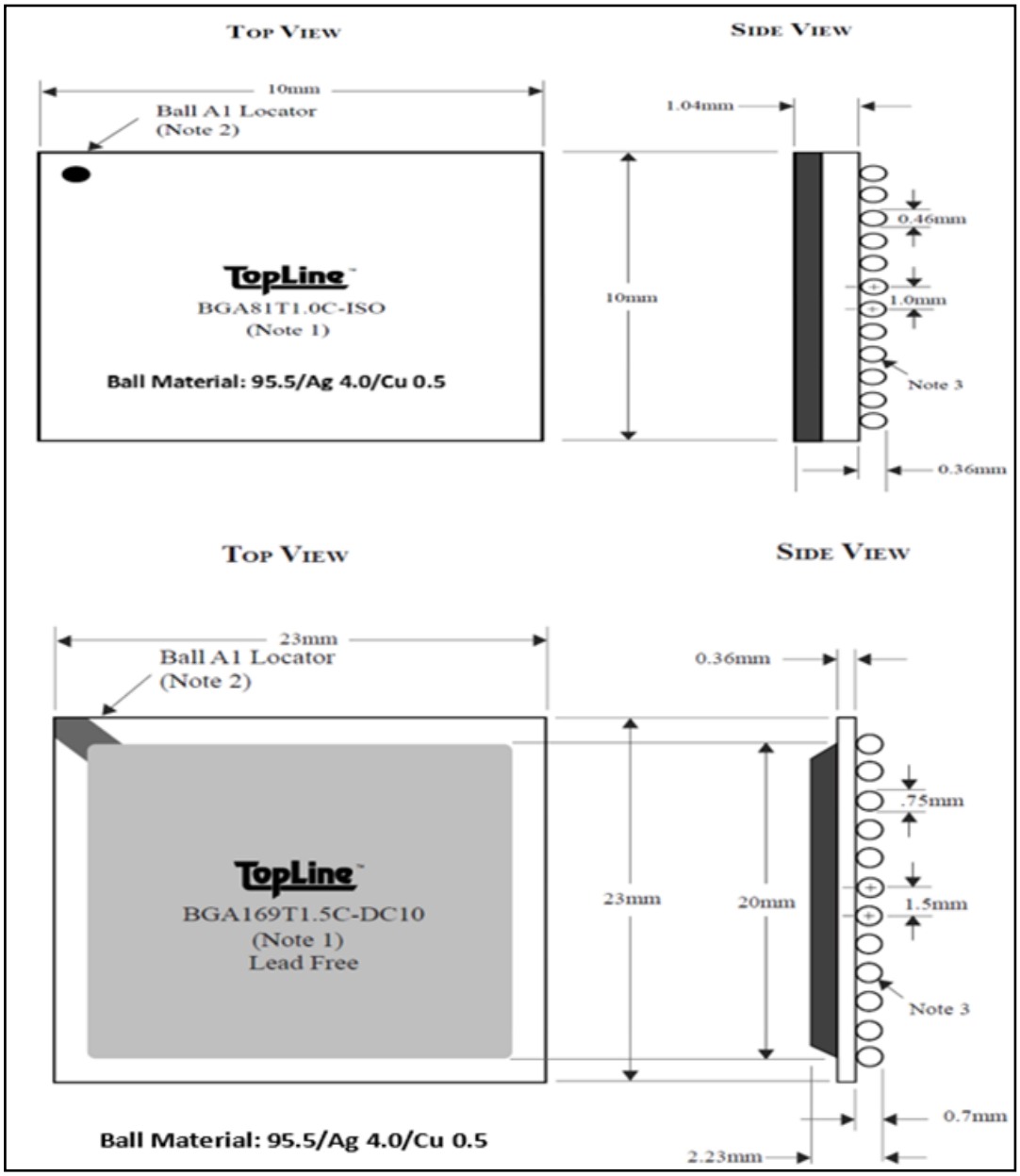


Figure 3.22: Design configurations of BGA81 & 169 top and bottom ball view

SOURCE: [ToplineBGA.com].

3.4 Equipment and Process

This section presents a brief description of the state-of-the-art laboratory equipment, experimental setup and their parameter values used for the investigations in this thesis. In ensuring that the data cum results obtained to comply with the IPC/JEDEC standards, the equipment used is not different from those commonly used in SMT packaging industries. The first set of the equipment includes DEK 260 Stencil Printing machine used when printing solder

paste onto a substrate, Gold-Place L20 Pick and Place (PnP) device used to place components (e.g. chip resistors and BGAs) on boards. The second phase comprises Novastar 2000HT 'Horizontal Convection' reflow oven for the reflow soldering process, ARs-0680 Climatic (Temperature and Humidity) chamber for ‘thermal and isothermal ageing'. The third part includes Struers Accutom-5 precision and Guillotine manual cutting machine, Dage Bond Tester (DEK 4000PXY series) for destructive ‘shear testing'. The final phase includes Struers polishing machine, X-Ray machine for ‘analysis of voids' in solder joints and the Benchtop SEM for evaluation of the microstructure and fracture analyses of solder joints. Figure 3.23 presented a summary of the experimental equipment and processes and described in details afterwards. There was no description of the thermal cycling/vibration chamber, and the Reichert microscope; but the metallographic materials and processes are elaborately dealt with towards the end of this chapter.

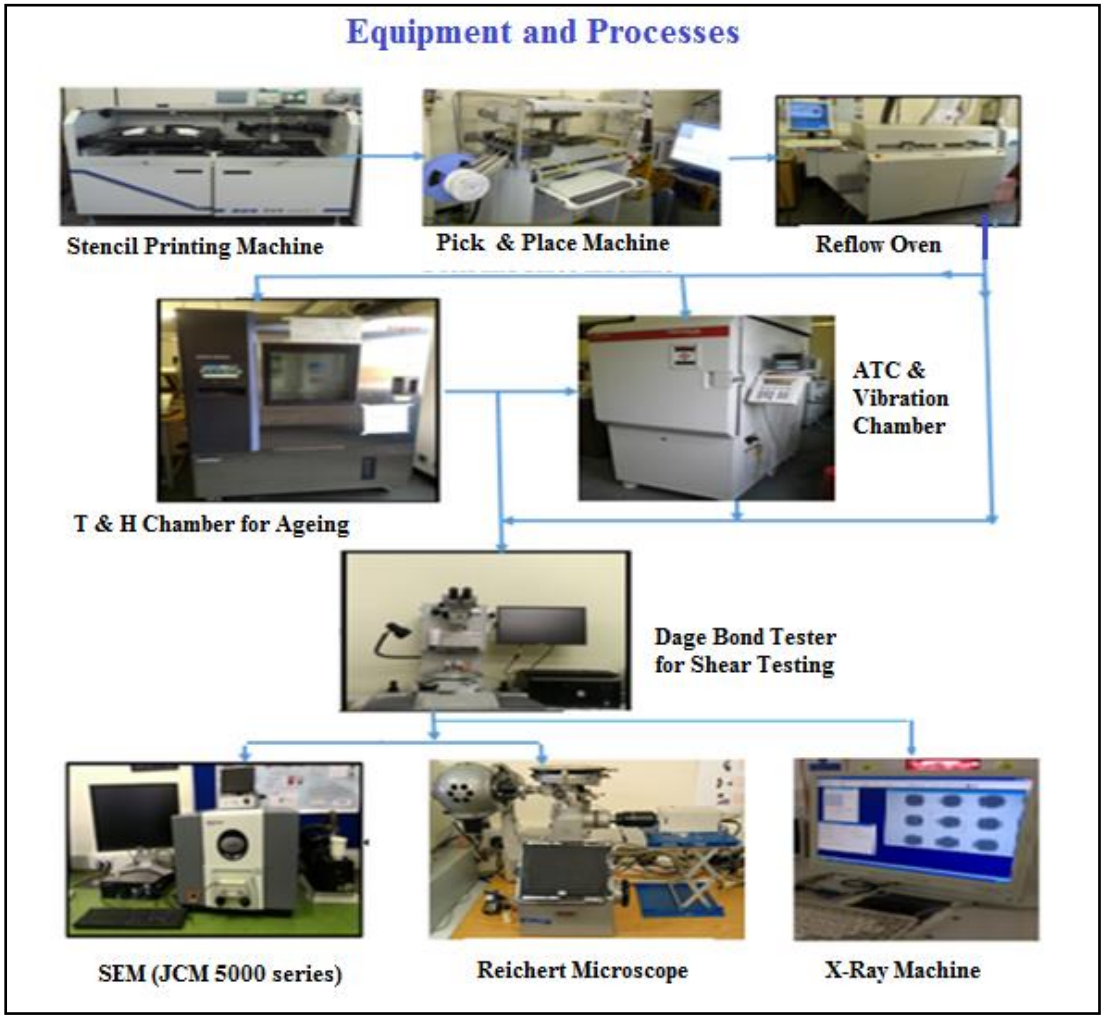


Figure 3.23: Equipment and Processes used in the study

3.4.1 Machine for Stencil Printing of Solder Paste

Stencil printing is a vital step in electronics assembly because an appropriate selection of solder paste volume, stencil aperture and squeegee pressure would contribute substantially to the quality and reliability of the solder joint. Stencil printing of solder paste used in the assembly of chip resistors is one of the critical steps in surface mount manufacturing. This machine works with both metal and the rubber squeegee. The metal (stainless steel) squeegee used for this experiment has an angle of 45°. Other specifications for this machine include the use of semi-automatic standalone screen printer, use of DEK Align 4 vision system with a print area of 440 x 430mm (17, 3'x16, 93'). The maximum board size is 500 x 450mm (16.69'x17.72') and screen frame is 508 x 508mm (20'x20') internal. A programmable control of process variables comes with this machine which ensures accuracy and repeatability in most difficult and busy situation (Mallik et al., 2009; Durairaj et al., 2002).

The printing process involves as previously mentioned a squeegee mechanism, which directly affects the product yield and quality of the final assembly. Moreover, with 'Fine Pitch' technology as today's technology demands, it is more prone to residual defects. However, the majority of the soldering defects encountered after the reflow process include delamination, open/short circuits as well as circuit bridging problems. They are contingencies attributive to defects originating from solder paste disposition process. The solder paste printing is achieved following IPC/JEDEC standard printing process by using Benchmarker II stencil apertures and by appropriately selecting the right choice of (Sn-Ag-Cu) solder paste/volume, substrate selection with appropriate surface finish pad and quality rubber or metal squeegee.

The parameters used in achieving the stencil printing at no or insignificantly little defects are presented in Table 3.4 while the stencil printing machine used throughout the experiments is DEK 260 SERIES as shown in Figure 3.24.

Table 3.4: Stencil printing parameters used

Parameters	Values
Forward Print Pressure	20mm/s
Pressure	8.0kg
Batch count	235 cycles
Vision alignment	0
Print mode	DBL squeegee
Reverse print speed (RPS)	20mm/s
Print stroke	342mm
Inspect rate	0
Separate speed	100%
Print gap	0.0mm

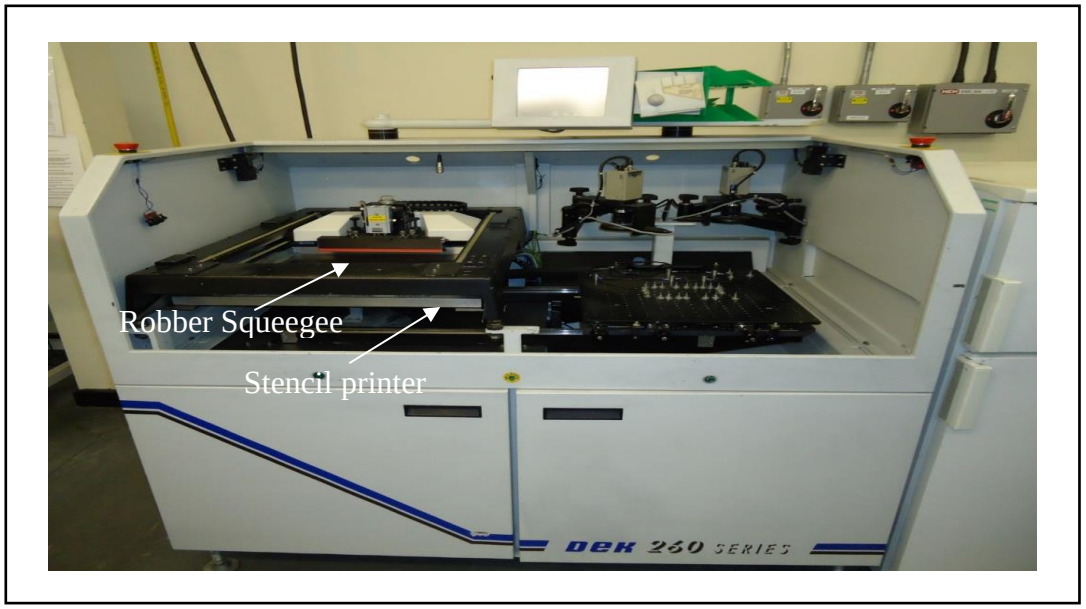


Figure 3.24: Stencil printing machine -DEK 260 series.

3.4.2 The APS Gold-place L20 Pick and Place (PnP) Machine

This equipment was used to place the components onto the PCB terminations or land areas to form test vehicles temporarily before reflow soldering. Solder flux was initially applied onto the PCB surface to hold the materials in position tentatively after being placed by the PnP machine to form the test vehicle as shown in Figure 3.25.

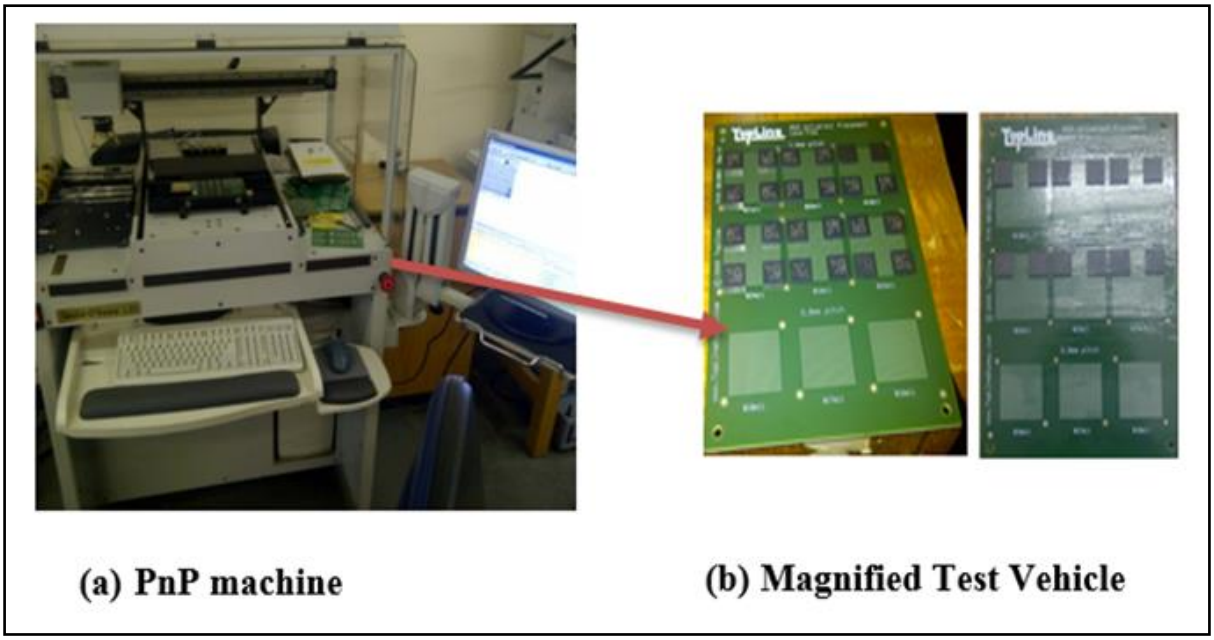


Figure 3.25: (a) PnP machine (b) Enlarged test vehicles after the component placement.

The computer uses the Advanced Planning and Scheduling (APS) software to control the pick and place machine, which was pre-programmed for the printed circuit board and components placement. The programming of the device enables components' mounting lacing with the aid of a vision fitted camera from its tray to the set location on the FR-4 PCB. The machine also uses a vacuum pick up tool to hold the component as it positions in a central squaring and vision-assisted alignment basin before precision placement accomplishment. For test vehicles with BGA81 (designated test vehicle 3a), a total number of five PCBs were used, with four components placed on each pad size (i.e. 19, 20, 21, 22, 23 and 24mil diameters). The various pad dimensions were used to fabricate the test vehicles used for the 'As-soldered' and 'Aged' shear strength test samples and help determine their influence. In the case of test samples for SEM examination, five (5) PCBs were also utilised with only two components placed on each of the pad sizes. The total number of components configured by the PnP machine on each board for the shear strength and SEM test samples were twenty-four (24) and twelve (12) 'components' respectively. However, for test vehicle with BGA169 (designated test vehicle 3b), a total of forty-eight (48) components were placed, two (2) components per board on sixteen (16) boards (PCBs) for SnSF pads and eight (8) boards for CuSF pads which represent test vehicle 3c. In all, one-half was used for 'as-soldered' while the other for 'Isothermal ageing'.

3.4.3 Convection Reflow Oven for the Reflow Soldering Process

The Novastar (2000HT horizontal) convection oven was used for the reflow soldering process. The method includes conveying the test vehicle (substrate with components already placed on it) through an oven with successive heating elements of varying temperatures. In the oven, each board typically goes through the stages of gradual pre-heating, brief duration at high soldering temperature ramp, controlled collapse (occurring at liquidus temperatures), and cooling process. This process lasted for about seven to eight minutes where the samples had to cross the six different heating zones and one cooling zone of the oven, each of them having their set temperature according to the set reflow profile. Soldering temperatures require appropriate temperature profiles for a given experimental design. The Novastar model is a production scale reflow soldering machine type, which operates on a forced convection heating system using heating elements, which can attain a maximum temperature range of 350 °C for each of the heating zones. The PCB test vehicle passes through the furnace of the reflow oven via an 1829 mm long conveyor belt system, whose speed is adjustable between 0.05 to 0.99 m/min. Figure 3.26 shows a reflow oven in which components were reflow-soldered. Once the reflow process was completed, three substrates are separated for isothermal ageing. The two substrates left were kept for the shear strength test, which is next in the discussion.

Figure 3.26: Convection reflow oven for components soldering.

3.4.3.1 Temperature Profile Used for the Reflow Soldering

The peak reflow temperature for the chip resistors solder joint was kept at around 245 ºC as shown in Figure 3.27. This step allowed the solder to melt and form the joint. The Ramp-To-Spike (RTS) reflow profile was used because of the uniform heating of the test vehicle, thereby ensuring that the thermal profile increase continuously along preheats and soak regions up to the peak temperature, before cooling down rapidly. The reflow duration was set at 8 minutes. Another purpose of the reflow profile was to enable the heating of the solder- alloy material to a temperature which is a little above the melting point of the alloy to allow soldering of the BGA or chip resistor solder balls/alloy onto the substrates to establish mechanical and electrical bonding of the assembly. Care is taken (following the optimisation process described in chapter four of this thesis) not to use temperature profiles which could totally melt the solder alloy causing it to flow and cause circuit bridging across the boards.

For the effect of CSH verification of BGA81.1.0T1.ISO component using 19-24 mil pad size variation (Test Vehicle 3a), a Ramp-to-spike reflow profile peak temperatures of 235°C was used. The peak temperature profiles of 225°C, 235°C, 245°C, and 255°C were used to verify the effect of BGA169.1.5T1.ISO CSH under temperature variation (Test vehicle 3b), both with a tolerance level of $\pm 5^0$C. The RTS profile has the further advantage of producing brighter and shiner joints that have lesser solderability problems due to the availability of flux vehicle in the solder paste during the preheat stage of the reflow process. The utilisation of peak temperature variation at various and critical stages of reflow allows the component resistors cum BGAs solder joints approach their dissolution state, dissolve and metallise to form a joint with the Cu base metals. The soldering process comprised the following reflow stages:

- **Pre-heating stage** - The Pre-heat stage is the point when the solder particles heat up before getting to their melting point level.
- **Activation stage** - Activation stage is the stage when the oxides in the flux evaporate.
- **Reflow stage** - The Reflow stage is the stage when the flux reaches its melting point at liquidus temperature.
- **Cooling stage** - The Cooling stage is the point when the samples cool down at a ramp-down rate.

Figure 3.4 and Figure 3.16 discussed earlier in this chapter present the experimentation process and equipment. The display of the RTS profile employed in this study is in Figure 3.27. The

reflow temperature profiles for the BGA test vehicle 3a and 3b are presented in Figure 3.28 and Figure 3.29.

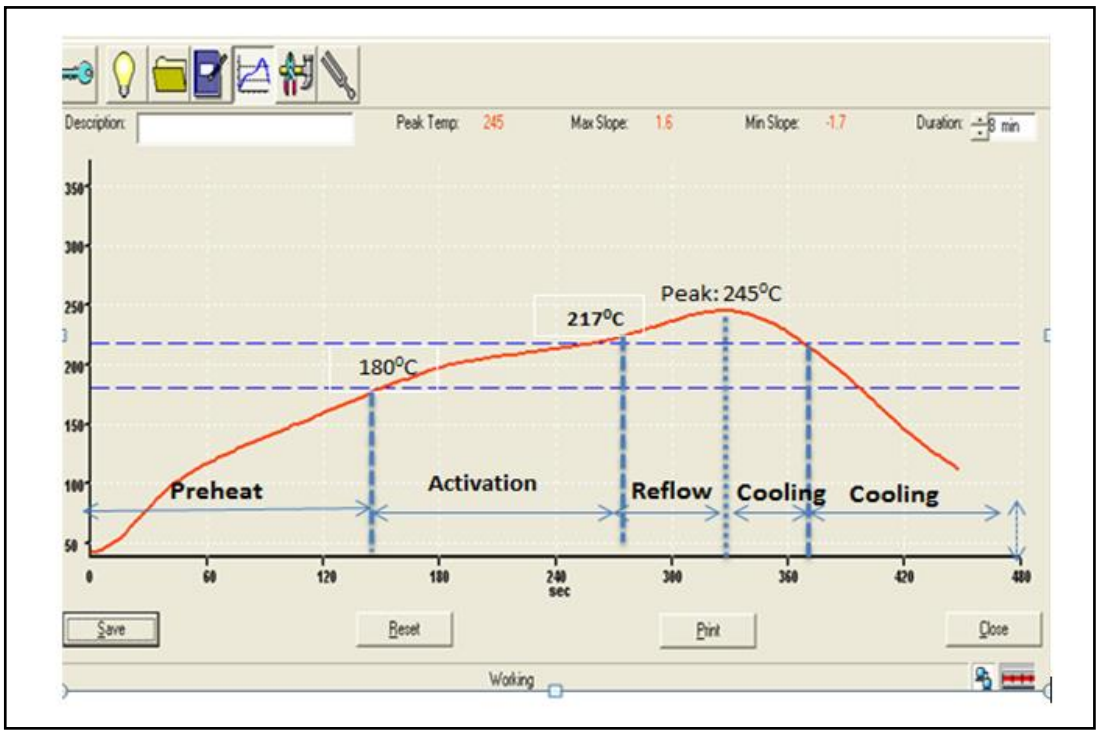


Figure 3.27: Sample of the chip resistors reflow profile

Figure 3.28: Reflow profile for test vehicle 3a

Figure 3.29: Reflow profile for test vehicle 3b

3.4.4 Climatic Chamber for Isothermal Ageing

Isothermal ageing of part of the test vehicles (for ageing temperature) was carried out in a Temperature and Humidity Chamber of the model (Espec ARS0680) with dimensions W1050×H1955×D1805. It has a programmable control unit to set the required temperature range in Celsius and time in hours. The control unit has a touch screen user Interface with which input was given to establish the parameters for the ageing process. The isothermal ageing process used involved placing three substrates of the test samples in the chamber, setting the control unit for 250 hours at 150 ^{0}C and saving it for all the components. The programme then ran to perform the process. Through the interface application of the chamber during process operation, and after every 24 hours the humidity level was continuously monitored and checked. The device application chamber switched off automatically after 250 hours of operation, and the samples removed from the hot enclosure for further analysis. The photograph of the climatic chamber is presented in Figure 3.30 (a-c).

Figure 3.30: (a) Temperature and Humidity chamber, (b) Programmable screen user interface and (c) Samples inside the chamber

3.4.5 Dage Bond Tester (DEK 4000PXY Series) for Test & Measurement

The Multipurpose 4000 series Dage Bond Tester is capable of performing all pull and shear test applications. The tester configuration functions as a simple wire pull tester, which is upgraded to provide ball shear, die shear, and bump pull tests. The equipment uses frictionless load cartridges and air bearing technologies, which ensure maximum accuracy, repeatability and reproducibility. The cartridges are designed for different applications and are readily exchanged to match a chosen operation. The cartridge also function as automated device with sophisticated electronic and software controls.

The test specimens were held in position within a sizeable fixture before the components were sheared at standard shear speed and shear height of 200µm/s and 60 µm for BGAs and 30µm for the chip-size resistors respectively. This equipment was used in this work to obtain the shear force required for the destructive shear tests on solder joints of BGAs and the components

of the chip-size resistors. It was also used to verify the integrity of the soldered assembly by using the set parameters in controlling the shear tool when shearing the SMD components from the substrate through the solder joints.

Dage bond tester mechanism involves the use of micro force to shear a soldered joint on the printed circuit board permanently; by so doing, the strength of the solder joint obtained reports and records on the screen. The overall aim of this task was to measure shear strength of solder joints for each component type at a designated or varying shear speeds. The Dage Bond tester is illustrated in Figure 3.31, and the enlarged form of the test vice, shear tool cartridge and shear tool position on test vehicle during shear testing is presented in Figure 3.32(a-b); while the process steps for the shear test are outlined in section 3.4.5.1 respectively.

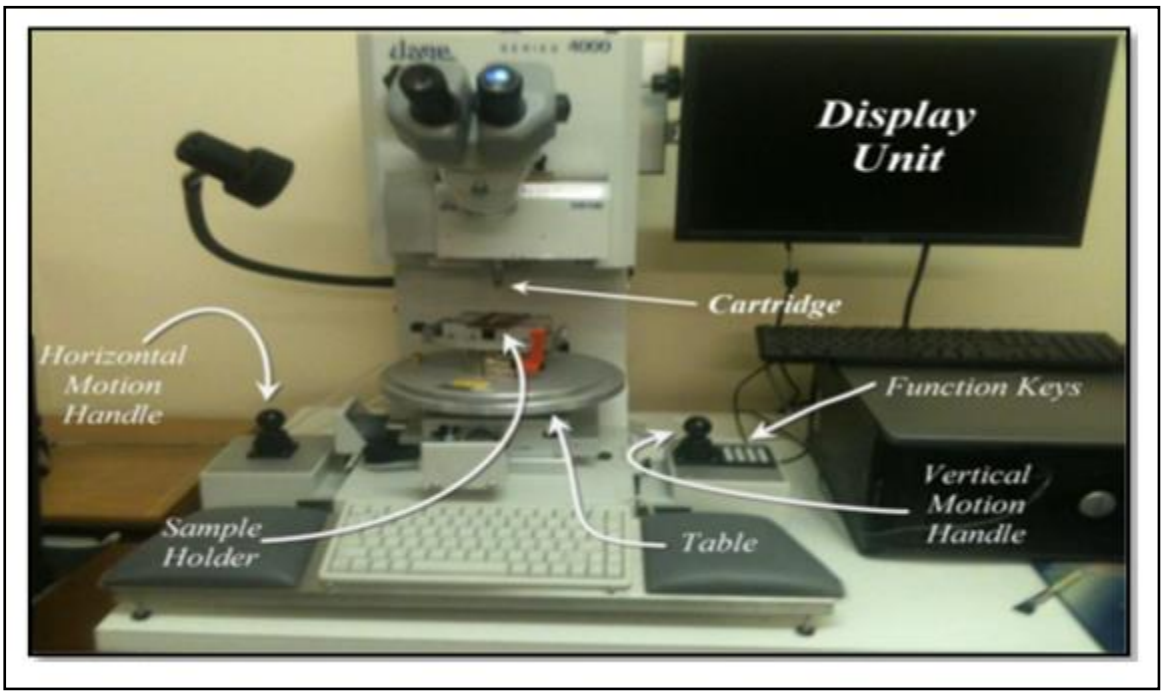


Figure 3.31: Dage Series 4000, Shear Testing Machine.

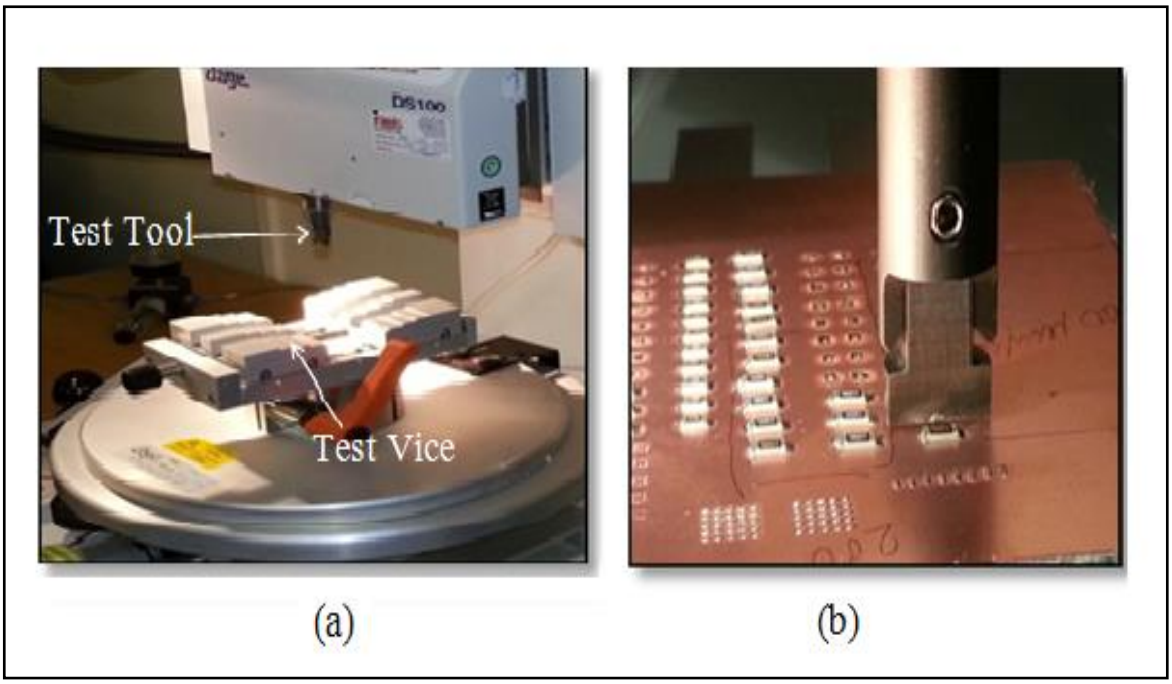


Figure 3.32: (a) Shear tool/sample holder (b) Shear testing position.

3.4.5.1 Process Steps Used in Shear Test and Data Collection

The process steps involve cutting the substrate into the right shape that can fit into the vice by removing the unwanted parts, and then apply shear force on each of the components as shown in Figure 3.33; with shear height and shear direction clearly indicated. The detailed steps are as follows:

- The hard board has to be trimmed and made of right shape so that they could fit into the test 'Vice' of the Dage Bond Tester.
- After fixing and tightening the substrates correctly on the test vice, the shear test is performed by applying shear force via the tool of the tester at different shear speeds.
- The shear heights are set at 30µm for a resistor and 60µm for a BGA solder joint. The shear height is the distance between the tool and the surface of the substrate.

Shear force values for each component was noted, and results were accordingly tabulated and categorised as there had to be segregation in the results for aged and non-aged samples respectively.

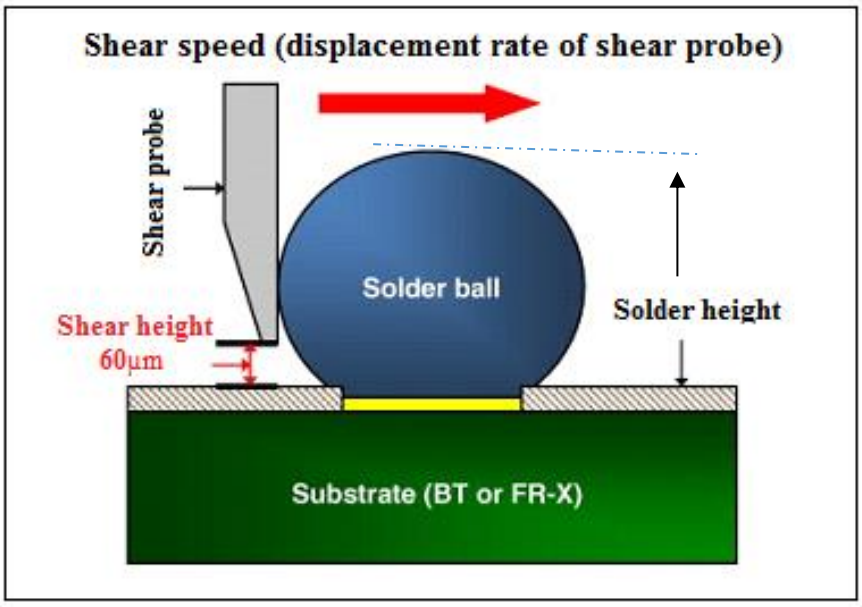


Figure 3.33 The schematic showing shear height and test direction of BGA solder ball

3.5 Precision Cutting of Samples for Metallography Preparation

The aim of this task was to prepare the test samples for further analysis using an image capture so that both the fractured and the non-fractured but cross-sectioned surfaces could be examined and analysed. PCBs of selected samples from the as-reflowed and the isothermally aged test vehicles were cut to size with manual guillotine machine and then cross-sectioned using the 'Struers Accutom-5' precision cutting machine. The assemblies along the centre path of the solder joint are sectioned in such a manner that the solder joint becomes revealed, enabling the microstructure analyses. Then, CSH and IMC measurements are carried out for as-soldered and aged samples using Scanning Electron Microscopy examination (SEM). The measurements are done after the metallographic phase of the laboratory experiment. The SEM preparatory task processes for the Chip Resistors solder joints test is presented in Figure 3.34 (a-d), while the precision cutter with the individual BGA solder joints strips are in Figure 3.35.

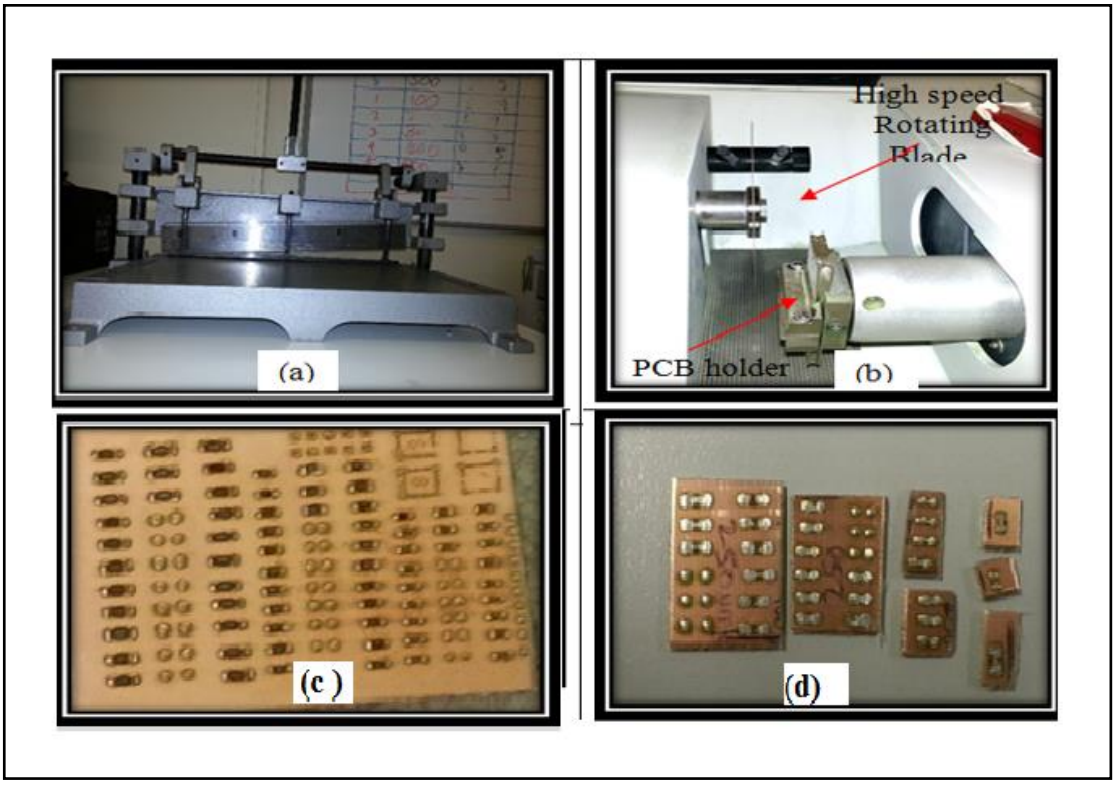


Figure 3.34: (a-b) Manual and precision cutter, (c-d) Test vehicle and sliced PCB

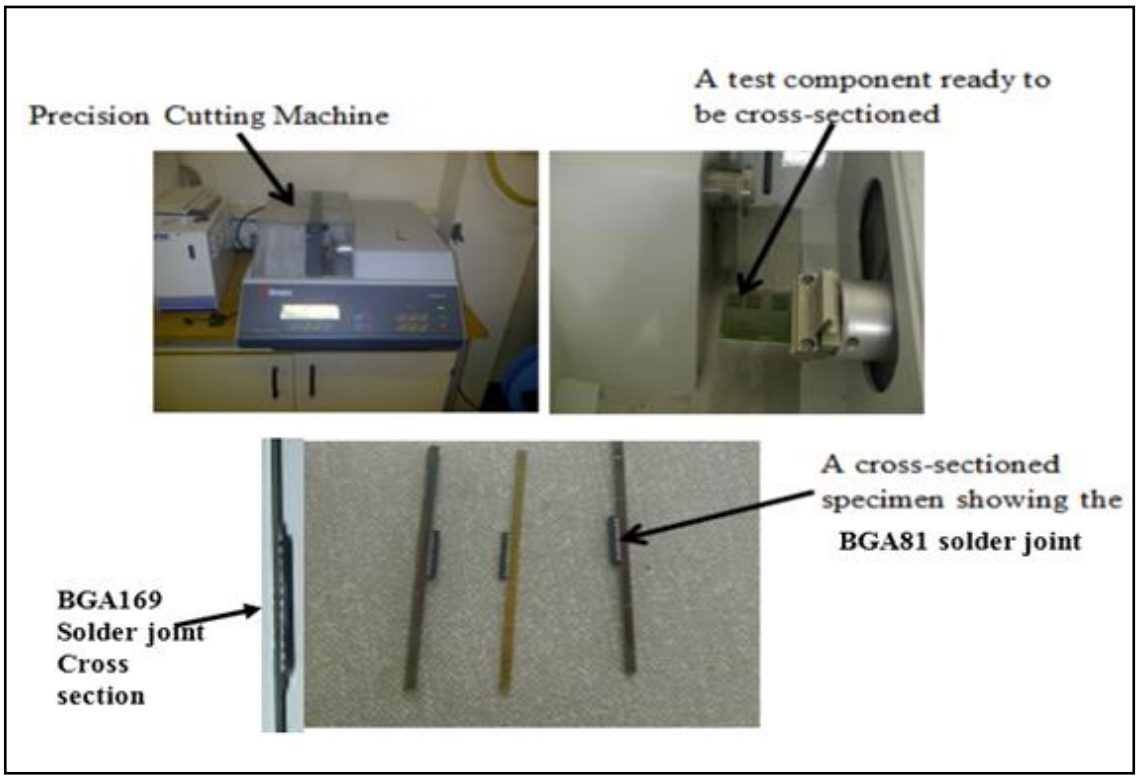


Figure 3.35: Precision Cutter & strips of cross-sectioned BGA components

3.5.1 Metallography Preparation

In preparation for the CSH as well as IMC measurements and microstructure study of the sectioned solder assemblies, the sectioned strips of the test vehicles were moulded using conductive Bakelite powder described in section 3.3.5.1 which are conductive materials and which allows the flow of electrons in the Mould while using the SEM. To remove roughness from the surface of the moulded test vehicles and to enable better quality view on the SEM, the surface was polished using the roll grinder and surface polisher. The equipment (or machines) for this study and their methodologies are discussed in the next sections.

3.5.2 The Buehler Compression Mounting Press

The Buehler compression machine produces the Mould after a period of about ten minutes of operation. This device operated pneumatically or assisted in making test samples for metallurgical moulds before carrying out the electron microscopy investigation. The test samples were initially placed on top of clean ram on the machine before mounting them on the Mould, (with the solder joints side facing downward) and before being released into the machine using a ram control. A measured quantity of standardised two and a half cup of Bakelite powder was poured directly into a space above the test specimen for moulding. The moulding chamber was air tightened and subjected to high pressure by covering it with a plunger before switching the machine on. The Ram control was pushed up at this point to build up pressure within the moulding chamber. This process was de-gasified after about five minutes of running, by pulling down the Ram control to release some built-in air or gases that might interfere with the moulding process. A photograph of the mould-making process using the already described Bakelite powder is in Figure 3.36.

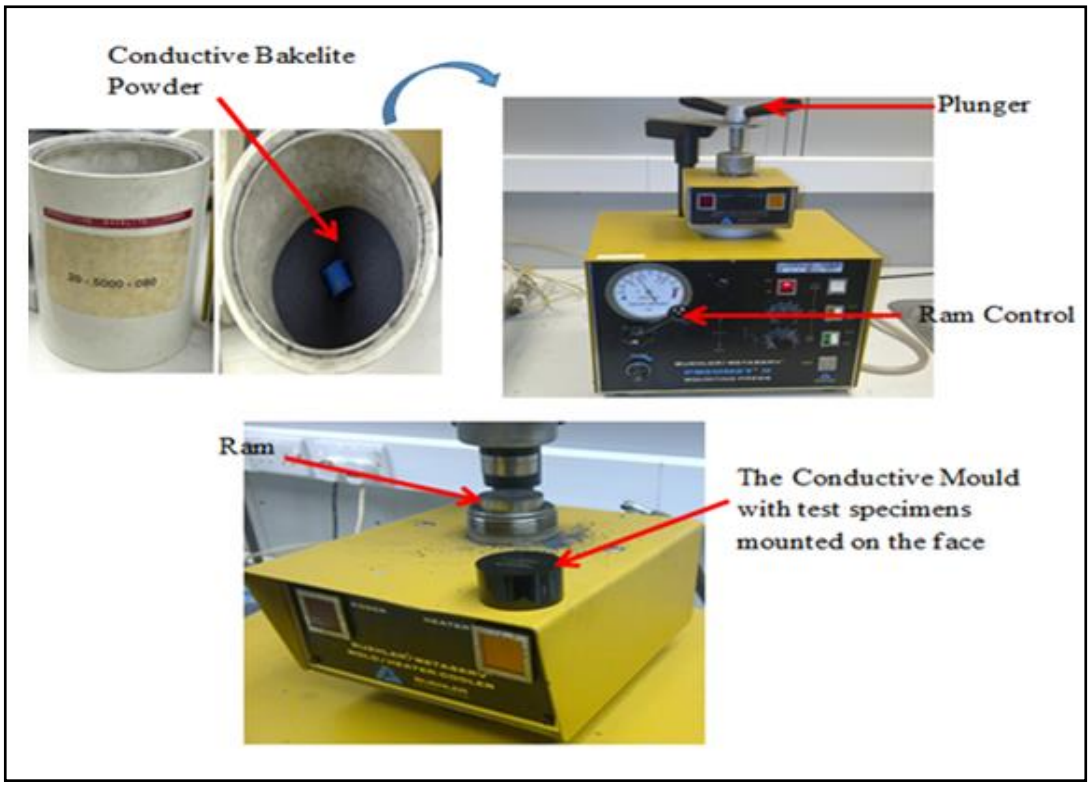


Figure 3.36: Images displaying the mould-making process
Source: [UoG-2015]

3.5.3 The Buehler Abrasive Paper Rolls

The Buehler equipment has four different abrasive rolls as shown in Figure 3.37, each of which has different surface finishes of 240, 320, 400 and 600grits respectively. The purpose of applying this equipment is to reduce the surface roughness of the moulded sample by polishing it consecutively on each of the paper rolls. The duration of time spent on the 240 grit is dependent on the surface roughness of the sample before proceeding to the other rolls having finer surface finishes. The surface texture of the abrasive paper rolls is finer, as it progresses from the 240-grit roll to the 600-grit roll. The face of the moulded sample showing the solder joints was hand polished by moving it haphazardly on the surface of the various abrasive paper rolls.

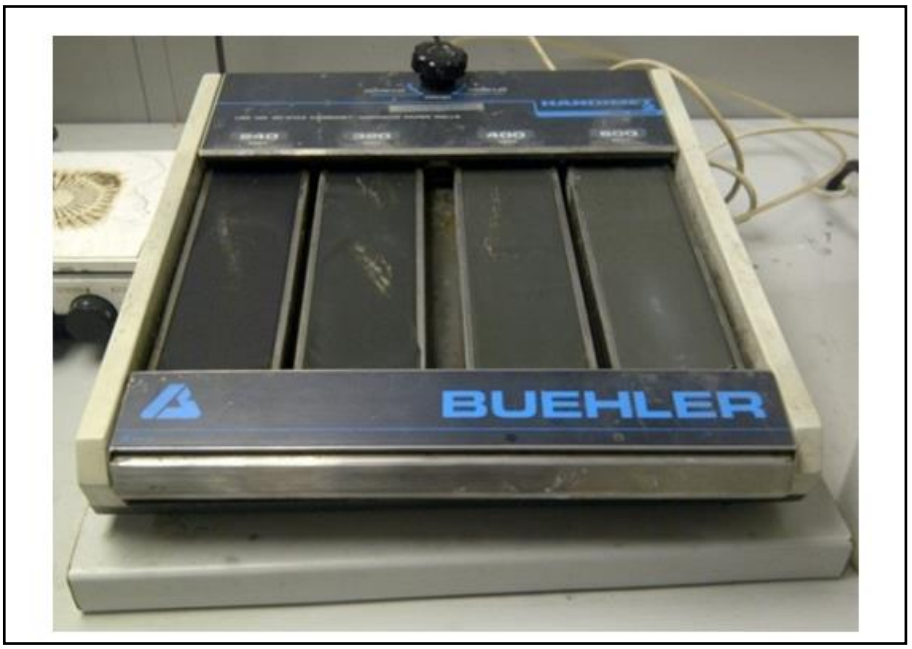


Figure 3.37: Image of abrasive paper rolls

Source: [UoG-2015]

3.5.4 Metaserv 2000 Grinder/Polisher

The final phase of the metallographic preparation of test specimens was conducted using this equipment. The grinding machine consists of two chambers, operated simultaneously depending on the kind of Monocrystalline Diamond Suspension (MDS) in use. For the purpose of this chapter, both grinding chambers were utilised owing to the use of two different monocrystalline diamond suspensions (6µm and 1µm) respectively. Once the equipment is switched on, the diamond suspensions were applied directly onto the moving Grinder (rough stone) before the moulded specimen was held firmly by the hand and placed in a stationary position while it spins and polishes with the suspensions, the surface to be examined. The 6µm suspension was applied firstly onto the first grinder before the application of the 1µm suspension onto the second grinder (Figure 3.38).The test specimen was washed properly with water after the first grinding before proceeding to the second grinder. This process provides a chemo-mechanical polishing (CMP) action on the surface of the specimens, which significantly increases removal rates of foreign particles or grains, reduces subsurface damage as well as improves the surface finish of test specimens for efficient electron microscopy examination.

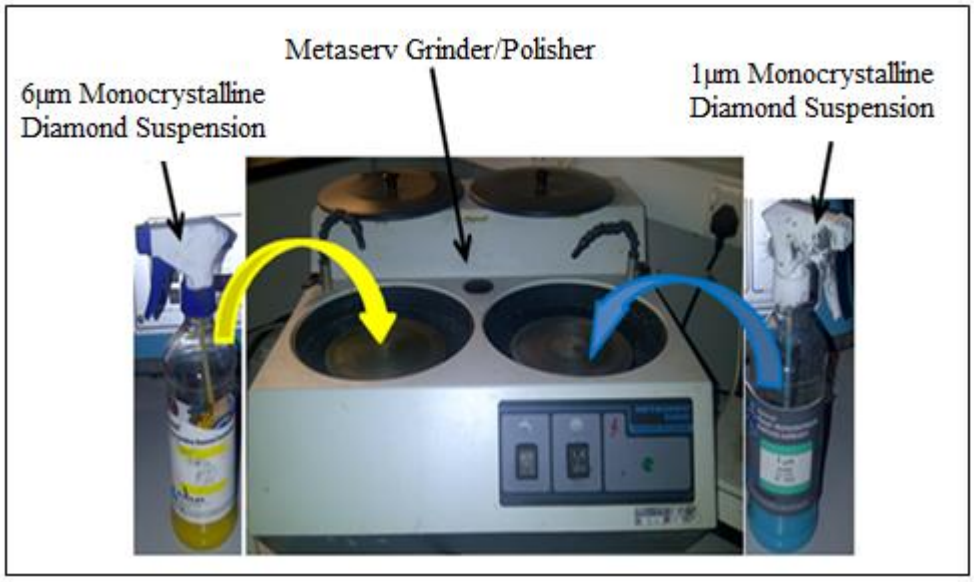


Figure 3.38: Metaserv 2000 grinder with polisher and MDS

Source: [UoG-2015]

3.6 Benchtop SEM for Fracture Analysis

The fractured surfaces of the components solder joints are investigated for both brittle and ductile fractures under a SEM. This SEM operates at a high magnification level of 10kV with a focused beam of electrons injected from an electron gun filament that produces images of a sample by scanning it. The injected electrons interact with atoms in the sample, thereby producing various visible signals. These cover information about the sample's surface topography and composition. Moreover, the atoms excited by the electron beam thus emit secondary electrons. Other forms of particles originating from the electron beam are the Back-Scattered-Electrons (BSE), which consist of high-energy electrons that arising from reflected or backscattered specimen volume interaction with specimen atoms. This equipment use was specifically for its high-powered capability of measuring and examining the CSH and the failure mode of solder joints. Figure 3.39 shows (a) the JEOL5000 series Neoscope Benchtop SEM used for the fracture surface analysis and (b) the internal structure showing specimen platform and its adjustable tray. The process steps used in achieving the SEM analysis is outlined in section 3.6.1, and a photograph of the JEOL Neoscope process analysis steps with appropriate labels is presented in Figure 3.40.

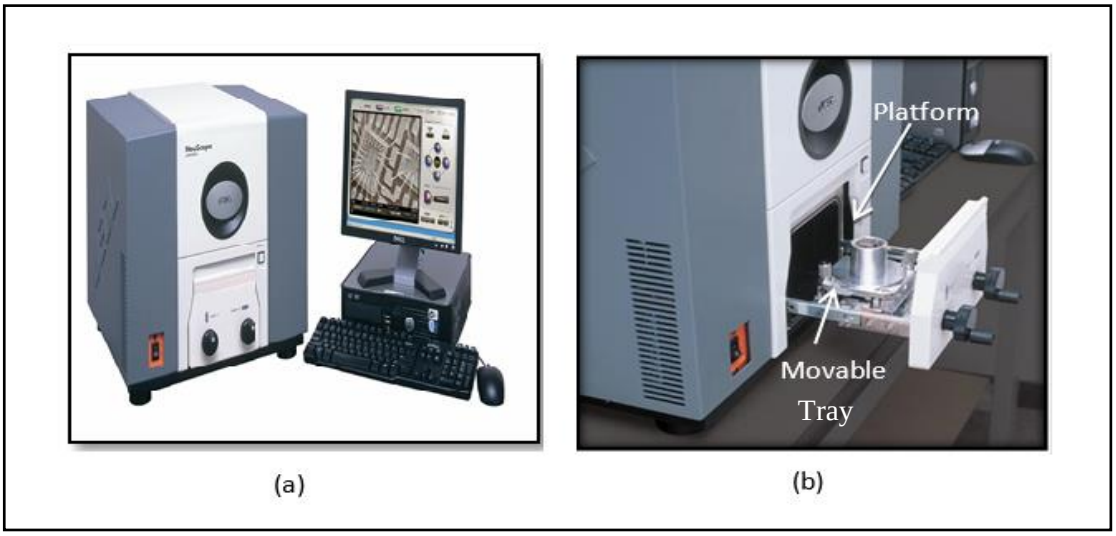


Figure 3.39: (a) JEOL Neo-Scope Benchtop SEM and (b) SEM internal structure.

3.6.1 Process Steps Used in SEM Analysis

Fractured surfaces of each component assembly (only the substrate sides) were observed, and compelling images were taken to support the further explanation. Slicing of the PCB was required because SEM has a limited viewing space inside its chamber to accommodate the sample. The following steps were followed:

- The PCB has to be trimmed into smaller pieces by using the metal board cutter known as Guillotine. Sliced parts having solder pad are placed on the observatory platform in the SEM chamber.

- Once the placement was done, the door of the environmental chamber is closed. The door is pushed tightly for a few seconds to activate the vacuum pump to create enough pressure to hold the tray in position.

- The settings of the image for clearer vision are completed by adjusting the object's position, brightness, sharpness and contrast to get the clearest possible image of the fractured surfaces.

- Four images from each solder pad were captured. The type R1206 and R0805 pictures were taken at 50X and 220X magnification, whereas type R0603, which has the smallest image was captured at 70X and 220X.

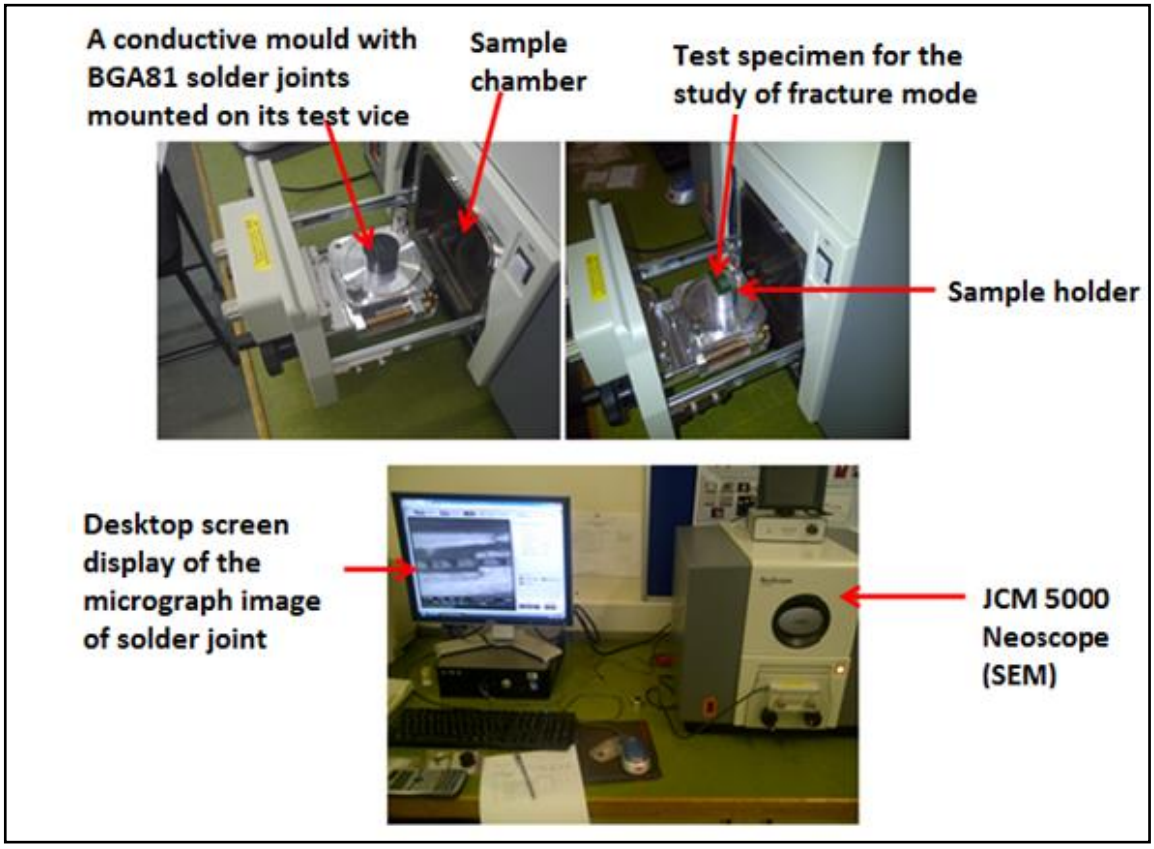


Figure 3.40: Images displaying the SEM process analysis step

Source: [UoG-2015]

3.7 X-ray Machine and Void Detection

The X-Ray machine shown in Figure 3.41 helps to determine the percentage of voids in the BGA solder joints. In the high-resolution X-ray source, electrons accelerate from the cathode with speed close to that of light. The electrons, through a magnetic lens, are focused to a minuscule point on a metal target. On the impact on the target of an atom, electron loses energy through a series of collisions. A small part of the interaction produces X-ray, of which most of the heat dissipate from the target material. In the x-ray source from the set parameters used in this investigation, electrons emitted from a fine wire accelerate up to 225 thousand volts (Charles Jr and Beck, 2007). The position of voids in the various solder joints are visibly observed, via the high-resolution beam. The X-ray systems are also used to determine the volume of each void and its percentage in the joint. The percentage is used to characterise the joint's pass or fail category. To make certain, same measurement conditions were applied to

all samples, some of the parameters are kept constant. Name and value of these parameters are presented in Table 3.5 while the X-ray visualisation is in Figure 3.42.

The visualisation, however, represented the result of the experiment on a test vehicle. Among these are (1) void edge threshold used to define the boundary of individual voids, (2) maximum total voiding is the upper limit of allowed void percentage in any solder bump and (3) maximum single voiding set the limit on the size of any single void in a solder bump. A solder bump will only ‘Pass' if it satisfies these three parameter values.

Figure 3.41: X-Ray machine for BGA voids analysis examined

Table 3.5: X-Ray machine-parameter setting for the lab experiment on BGA voids

Parameters	**Values**
BGA Ball Size 13x13 matrix array,	0.76D, 1.5pd
Ball Edge Threshold	88
Maximum Compactness	2.50
Ball Diameter	Auto
Tolerance	10%
Ball	16×4 (For four corners)

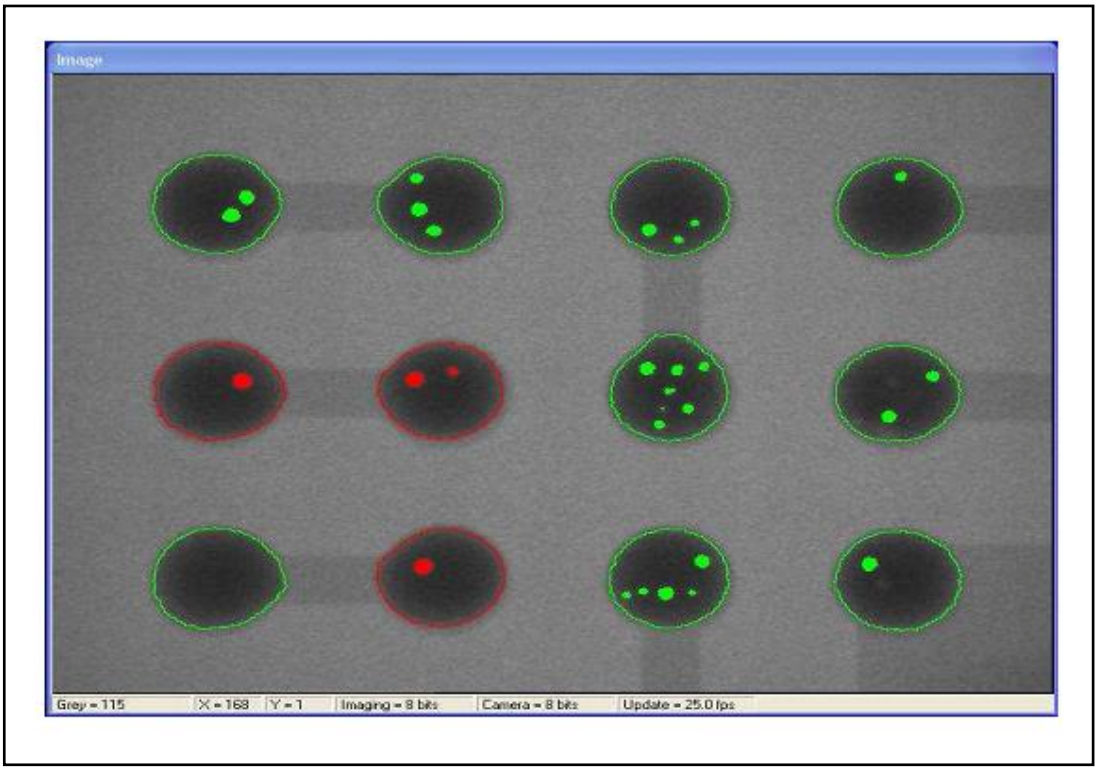


Figure 3.42: Sample of BGA solder bump X-ray visualisation.

3.8 Data Analysis

After conducting the experiments using the chosen DoE, and obtaining the respective results from the five critical experiments carried out and reported in five different chapters in this thesis, the data was analysed and compared with the expected results, most of which are from literature. After observations and analysis of the results, recommendations were made. Also, conclusions on each of the experimental test outcomes were drawn and they are summarised in each of the respective chapters.

3.9 Chapter Summary

An overview of the experimental methodology, equipment and materials utilised in the study reported in this thesis is presented. It includes a description of the test vehicles used and elaborates the novel equipment, materials and procedure employed in achieving the results presented and analysed in this research work. The chapter also covers the manufacturing process of solder joints stencil printing, the reflow profile for the formation of solder joints, and the thermal ageing processes used in the study respectively. It also describes the metallographic preparation of test samples for the measurement of CSH and IMC, and for the microstructural analysis of the joints after the destructive shear test and micro sectioning of test samples were achieved. The required optimal CSH for a reliable solder joint is accomplished through an optimal reflow parameter setting obtained from numerous trial 'tests'. Several other obtained results have their conclusions drawn from their data analysis and examination presented in each of the experimental chapters found in this thesis. The effect of reflow profile parameters setting on the shear strength of solder joints' in SMT chip size resistors assembly is provided in the next chapter.

Chapter 4: Study on Effect of Reflow Profile Parameter Setting on Shear Strength of Solder Joints in Surface Mount Chip Resistor Assembly

4.1 Introduction

Thermomechanical reliability of lead-free solder joints in SMCs depends to a huge extent on the structural integrity and shear strength of the joints (Wang, Dutta and Majumdar, 2006; Zhao et al., 2000). It has been widely demonstrated that the shear strength of solder joints (SJs), in turn, depends (to a large extent) on the reflow profile used in forming the joints (Pan et al., 2006; Tsai, 2012). The shear strength of solder joint is considered in this investigation because the researcher found in his literature review that shear strength influences the reliability of SJs more than any other strength measuring methods. In specific terms, it measures the shock/impact strength better than their axial or compressive loading. Electronic devices knowingly fall from heights now-and-then, and thus experience mechanical shock and impact load. It is also imperative to consider the effect of thermal shock on the strength of solder joints. Webster et al. (Webster, Pan and Toleno, 2007) reported on the effect of thermal shock on the solder joint shear strength; and recommended for used when evaluating the integrity of solder joints.

In the electronics manufacturing industry, convection reflow soldering has been an essential soldering process. The strength of solder joints depends significantly on the reflow profile used during the assembly of components on the substrate using solder paste (Lee, 2006). In addition to determining the strength and integrity of solder joints, the reflow profile determines the degree of defects, which occurs during component reflow assembly. These defects include but are not limited to tombstoning, cracking, cold joints, excessive intermetallic formation, bridging, poor wetting and solder balling. The reference (Lee, 2002) reported that improper reflow profile setting parameters are the primary cause of these defects in electronic assembly. In specifics, Beddingfield and Higgins (Beddingfield and Higgins, 1998) reported that the popcorn defect which occurs in solder joints is due to improper reflow profile. The reflow profile is determined by the settings of the different reflow stages of the reflow process. The stage parameters settings control the nature of these steps. These settings determine the shape, microstructure and the strength of the solder joints (Harrison, Vincent and Steen, 2001). The settings due to surface tension can also affect the solderability and wettability of the solder joint during reflow soldering as defined in Chapter 2, sections 2.7.4.4 and 2.7.4.5 respectively.

A typical ramp-to-spike reflow profile is shown in Figure 4.1. The critical process stages consist of the preheating slope, TAL, peak temperature and cooling rate. The peak temperature of lead-free reflow profile for solder bumps on the FR4 substrate was found to be a significant

parameter that determines the thickness of the intermetallic compound layer and microstructure quality (Salam et al., 2004). The soldering parameters that influenced the mechanical bonding of solder were selected, and their values varied to determine their impact on the joint's strength. The determination of their impact on solder joint strength has become crucial in consideration that the integrity of solder joints has become increasingly critical owing to current electronics components and device miniaturisation trend. The decrease in the size of electronic devices and components has forced the SJs in these elements also to reduce significantly - thus resulting in the increase in concern about their joints strength.

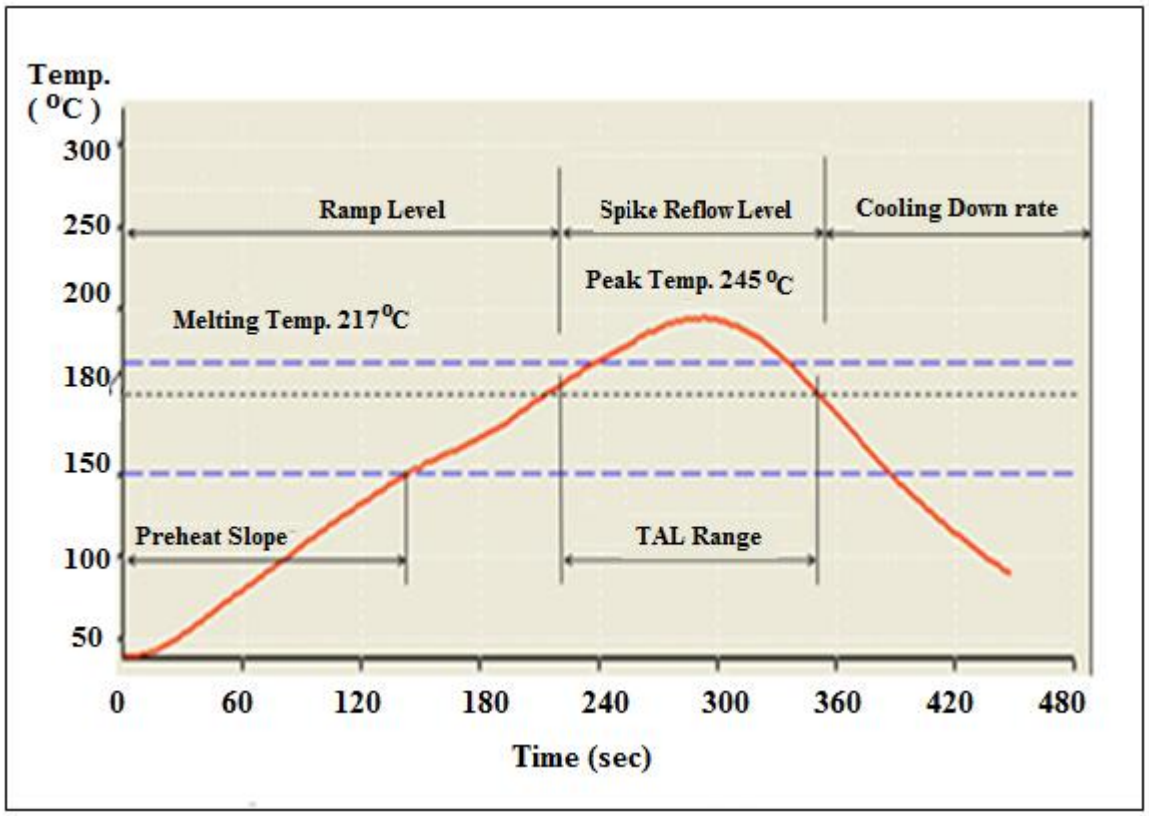


Figure 4.1: Ramp-To-Spike Reflow Profile

4.2 Research Design and Experimental Details

This chapter presents an investigation which seeks to determine the effect of reflow profile parameter setting on the strength of solder joints in surface mount resistor assembly amidst the miniaturisation manufacturing trend. The objectives of the investigation include but are not limited to:

- Generate experimental designs, using the design of experiment (DoE), in which the values of the reflow parameters are varied to determine their effect on the strength of solder joints formed using each of the resulting profile.
- Use three different sizes of surface mount resistors assembled on PCBs as the test vehicles to produce solder joints of different sizes that their study will inform on the effect of miniaturisation on solder joint integrity.

To investigate the aim and objectives of the research presented in this chapter, Taguchi design of experiment was employed. The adequacy of employment of design of the experiment and in particular the Taguchi design as earlier discussed has been widely reported (Theodore F Bogart, Jeffrey Beasley, 2013; Amalu et al., 2015). The factors and the parameter investigated in the reflow profile are the preheat slope, time above liquidus, peak temperature and cooling rate. Two levels of these four factors are selected and used in the design. The design is thus a four factor on two level, $L2^4$. The experimental parameters and their levels utilised for the study are shown in Table 4.1 while Table 4.2 presents the eight orthogonal array design points. A detailed description of the vehicle is given in Figure 3.5, section 3.2.4.

Table 4.1: Experimental parameters and their levels

Factors/factors	Levels	
	High (2)	Low (1)
A= Preheat Slope	1.2°C/sec	1.0°C/sec
B= Time above Liquidus	60secs	45secs
C = Peak Temperature	245°C	230°C
D = Cooling Rate	100%	60%

Table 4.2: Eight design points using the Taguchi DoE

Design Point no.	Preheat Slope (°C/ sec) [A]	Time Above Liquidus (sec) [B]	Peak Temperature (°C) [C]	Cooling Rate (%) [D]
1	2 (1.2)	2 (60)	2 (245)	2 (100)
2	2 (1.2)	2 (60)	1 (230)	1 (60)
3	2 (1.2)	1 (45)	2 (245)	1 (60)
4	2 (1.2)	1 (45)	1 (230)	2 (100)
5	1 (1.0)	2 (60)	2 (245)	1 (60)
6	1 (1.0)	2 (60)	1 (230)	2 (100)
7	1 (1.0)	1 (45)	2 (245)	2 (100)
8	1(1.0)	1(45)	1(230)	1(60)

4.3 Results and Discussion

The general results of the investigation presented in Tables 4.3 and 4.4, and Figure 4.4 to 4.7 respectively are discussed. Table 4.3 presents the main experiment, which shows the average IMC thickness and shear force for each design point number across the different sizes of the test vehicles, while Table 4.4 shows the shear strength equivalence of the shear forces. The shear strengths were calculated using ($1.55x10^{-6}$, $1.0x10^{-6}$ and $0.48x10^{-6}$) which are the measured shear/cross-sectional area of the respective component resistors employed in the study. Additionally, the table demonstrates that design point 3 and 5 showed the extreme shear strength of solder joint. While design point number 3 has the highest shear strength, design point number 5 has the least shear strength. Thus, these are the critical models representing the best and worst designs, respectively. To have a better understanding of the distribution of the shear strength, the joints microstructures are one of the important models examined. Table 4.5 presents the micrographs, which show the microstructure of the vertical cross sections of these designs. The microstructure of the solder joints depends on the interfacial reaction between the substrate and solder. Also, the effect of substrate and solder interfacial reaction determines the reliability of the solder joints (Blair, Pan and Nicholson, 1998; Chen, Lin and Jao, 2004).

As can be seen in Table 4.5, the design point number 3 present is microstructures, which distinguish the solder, the IMC layer and the substrate. The interface boundary between the IMC layer and the solder and substrate is seen to be stable. On the contrary, the table shows that design point number 5 contains crack which seem to develop at the interface between the

IMC and the solder bulk and which usually propagate along the boundary region of the component/metallised bond.

However and as easily observed from a close examination, the constituents of the IMC layer in design point number 5 has significantly diffused into the solder bulk region as the region contains some patches of white substance not found in the design point number 3. By comparing the parameters and the settings between the two designs, however, it is observed that the settings of the pre-heat and time above liquidus is different in the two designs. From the observation, therefore, it is easily inferred that high pre-heat and low time above liquidus is critical to forming solder joint, which will possess high shear strength. Figure 4.2 depicts the EDX spectra of the 1206 CuSF test vehicle microstructure, which shows the distribution of the various elements in the solder joint while Table 4.6 presents their elemental and atomic percentage content. Figure 4.3 presents the backscattered electron image of the interface of the cross-sectioned 1206 resistor solder joint with spots showing the atomic concentration of Cu_6Sn_5 and Cu_3Sn intermetallic. The detailed discussion on these results are in four parts presented in sections 4.3.1 to 4.3.4.

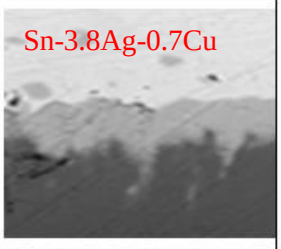
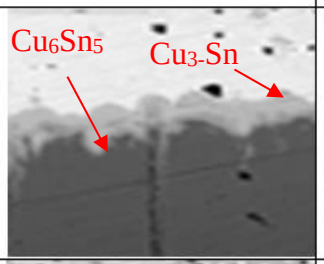
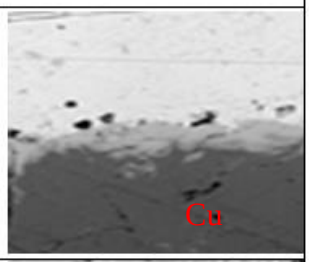
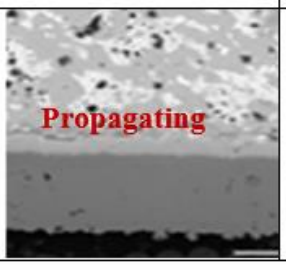
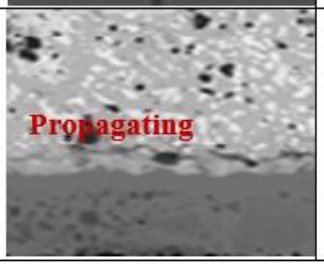
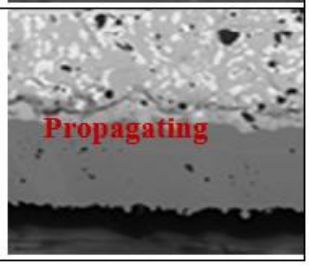
Table 4.3: Shows main expt. run with design point no., IMC thickness and shear force

Design point no	Factor and levels				Resistor component						Average IMC thickness in resistors' joint (µm)	Average shear force of resistors' joint (N)
					R1206	R1206	R0805	R0805	R0603	R0603		
	Preheat (°C/sec) [A]	Time above liquidus (sec) [B]	Peak temperature (°C) [C]	Cooling rate (%) [D]	IMC thickness (µm)	Shear force	IMC thickness (µm)	Shear force	IMC thickness (µm)	Shear force (N)		
1	1.2	60	245	100	7.01	65.54	3.91	62.17	4.25	42.23	5.06	56.65
2	**1.2**	**60**	**230**	**60**	**8.43**	**74.85**	**3.67**	**55.19**	**5.32**	**42.36**	5.81	57.47
3	1.2	45	245	60	3.82	67.60	4.78	62.72	3.58	46.48	4.06	58.93
4	1.2	45	230	100	3.23	72.94	4.22	58.05	3.92	40.21	3.79	57.07
5	**1.0**	**60**	**245**	**60**	**4.45**	**61.78**	**4.47**	**51.45**	**4.60**	**40.78**	4.51	51.34
6	1.0	60	230	100	5.78	64.33	5.56	66.00	5.53	42.12	5.62	57.48
7	1.0	45	245	100	6.9	68.63	4.56	68.32	4.72	39.21	5.39	58.72
8	1.0	45	230	60	3.21	67.94	4.60	58.41	3.20	43.13	3.67	56.49

Table 4.4: Data showing design point number, average IMC thickness and shear strength

	Resistor component							
	R1206	R1206	R0805	R0805	R0603	R0603		
Design Point no.	**IMC thickness (µm)**	**Shear Strength (MPa)**	**IMC thickness (µm)**	**Shear Strength (MPa)**	**IMC thickness (µm)**	**Shear Strength (MPa)**	**Average IMC thickness in resistors. Joint(µm**	**Average Shear Strength of resistors.' joint (N)**
1	7.01	42.28	3.91	62.17	4.25	87.98	5.06	64.14
2	**8.43**	**48.29**	**3.67**	**55.19**	**5.32**	**88.25**	5.81	63.91
3	3.82	43.61	4.78	62.72	3.58	96.83	4.06	67.72
4	3.23	47.94	4.22	58.05	3.92	83.77	3.79	63.25
5	**4.45**	**39.86**	**4.47**	**51.45**	**4.6**	**84.96**	4.51	58.76
6	5.78	41.50	5.56	66.00	5.53	87.75	5.62	65.08
7	6.90	44.28	4.56	68.32	4.72	81.69	5.39	64.76
8	3.21	43.83	4.60	58.41	3.20	89.85	3.67	64.03

Table 4.5: Micrographs showing the microstructure of the vertical cross sections on the various test vehicles of the eight design points

Design point number	1206 Micrograph	0805 Micrograph	0603Micrograph
3			
5			

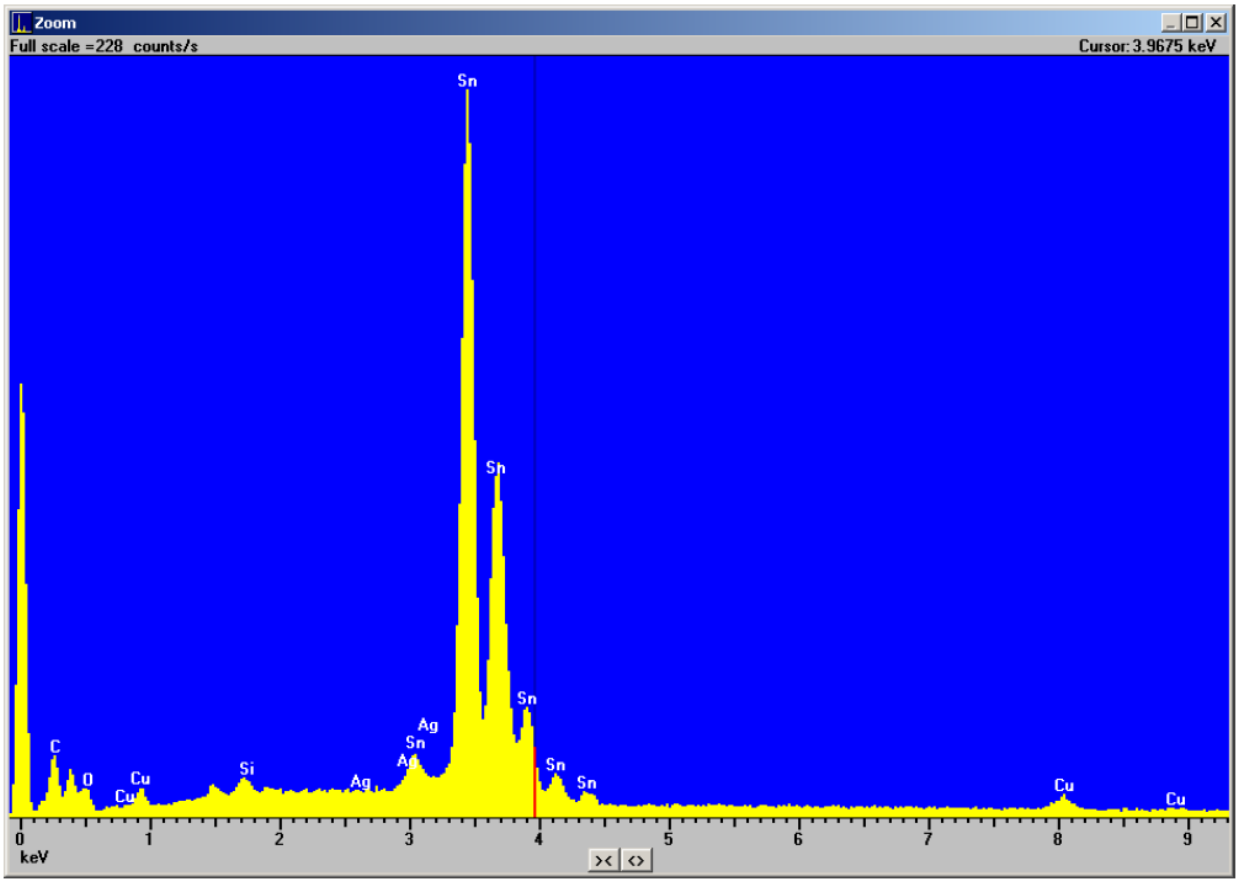


Figure 4.2: EDX spectra for SnAgCu lead-free solder joint microstructure with CuSF showing location of peaks for Sn, Ag and Cu

Table 4.6: Atomic % concentration of spots (indicated on fig. 4.3) and located at the solder/substrate interface metallisation and close to it

Element Type	Spect.	Element %	Atomic %
Si K	ED	1.67	6.30
Ag K	ED	0.93	3.67
Cu K	ED	3.92	6.55
Sn L	ED	93.47	83.49
Total		100.00	100.00

* = <2 Sigma

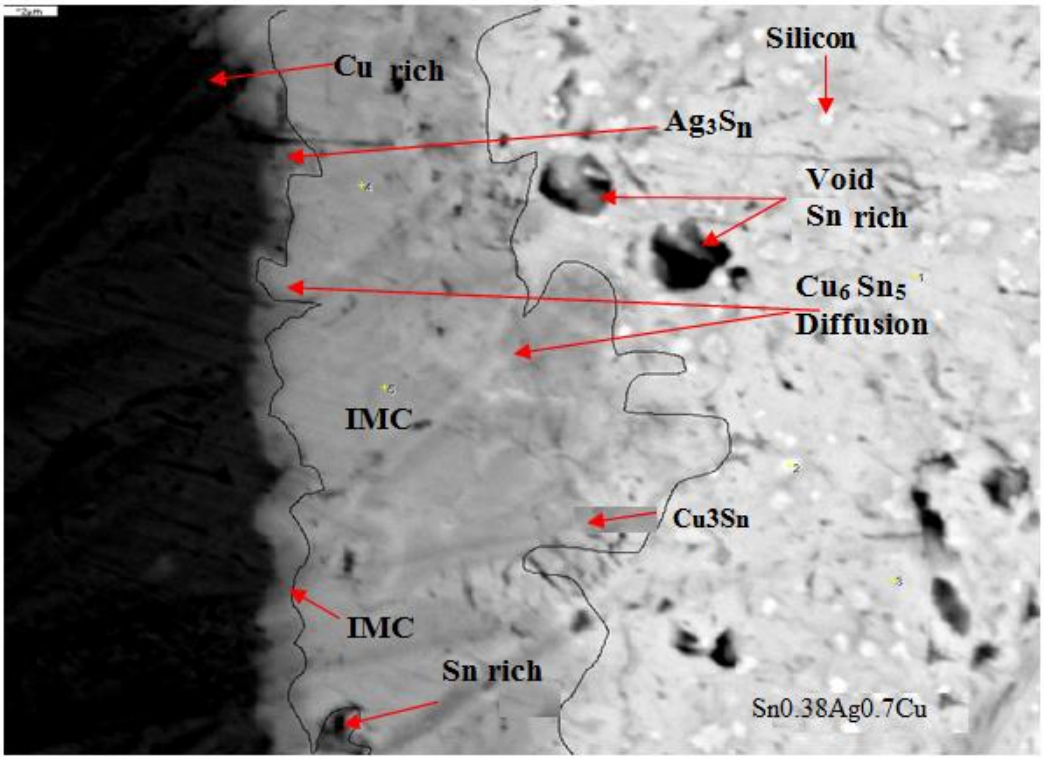


Figure 4.3: Backscattered electron image of the interface of the crosssectioned 1206 resistor solder joint with spots showing the atomic concentration of Cu_6Sn_5 and Cu_3Sn

4.3.1 Effect of Reflow Profile on Shear Strength of Solder Joints

Many researchers have reported on the effect of reflow profile on lead-free solder joints shear force. A survey of the reports shows that there are no established parameters settings for the reflow profile to yield solder joint, which will possess high shear strength and thus high reliability. Consequently, an investigation, which will advise on the settings of reflow profile parameters to achieve higher solder joint shear strengths and reliability, is considered in this research work. Table 4.4 presents the IMC thickness in addition to the shear stress for each design point number. The measured values of the experimental outcome are plotted; and their graph plots are in Figure 4.4 to Figure 4.7. Figure 4.4 represents the average shear strength of the eight designs. It shows that design point number 3 produced joints, which have the highest shear strength while design point number five produced joints, which have the lowest, shear strength.

The parameter settings of design point number 3 allowed for the proper formation of high integrity solder joints with right thickness of IMC.

Figure 4.5 is the plot of the average IMC layer thickness for the eight designs. It shows that design point number 2 possess the highest thickness of IMC while number 8 possess the least thickness. Since none of these two designs produced joint with the highest shear strength, the argument remains that the IMC thickness need to average for the integrity of the joint to be high. Corollary, too high and too thin IMC thickness is not advisable for the production of high integrity solder joint. By referring to Table 4.2 and Table 4.3, one can easily see that high preheat and time above Liquidus has accounted for the formation of highest IMC thickness.

Further comparison of the parameter settings of design point number 2 and 3 shows that the settings of time above Liquidus and peak temperature is critical in forming solder joint which will possess high shear strength. The research work by (Chen, Lin and Jao, 2004) concluded that both reflow peak temperature and time above Liquidus of the lead-free reflow profile are critical factors that determine the shear strength of the SnAgCu solder joints. Also, (Arra et al., 2002) stated that the peak temperature and the time above liquidus during reflow process are most important parameters affecting the solder joint reliability performance. Accordingly, in the case of SnAgCu reflow soldering, a peak temperature of 230°C is recommended for obtaining quality solder joints in t

Furthermore, a peak reflow temperature of 241°C led to decidedly more robust and effective solder joints than profiles with peak temperatures of 220 and 228 °C. The Figure 4.6 and Figure 4.7 present a plot of the thickness of IMC and the shear strength on the same column chart. The aim of the plots is to correlate the interaction and relationship of the two parameters. It is easily deduced from the plots that the strength of solder joints increases when IMC thickness increases and decreases when IMC thickness decreases except for design point numbers 3, 5 and 7. These points are considered as the points of inflexion and suggest the existence of interactions among the parameters, which might influence the solder joint shear strength.

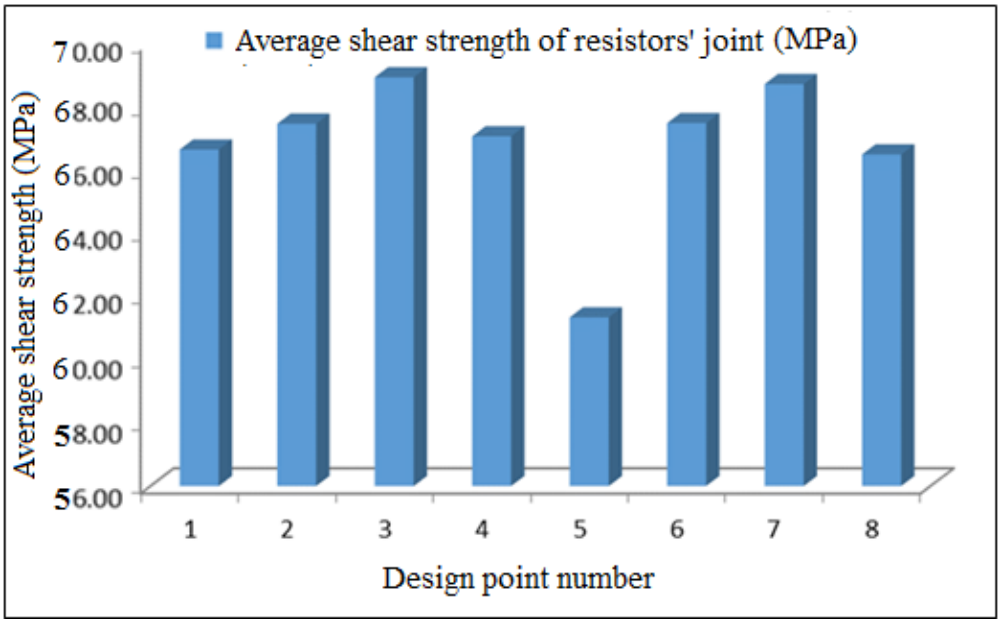


Figure 4.4: Plot of Av shear strength against design point number for all eight (8) designs

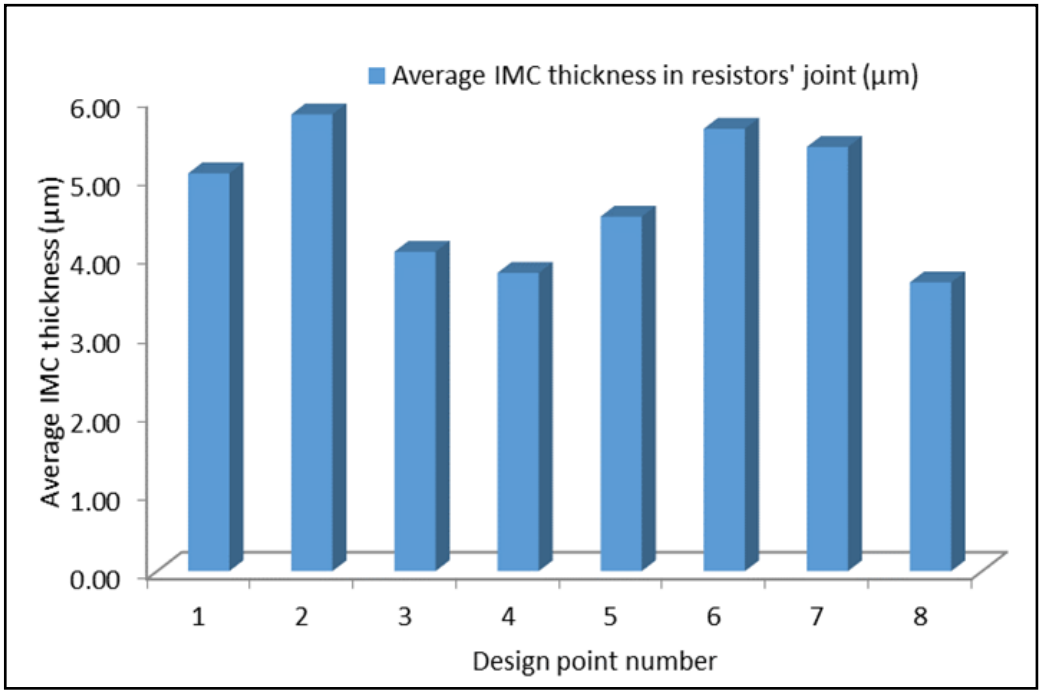


Figure 4.5: Plot of Av. IMC thickness against design point number for all eight designs

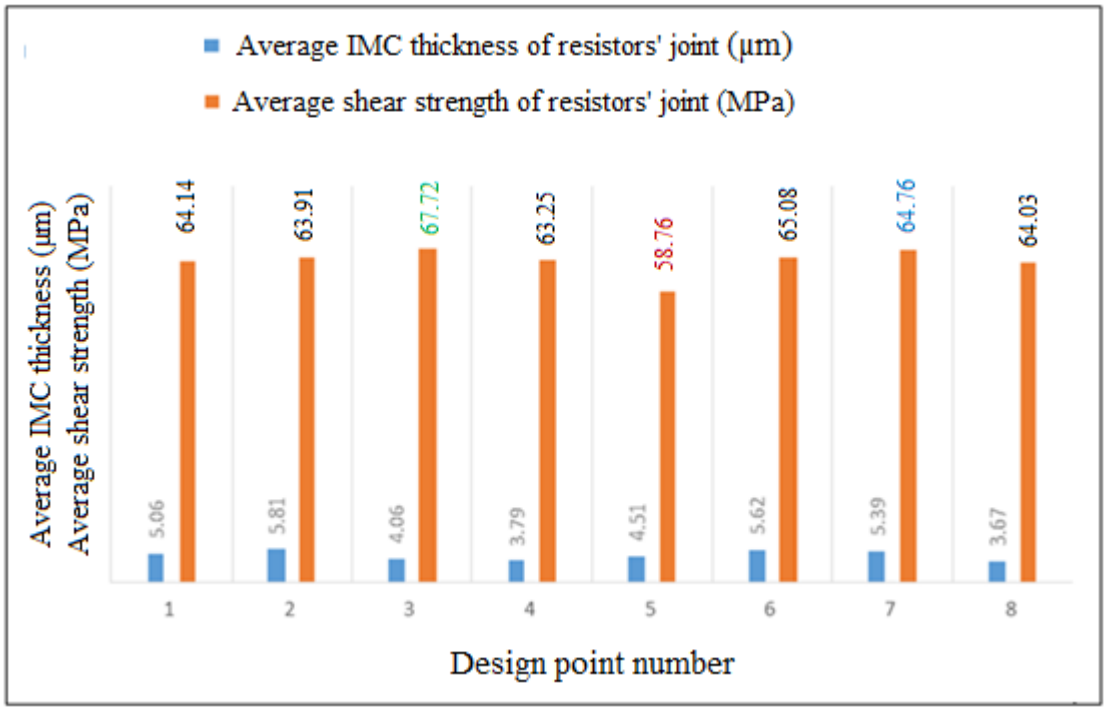


Figure 4.6: Bar plot of the thickness of IMC and the shear strength on the same column chart against design point number for all eight (8) designs

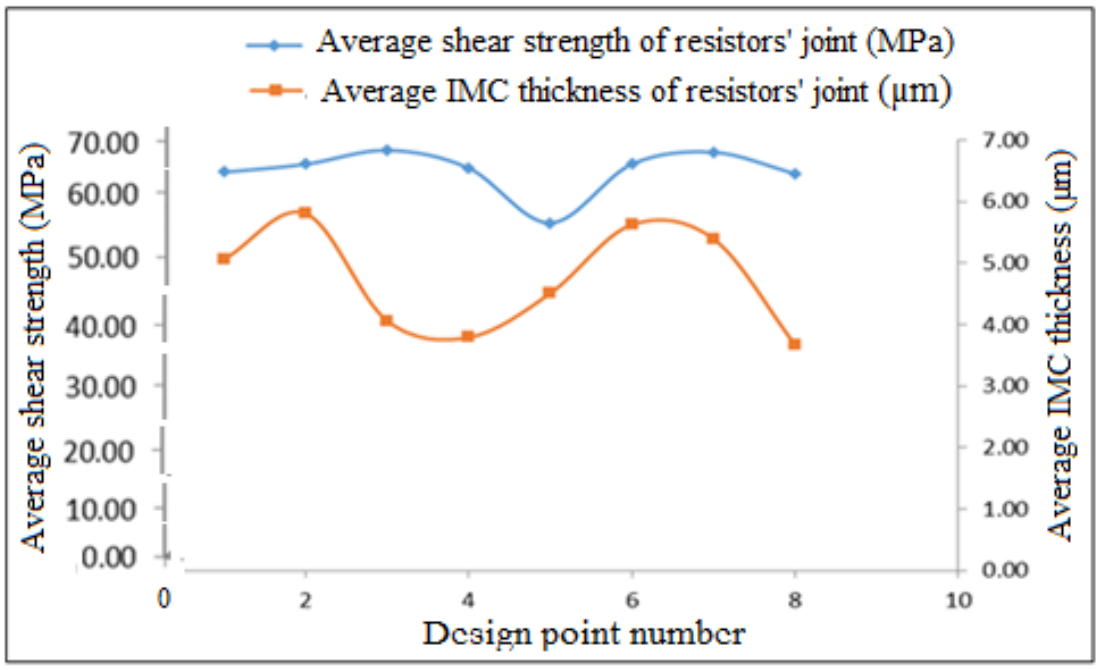


Figure 4.7: Av. IMC thickness and shear strength compared against design point number

4.3.1 Effect of reflow profile on size of solder joints

The effect of reflow profile parameters on the shear strength of the various resistors joints vary with the miniaturisation trend. Figure 4.8 shows the plot of shear strength of the different resistor solder joints against design point number. As can be seen from the plot, the shear strength increases as the size of the resistor component and its solder joints decrease. This shear strength behaviour was in contrast to the high shear forces obtained from each resistor component; meaning that the bond pad diameter and cross-sectional area (Figure 3.7.1, section 3.2.5.1) play major roles in the physical and material property characterisation of the solder joint. However, the perplexing result also reveals that in line with product miniaturisation trend, lead-free solders irrespective of their price effectiveness and throughput consolidations are capable of forming good metallurgical bonding and can serve as an excellent alternative to SnPb solders especially in consumer electronics. Figure 4.9 presents the microstructure of the three different joints. From a close observation, the smallest joint (the R0603 Resistor) apart from having high shear strength as presented in Table 4.4, shows a significant degree of fracture and the largest solder joint (R1206) exhibited the least considerable damage.

The EDX spectra in Figure 4.2 shows the presence of Sn, Ag and Cu. Some whitish silicon impurities appeared in the micrograph of the soldered joints, expressing some doubts in the integrity of the solder joint formulation. Table 4.6 presents their elemental and atomic contents. The solder/substrate interface metallisation (Table 4.6) and close to it exhibited 100% Sn-Cu and Ag-Sn intermetallic as shown in Figure 4:3. (for example with backscattered electron image of the interface of the cross-sectioned 1206 resistor solder joint with spots showing the atomic concentration of Cu_6Sn_5 and Cu_3Sn), which cuts across in similar form, but in much less dense proportion to the other two resistor components, for both soldering and PCB bonding used.

In general, the results demonstrate that miniaturisation effects the solder joint integrity significantly. Consequently, electronics design and manufacturing engineers need to seek technique of improving the solder joint strength to manage the solder joint reliability with increasing miniaturisation-manufacturing trend.

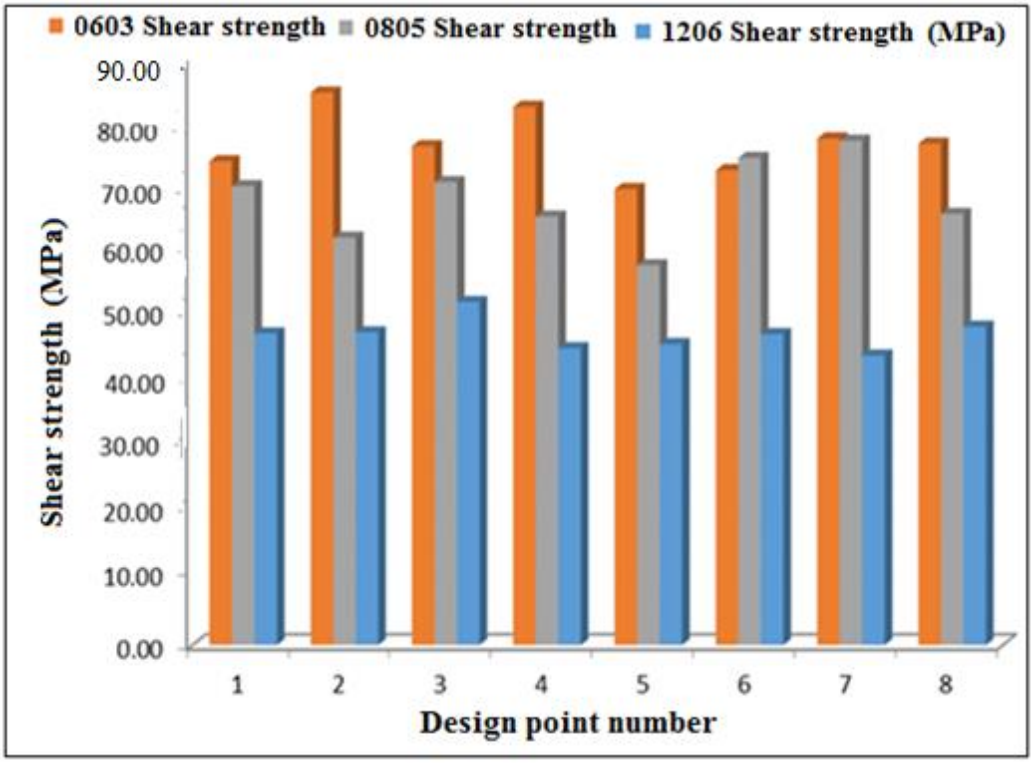


Figure 4.8: Plot of shear strength against design point number for all eight (8) designs

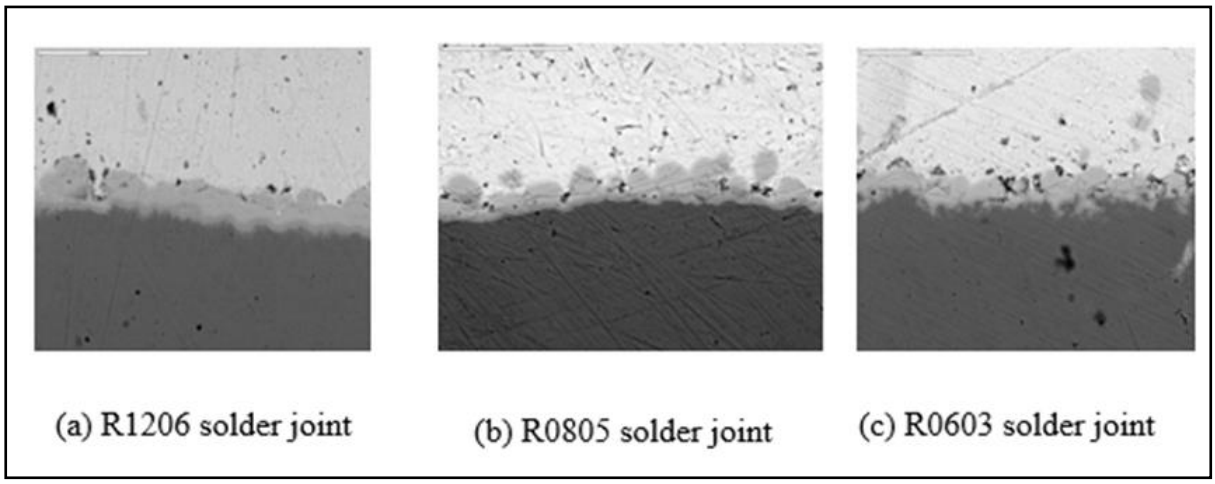


Figure 4.9: Microstructure of the joints of the three resistor assemblies.

4.3 Chapter Summary

The settings of reflow parameter values influence the integrity and consequently the shear strength of solder joints in SMT resistor assembly. Based on the results of this investigation, variations on the magnitude of preheat and time above Liquidus have accounted for the largest and smallest solder shear strength observed in the study. Since a higher preheat, and a lower peak temperature has demonstrated the potential of producing higher integrity solder joints in SMC assembly. These factors as concluded have main effects on the strength of the solder joints. The author suggests that parameter settings of design point number 3 should be utilised for reflow profiling when soldering surface mount chip resistor on the substrate.

From the investigation on the effect of parameter, settings on the reliability of solder joints in miniaturised components, the shear strength of the solder joints increases as the resistor size and in turn, the joints decrease in size. Consequently, the mechanical reliability of SMC lead-free solder joints studied decreases as the components become larger in size. This outcome could be attributive to the low level of thermal distribution and diffusion of peak temperatures on larger components, which require soaking time during, reflow soldering period. The significance of this observation in material property evaluation is the need for electronics design and manufacturing engineers to explore advanced techniques of keeping up with device solder reliability in the current quest for matching customer demand on product miniaturisation.

Chapter 5: Effect of Strain Rate on Thermomechanical Reliability of Surface Mounted Chip Resistor Solder Joints in Electronic Manufacturing

5.1 Introduction

The thermomechanical reliability evaluation of surface mounted chip resistors' solder joints is becoming increasingly important in the packaging industry due to increasing miniaturised electronic products. Miniaturisation in electronics (Johnson et al., 2004) has occurred on a very vast scale and every single moment is spent to decrease the size and increase the functionality of every single electronic chip. The most apparent reason for this extensive miniaturisation is to save resources and cost of manufacturing ultimately (Lau and Pao, 1997). Since electronic components are getting smaller and their usage is increasing simultaneously, the need to build stronger IC product parts also arises. Considerably, the components have to go through all the thermomechanical shocks and should be able to withstand the thermal cycling/vibration effects (Liu, 2001; Park and Feger, 2009) without failing or getting fractured.

Small chips, which are attached to PCBs, are mostly prone to breaking off during temperature cycling since the solder joints between the chip and PCB are fragile and cannot withstand high shear forces. Weak strength of solder joints (Ekere et al., 2008) adversely affects the overall performance of every electronic device and numbers of methods have been employed to counter this problem. The most promising are selecting the right solder alloy which would give the solder joint its tensile or ductile properties, (Lau et al., 1990; Lau, 1996) make it more sustainable and give it the ability to withstand thermal load (Ekere et al., 2008) and other environmental stress conditions.

This chapter evaluates the 'Effect of Strain Rate' on the thermomechanical reliability of surface mounted chip resistors solder joints in electronic manufacturing. The test materials, the equipment and the experimental methodology used in this study have been described;, and presented in Chapter 3. In this chapter, a pictorial representation of the test vehicle is in Figure 3.8, and the experimental procedure is as described in section 3.2.5. The results of the experimental outcome were analysed and discussed in section 5.3 and the conclusions drawn are presented in section 5.5 of this chapter.

5.2 Experimental Details

The investigation and the evaluation of the effect of strain rate on the thermomechanical reliability of the surface mounted chip resistors solder joints were carried out after the reflow soldering and isothermal ageing process. The reflow parameters used was an enhanced reflow

following the outputs from Chapter 4. It comprises of materials and methods, equipment and test vehicle preparation and assembly procedure. The experimental test process used for as-soldered or non-aged samples in this investigation consists of five steps and one additional step for the isothermally aged samples. The details of the samples are in Chapter 3 section 3.2.3, Figure 3.4. The commercially available lead-free solder paste sample described in Chapter 3, section 3.3.1 is used in this investigation as the jointing material when mounting the resistors. The components were carefully selected so that they represent the different sizes of SJs when mounted on the substrate. However, a shear test was performed with the assembled components at a different shear rate to determine the rate of strain deformation. Finally, further test analysis and examination conducted was on the solder joints micrographs for ductile and brittle fractures. The experimental data was used to compare the results from the literature.

5.3 Experimental Results and Discussion

This section presents the results and analysis of the experimental study on 'Effect of Strain Rate' on the thermomechanical reliability of surface mounted chip resistor solder joints. The section consists of four main sub-sections. The first sub-section presents the shear test results for the non-aged samples. The second part shows the shear test results of the isothermally aged samples. The third section presents a comparative study of the shear test results of the aged and non-aged samples. The fourth and last part outline the results from the observation of fractured shear surfaces using SEM.

5.3.1 Shear Strength Test Results of Non-Aged Samples

The results for the non-aged reflowed samples comprising the three component types (1206, 0805 and 0603); described earlier are tabulated in Table 5.1 to Table 5.3 and represented graphically on Figure 5.1 to Figure 5.3. A strain rate calculation from shear speed and gauge length is obtained using the following formula in Eq. 5.1:

$$\text{Strain Rate} \qquad \dot{\varepsilon} = \frac{speed,\ v\ [\mu m/s]}{gauge\ length, \Delta L\ [\mu m]}. \tag{5.1}$$

Here, gauge length is the shear height, which was constant at 60 µm, all through the experiments. The shear strength values, however, were also calculated by dividing the respective shear forces of the different chip resistors with their respective shear areas.

Table 5.1: Average shear strength for as-reflowed ‘1206. 'component type

Component Type ‘1206.'				
Shear Speed (µm/s)	**Strain Rate (sec^{-1})**	**Shear Force (N)**	**Shear Area (m^2)**	**Shear Strength, MPa**
100	1.67	61.88	$1.55x10^{-6}$	39.92
250	4.17	61.14		39.45
400	6.67	60.78		39.21
550	9.17	64.71		41.75
700	11.67	57.06		36.81

Table 5.2: Av. shear strength for as-reflowed ‘0805.'Component type’

Component Type ‘0805.'				
Shear Speed (µm/s)	**Strain Rate (sec^{-1})**	**Shear Force (N)**	**Shear Area (m^2)**	**Shear Strength, MPa**
100	1.67	52.59	$1.0x10^{-6}$	52.59
250	4.17	71.3		71.30
400	6.67	56.27		56.27
550	9.17	51.12		51.12
700	11.67	55.57		55.57

Table 5.3: Av. shear strength for as-reflowed ‘0603.'Component’ type

Component Type ‘0603.'				
Shear Speed (µm/s)	**Strain Rate (sec^{-1})**	**Shear Force (N)**	**Shear Area (m^2)**	**Shear Strength, MPa**
100	1.67	37.39	$0.48x10^{-6}$	77.90
250	4.17	37.32		77.75
400	6.67	36.01		75.02
550	9.17	45.85		95.52
700	11.67	32.88		68.50

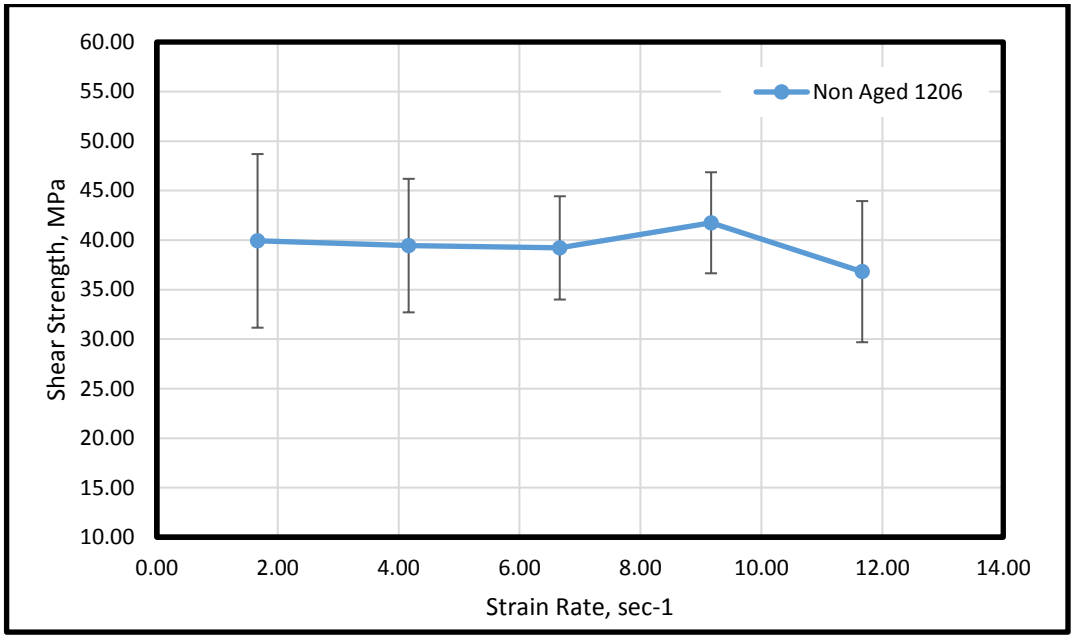


Figure 5.1: Relationship between shear strength and strain rate for 1206 component.

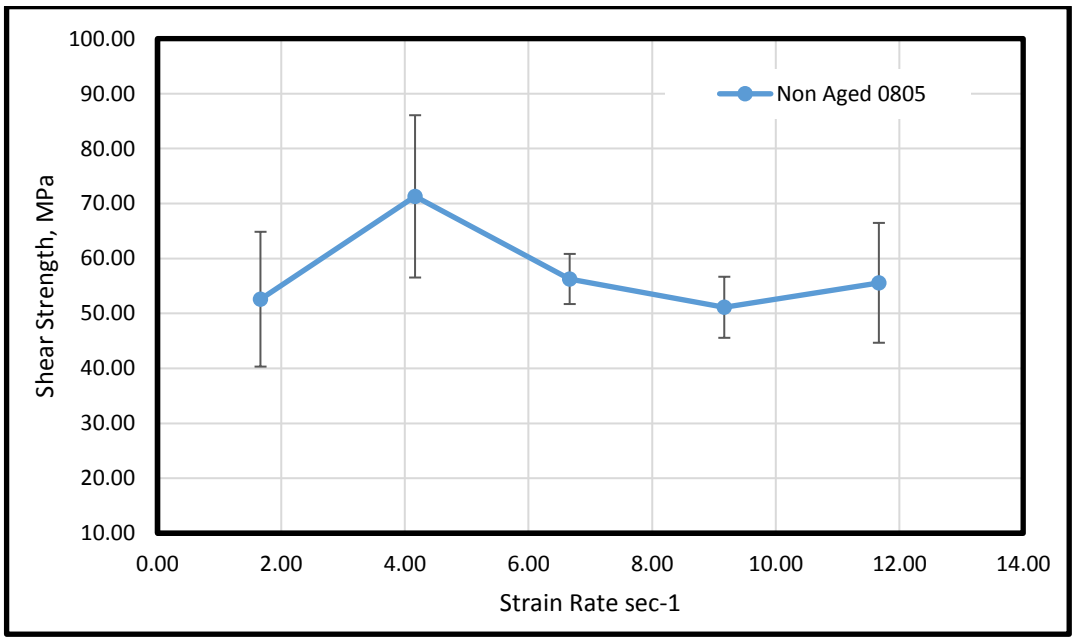


Figure 5.2: Relationship between shear strength and strain rate for 0805 component.

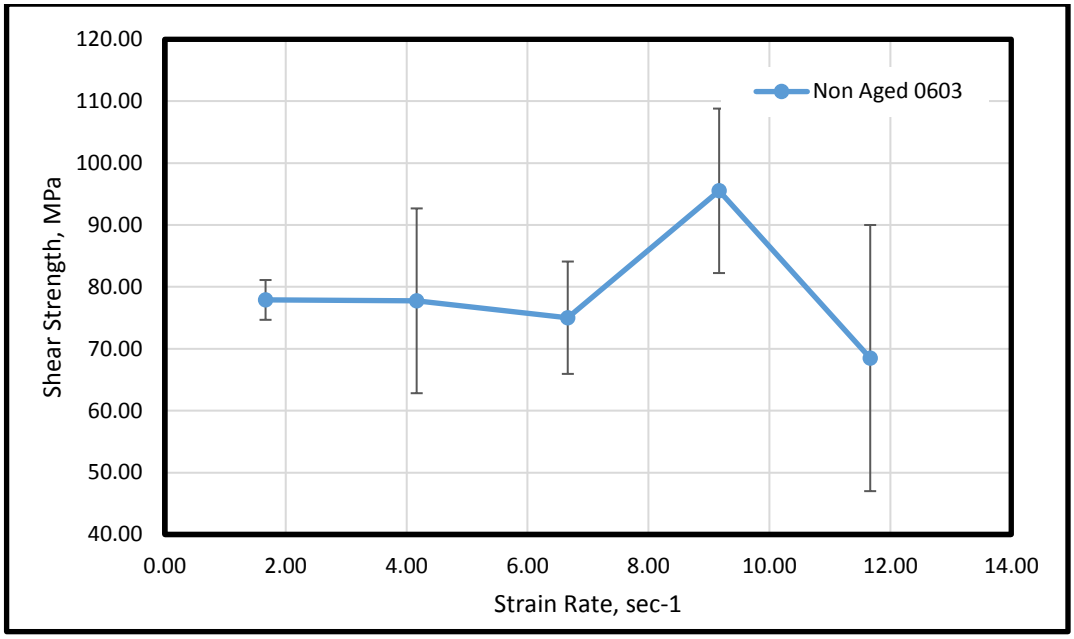


Figure 5.3: Relationship between the shear strength and strain rate for 0603 component.

The results of the non-aged (i.e. reflowed samples) tabulated in the given three Tables 5.1 to 5.3 represented all three types of components used in this work. Before the conduction of the experiment, the given theory of Hook's law of elasticity was first in consideration; that when strain rate increases, the shear strength decrease and the larger the component is, the greater, the shear force will be to cause a fracture. Nonetheless, the effect of strain rates on the shear strength of dynamic solder joints has ben described in section 2.7.2 of Chapter 2 with reference from different resources. By the results presented, the author's expectations were in agreement with the theory mentioned above that with the increment in strain rate, a gradual decrease in shear force values would be observed.

However, the graph for component type '1206' shows that for the first three strain rates the shear strength of the solder joints gradually declined, but it suddenly increased at a substantial shear speed of up to 550 microns/sec (strain rate 9.17/sec). Ultimately, it dropped again at 700 microns/sec and the force value was even smaller than the first three values observed. More significantly, the graph plots depict a decreasing trend as noticed in the force values except one value, which has deviated a bit. Applying a correction factor given in Equation 5.2, which is beyond the scope of this work on the graph, could align the trend more appropriately. For example, assuming C_f = Correction factor for x and y coordinate axis. Then,

$$C_f = \frac{1}{n}\sum_{i=1}^{n} x_i - y_i,$$

$$y = x + C_f \tag{5.2}$$

Equation 5.2 would represent an estimate of the amount by which y-values differ from x-values, which will help to quantify the potential relative drift in a graph.

The graph for component type '0805' demonstrates that strain rate has a significant main effect on the shear strength values. However, the graph curves initially showed a sudden rise upstream when shear speed increased from 100 to 250 micron/sec. This speed increase is an equivalent of 1.67 to 4.17 strains rate sec-1 and might be due to cold solder joint at the first plot; and then there was a recovery with a sudden decrease in shear strength when shear speed increased with a difference of 150 microns/sec (2.5-strain rate sec^{-1}). Following the sudden decline, there is a further gradual drop in the shear force for a simultaneously increasing strain rate, and ultimately it increased again. Although the decreasing trend prevails in the graph since the shear strength has decreased consecutively for two strain rates, it is quite noticeable that data has scattered and the results have moved a bit away from the initially proposed general and theoretical expectations. This outcome may have resulted from inadequate heat transfer by radiation (Archambeault et al., 2013) from the top and bottom surfaces of the reflow soldering board (Tsai, 2012), which is significant in many natural convection cooling situations and must be, not overlooked. In this wise, a correction factor which is beyond the scope of this study may be needed to align the curve to the right trend for analysis purposes, repair and rework (J. Liu et al., 2011) of the defaulting or cold joints may become necessary for reliability determinations.

The third graph, which is belonging to component type '0603', possesses similarities with the first graph since the pattern followed is identical to the first one. The shear strength values descend with the increment in the strain rate, but again a sudden rise could be seen in the effect when the strain rate was 9.17/sec. At last, the graph dropped down again when the strain rate value was 11.67/sec, much lower than the first three values. However, just like the first graph, the declining trend in the strength values has been observed; with only one value deviating from the original pattern, otherwise, the shear strength values decreased relatively as the strain rate increased. The deviated joint may have resulted from the growth of tin whiskers in the

solder joint (J. Liu et al., 2011); or from an entrapped moisture from the package/component during reflow. During reflow, however, high temperature makes the moisture to evaporate and increase the pressure inside the component, leading to component failure by bulging and popping, known as popcorning (Ning-Cheng, 2002).

From Figures 5.1 to 5.3 it was observed that the shear strength is independent of the shear strain rates used. The independent behaviour is quite contrary to author's expectation on this type of material. Moreover, a multiphase alloy like solder should show rate-dependence as reported correctly in Figure 2.26. It might be possible that the growth on IMC may be cancelling out any expected increasing rate-dependence. The shear rate independent behaviours of solder can be explained in the light of the research carried out by (Chia, Cotterell and Chai, 2006). Concerning the dependence of dynamic solder joint strength with strain rate, it may be possible to say that the limited decades of time considered here (e.g. 700μm/s = 11.67 strain rate sec^{-1}) might be accounting for the observed rate-independence. In an ideal case, one needs to go up to at least four decades of time (104 strain rate sec^{-1}) to conclude on the substantial effect of strain rate (as per Chia et al., 2006). However, the Dage Tester used in this investigation is not designed for high-speed shearing, where maximum shear speed is limited to 700μm/s. The research outcome recommends that a future work on high-speed shear behaviours of solder strength, to understand the effect of strain rate on the shear strength fully.

5.3.2 Shear Strength Test Results of Non-Aged Samples Compared

The comparison in shear results on strain rate deformation is tabulated in Table 5.4 and represented graphically in Figure 5.4 respectively.

Table 5.4: Av. Shear strength values for non-aged 1206, 0805 and 0603 compared

	Average Shear Strength, MPa		
Strain Rate	**Non-Aged**	**Non-Aged**	**Non-Aged**
(/s)	1206	0805	0603
1.67	39.92	52.59	77.90
4.17	39.45	71.30	77.75
6.67	39.21	56.27	75.02
9.17	41.75	51.12	95.52
11.67	36.81	55.57	68.50

By observing and comparing what was obtained from the shear strength values of non-aged samples, it was noted that as the test speed changed, fracture behaviour of the solder joint also changed, resulting in a variation in its shear strength. Fracture behaviour varies in such a way that brittleness in the fracture occurs in abundance when strain rate is high thereby producing little shear strength. Ductility takes over when strain rate state is low and this in return makes the solder joint to go under inelastic expansion, which results in increasing the force required for fracture. Law of physics also applies here. Shearing at low-test speed possesses less momentum and exerts more force to break the joint. When the test speed was increased, energy increases and the tool use less power to cause a fracture. Due to all these reasons, the expectation was that shear strength for aged, and non-aged samples decrease with increasing strain rate.

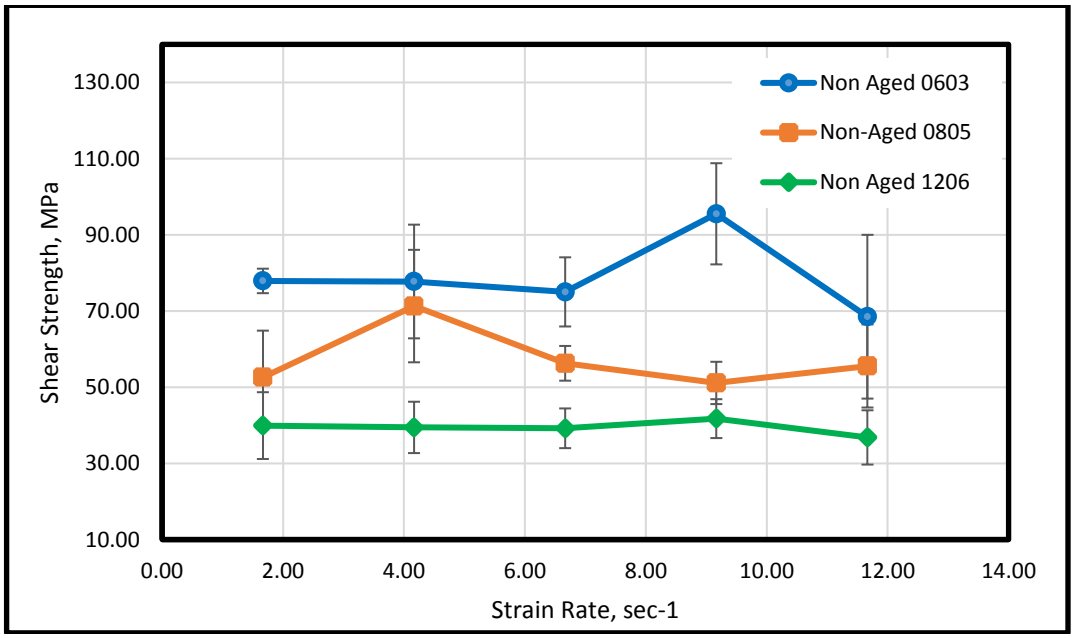


Figure 5.4: Shear strength as a function of strain rate for non-aged samples

5.3.3 Shear Strength Test Results of Aged Samples

Table 5.5: The average shear strength of aged samples of the '1206' component type

Component Type '1206.'			
Shear Speed (µm/sec)	**Strain Rate (/s)**	**Shear Force (N)**	**Shear Strength (MPa)**
100	1.67	63.5	40.97
250	4.17	57.45	37.06
400	6.67	53.16	34.30
550	9.17	55.26	35.65
700	11.67	60.9	39.29

Table 5.6: The average shear strength of aged samples of the '0805' component type

Component Type '0805.'			
Shear Speed (µm/sec)	**Strain Rate (/s)**	**Shear Force (N)**	**Shear Strength (MPa)**
100	1.67	53.84	53.84
250	4.17	65.31	65.31
400	6.67	54.32	54.32
550	9.17	61.23	61.23
700	11.67	61.48	61.48

Table 5.7: The average shear strength of aged samples of the '0603.' component type

Component Type '0603.'			
Shear Speed (µm/sec)	**Strain Rate (/s)**	**Shear Force (N)**	**Shear Strength (MPa)**
100	1.67	35.6	74.17
250	4.17	38.41	80.02
400	6.67	32.81	68.35
550	9.17	37.33	77.77
700	11.67	36.44	75.92

5.3.4 Shear Strength Test Results of Aged Samples Compared

The tabulated comparison in the shear results on strain rate deformation for all three samples is in Table 5.8 and graphically represented in Figure 5.5 respectively.

Table 5.8: Av. Shear strength values of isothermally aged 1206, 0805 and 0603 compared

Strain Rate (/s)	**Average Shear Strength, MPa**		
	Aged 1206	**Aged 0805**	**Aged 0603**
1.67	40.97	53.84	74.17
4.17	37.06	65.31	80.02
6.67	34.30	54.32	68.35
9.17	35.65	61.23	77.77
11.67	39.29	61.48	75.92

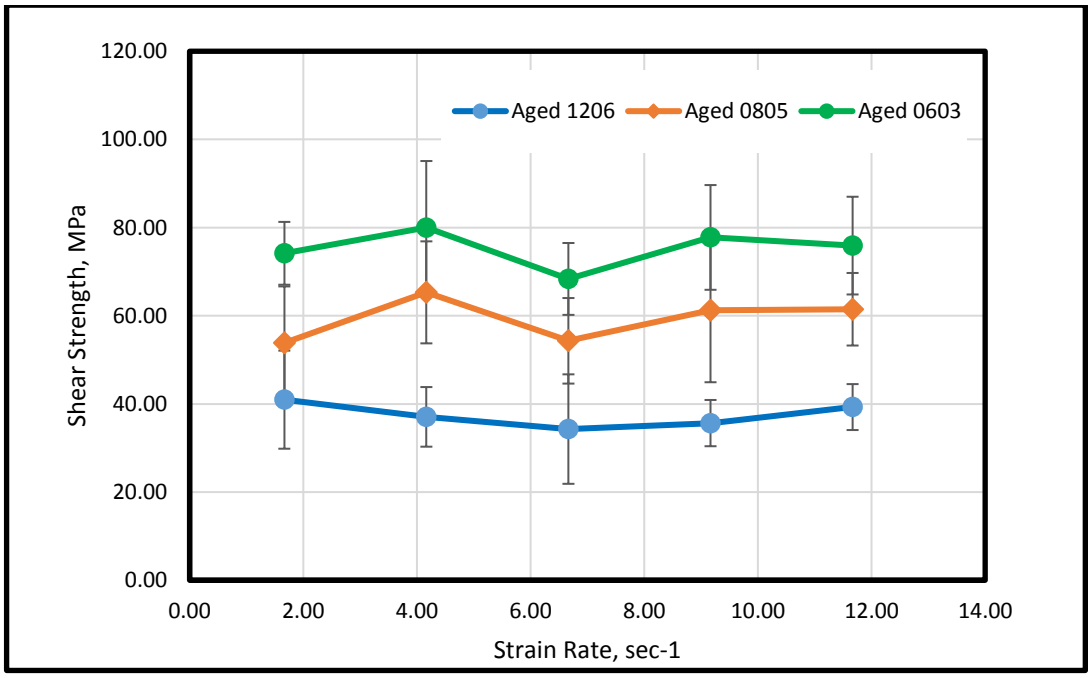


Figure 5.5: Shear strength as a function of strain rate for aged samples

5.3.5 Study on the Fracture Surface of Aged Solder Joints

The results for aged samples are as tabulated in the last three tables for the components from all three types. Before the conduction of the experiment with the thermally aged specimens, it was again expected based on existing theories in material science and laws of physics that when

Strain rate increases, the Shear strength decreases and the larger the component is, the larger the shear force will be to cause a fracture. By referring to the explanation given in the second chapter for the effect of ageing, which stated that thermally aged samples would have comparatively low shear strength due to the growth of thicker intermetallic layer structure.

The graph of the 1206-aged sample shows that the shear strength is initially decreasing with increasing strain rate, but this happened only with the first three strain rates. After 6.67/sec when the strain rate raised to 9.17/sec, the increment in the shear strength was noticed to have gone upstream up to the highest peak by following the same linear pattern with which it came down to the first three strain rates. The expected decreasing trend initially noticed did not hold on, but since the overall behaviour of the data is random, the trend has entirely changed. The second graph for aged 0805 sample shows that the strength has an upward swing right at the beginning and again the strain rate in this regard does not seem to have a significant effect. When the strain rate increased to 4.17/sec the force value fell significantly but it again increased when 9.17/sec was applied, and at 11.67/sec a very slight increase could again be noticed. The third graph for aged 0603 sample shows almost the same pattern as the graph of the thermally aged 0805 with a few noticeable differences. Initially, the difference was in the trend that shear strength value followed. From approximately 2 to 4--strain rates/sec, the shear strength rose gradually from approximately 74 to 80 MPa and went through sudden decrease when 6.67/sec was applied. At 9.17/sec the shear strength has again increased following the same pattern as in the graph of 0805. In the end, at 11.67/sec, the force has decreased again very slightly.

After analysing the obtained results from the shear strength of the thermally aged samples, the analysis showed that there had not been a direct correlation between the strain rate and the shear strength. The indirect relationship shows that the trends on all the graphs do not have any particular trend and the fractured behaviour of the said thermally aged samples has varied randomly. Even there is a contradiction in the second assumption, that more shear force is required for fracture if components are bigger in size as ‘0805’ type component had taken almost the same shear force as type ‘1206’ to fracture even when there was a noticeable difference in the sizes. Therefore, isothermal thermal ageing overall did not have any noticeable effect on the shear strength of the solder joint at the limit measured. The reason for not noticing any significant effect was because during the ageing stage, two different processes were taking place at the same time and each of them was working in opposite manner. If intermetallic layer were growing due to the formation of intermetallic compounds at the solder joint’s common

base or near interfaces, there would be a decrease in the strength resulting from increasing brittleness and formation of precipitates. In this case, Tin is dissolving other metals present in the solder alloy at a higher rate due to the elevated temperature and excess Tin precipitates occurrence. These precipitates due to long ageing hours, get tiny and disperse finely and immobilise the dislocations in the microstructure resulting in high strength (Shekhter et al., 2004; Jones, 2001; Xiao, Nguyen and Armstrong, 2004). This immobility of the dislocations in the microstructure was the reason for the shear strength of aged samples to be same as the non-aged ones. Another reason may be that lead-free solder joints can sustain high-temperature ageing.

5.3.6 *Comparative Study of Shear Strengths of Aged & Non-Aged samples*

Figure 5.5 to Figure 5.8 present a comparative study of shear strength values for aged and non-aged samples. In the non-aged samples observed, results followed mostly the general theory and in most occasions, the shear strength decreased with increasing strain rate. Secondly, there was a noticeable difference in the force values on the size of the component. It was observed from Table 5.4 that between the component type 1206 and 0805 there is a gap of about 5 to 7N in the shear force values; furthermore, there is a vast difference in the magnitude of shear forces of type '0805' and '0603'. Therefore, results were according to expectation.

In aged samples, observations made showed that results scattered randomly and did not follow any particular trend; and thereby completely contradicting the theoretical assumptions earlier reviewed. Firstly, as expected from the non-aged (reflowed) samples, there would be a decreasing trend as observed in the shear strength values with increment in the strain rate of thermally aged specimens. However, it would be a lot less reliable as less shear force will be required to cause fracture due to thicker intermetallic layer structure. There was contrary observation, as there was no particular pattern followed by shear strength trend with increasing strain rate and the shear force exerted to cause fracture was almost the same as the non-aged samples.

Secondly, from the experiment done with the different type of components, except the difference in the result of 0603, there was no such difference observed between 1206 and 0805 values as shown in Table 5.5 and Table 5.6 respectively. Nevertheless, only minute differences as noted occurred in the shear strength for component type '1206; and '0805'. However, the

results and the graph trend do not represent earlier expectations. The reasons why results deviate are already answered questions in the previous discussions, attributively is to thermal and isothermal changes during reflow soldering. In concluding, each solder joint possesses its shear strength irrespective of the type and the size of the component and it is dependent upon the environment and the subjected operating ambient temperature condition (isothermal ageing). The variation in shear strength is attributive to the uneven development of the microstructure and growth of intermetallic layer in each solder joint. Some of the joints even if they are smaller and less dense, they have still consumed more shear force to fracture (see Table 5.4 and Table 5.5), and this could be because more precipitates may have formed in their grain structure.

Finally, this investigation showed that isothermal ageing has not significantly affected the reliability of the solder joints as the shear strength values have appeared to be almost same for aged and non-aged solder joints. However, more ageing time to enhance growth that is more metallic may be required to actualise the trend and behaviour of the joint. This is because if an intermetallic layer is decreasing the strength, then encountered is also the increment in the overall strength; and this occurs due to precipitation in the solder alloy (Mallik and Mehdawi, 2013).

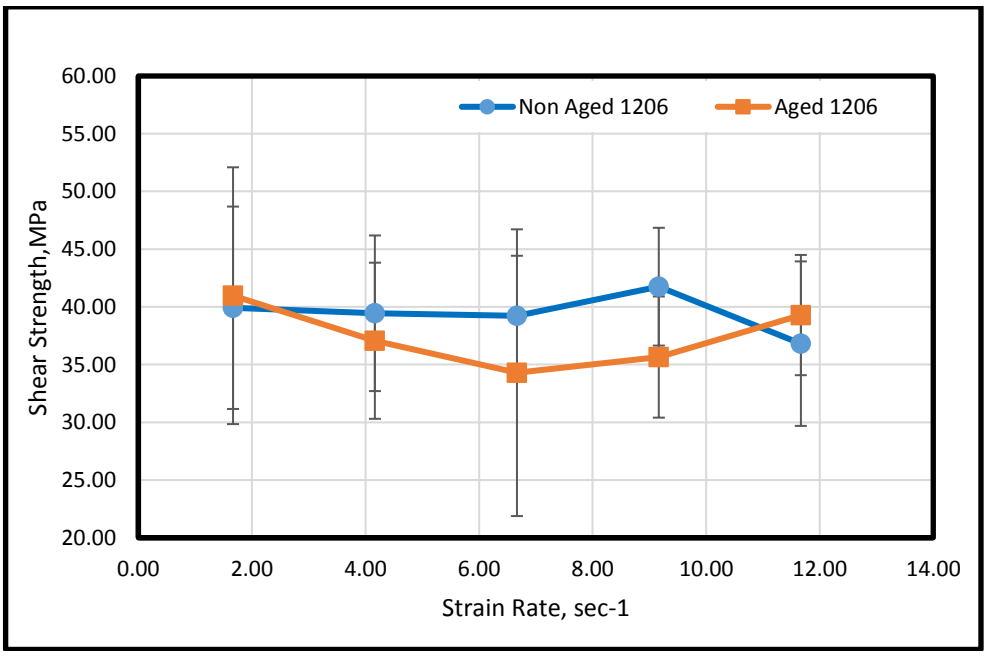


Figure 5.6: Shear strength vs. strain rate for aged and non-aged 1206 samples

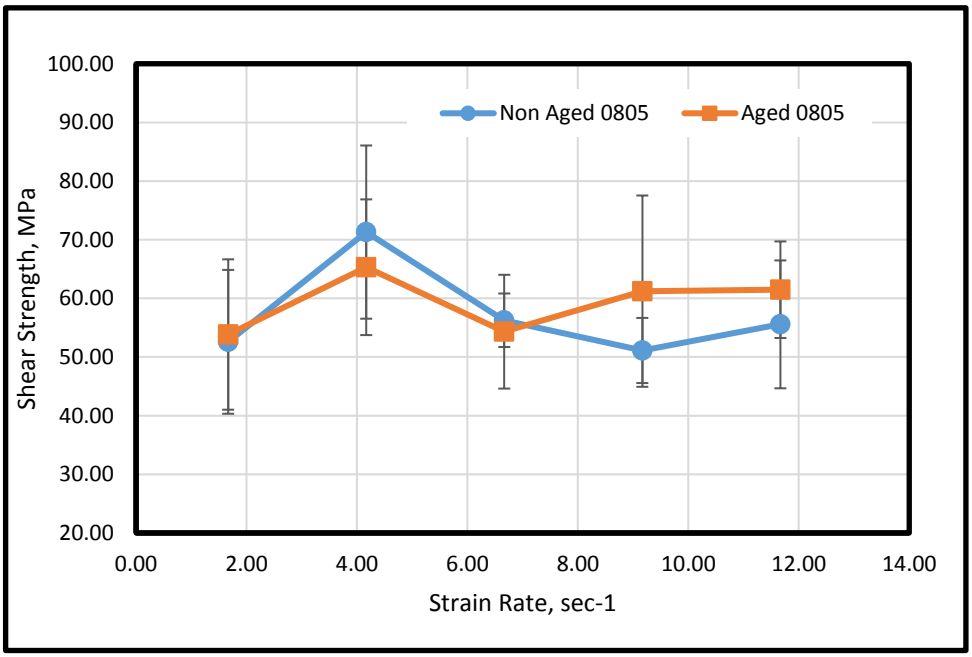


Figure 5.7: Shear strength vs. strain rate for aged and non-aged 0805 samples

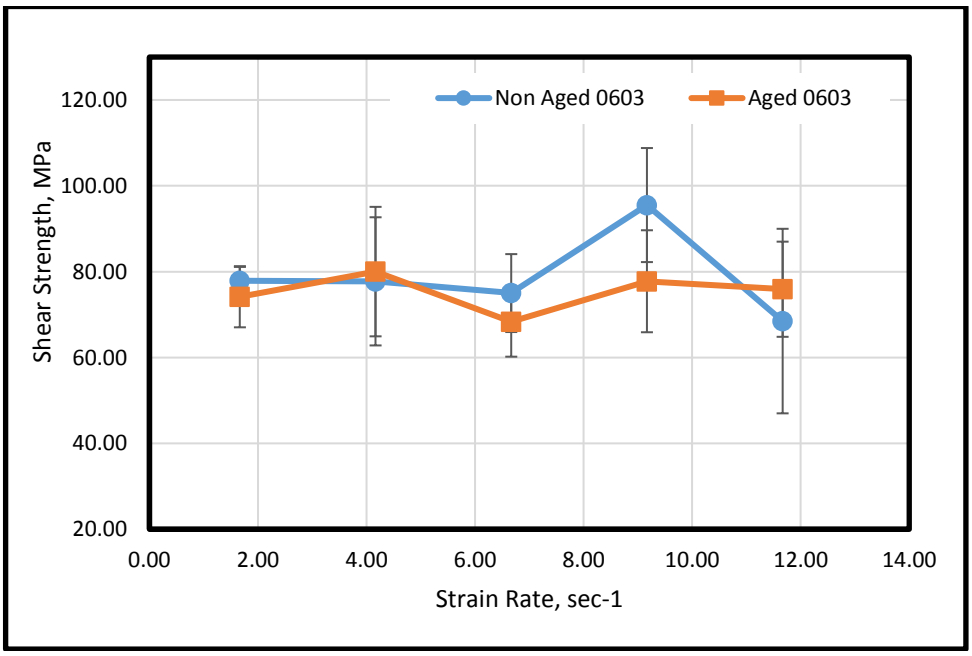


Figure 5.8: Shear strength vs. strain rate for aged and non-aged 0603 samples

5.3.7 Investigating Aged and Non-Aged Solder Joints Surface Fracture

The previous three sections of this chapter focused on how shear strength was affected by different strain rates and the effects of isothermal ageing on solder joints. In this part, carefully observed fractured surfaces of all soldered components type in use were analysed. Each micrograph presented in this section comprised of two snapshots; the left part shows the fractured solder pad and the right show the magnified view of it.

The fracture behaviour of solder joints is very complex in nature. For example, depending on the intensity and speed of applied load, solder balls could fail through pad lift, interfacial fracture (solder/intermetallic or intermetallic/pad) and bulk solder failure (Ahmadi, 2009). Among these failures, interfacial fractures are predominantly brittle, and bulk solder fractures are or tend to be ductile in nature. However, solder ball failure through mixed fractures is also frequently observed by various researchers (Mannan et al., 1995; Ahmadi, 2009). Figure 5.9 and Figure 5.10 present the SEM fracture surface micrograph for non-aged 1206 component sheared at 100µm/sec and 700µm/sec (1.47 and 11.67 strain rate/sec) respectively.

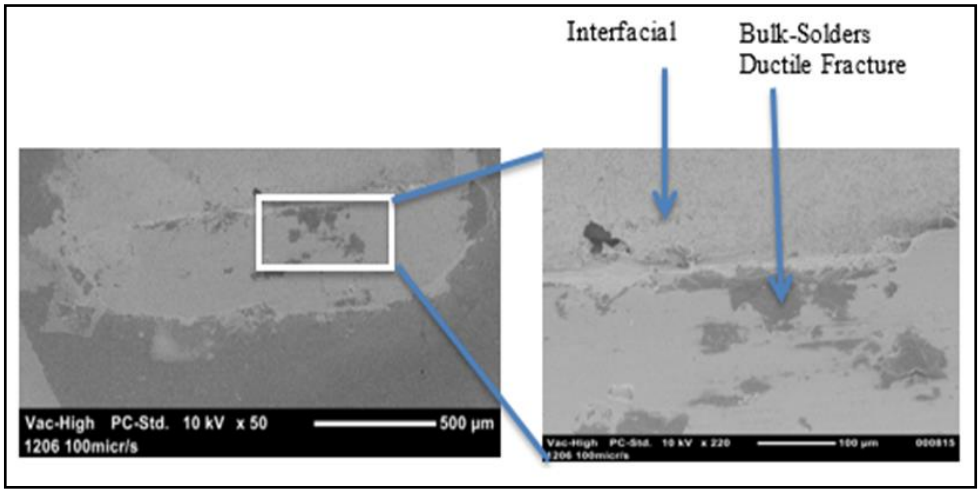


Figure 5.9: SEM Micrograph of non-aged 1206 sheared at 100µm/sec

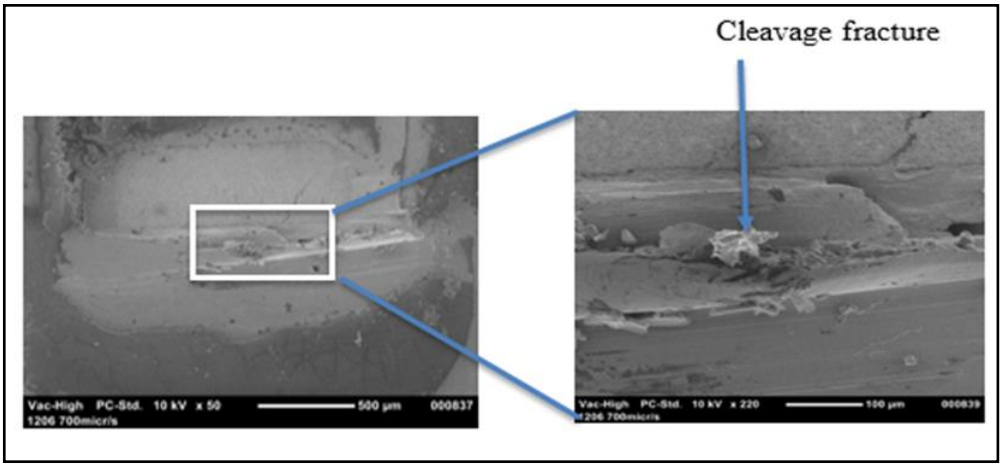


Figure 5.10: SEM micrograph of non-aged 1206 sheared at 700µm/sec

5.3.8 Study on the Fracture Surfaces of Aged Solder Joints

In the magnified view (Figure 5.9 and Figure 5.10) of both micrographs, there are two distinct observed areas for surface texture. The top side is the area, which was underneath the component, and bottom side represents the bulk solder area on the edge of the joint. Different surface texture indicates that the solder joint fractured through two types of fracture modes. The fracture at the area underneath the component was due to brittle interfacial fracture and the fracture happened at the interface between the component and solder. Understandably, the mode of fracture was mainly due to the formation of a weak intermetallic bond between the component and solder. However, the fracture on the component side as observed was ductile in nature and breach happened in the bulk solder, and not on the interfaces. However, and because of the arrangement of the shear tool, the direction and area of the shear influenced the former fracture mode.

Nevertheless, the brittle fracture at the underside (substrate side) of the 'Component' and ductile fracture on the part side (Die/package side) indicates the 'Component' underneath is more vulnerable than any other areas for fracture. By expectation, the brittle fracture mode would dominate at high strain rates. However, Figure 5.9 and Figure 5.10 present similar fracture patterns as observed from SEM despite the fact that they represent fracture surfaces for different strain rates (100 and 700µm/sec). There are two possible explanations for this behaviour. Firstly, the argument was that the solder joint is stiff enough to maintain similar

fracture pattern even at a speed of 700µm/sec. The other argument is that the high strain rate of 700µm/sec was not high enough to induce brittleness in the bulk solder. Figure 5.11 and Figure 5.12 show the fracture micrographs for 1206 components sheared at 100 and 700µm/sec. It was expected that the 'aged samples' would be more brittle than the 'non-aged' samples owing to the development of brittle intermetallic compounds at the joint's interfaces. However, the micrographs did not show any significant change in fracture patterns due to isothermal ageing. The outcome of the result means that the solder joints can sustain the isothermal ageing temperatures up to a range of 150 degrees Celsius and can maintain their structural integrity.

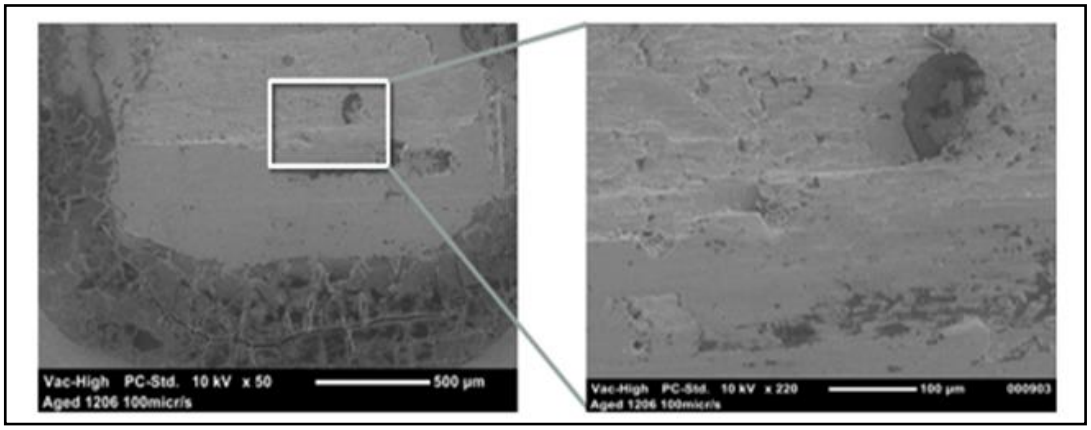


Figure 5.11: SEM micrograph of aged 1206 sheared at 100µm/sec

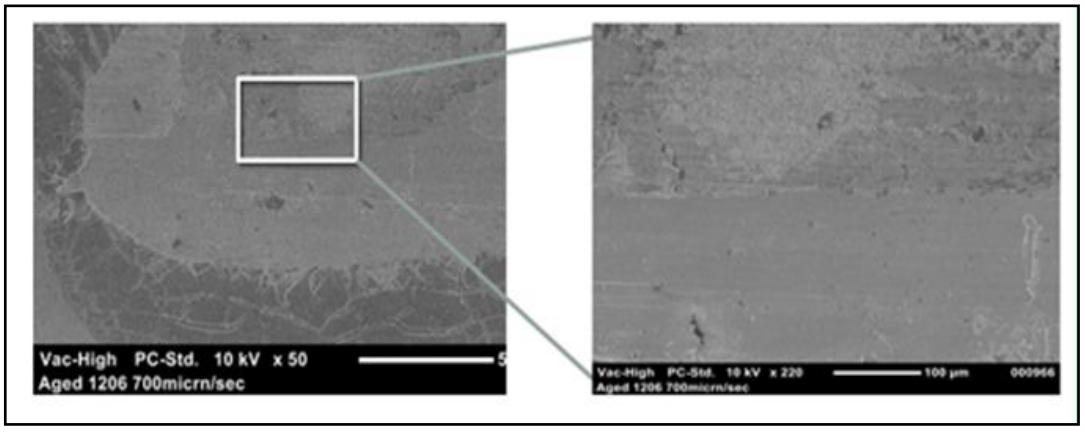


Figure 5.12: SEM micrograph of aged 1206 sheared at 700µm/sec.

This observation, therefore, strengthens the findings from the shear force values where there was no big difference in the 'Shear Force' values of aged and non-aged samples. However, both ‘Dimple Rupture’ and ‘Cleavage Fracture’ surfaces were observed in this investigation, although, they were unlike the observed shear strengths in the 'aged and non-aged' samples since they do not have much fluctuation. It was in expectation, however, that aged samples or samples sheared at higher 'Strain Rate' will be observed with more cleavage fracture due to high brittleness. Nevertheless, non-aged samples or those sheared at low 'Strain Rate' will be found with dimple rupture due to high ductility resulting from low adhesion strengths of solder joint during metallisation. This disparity in behaviour is characteristic of the internal structure of solder itself and temperature gradient during reflow (K. E Yazzie et al., 2012).

5.4 Rare Characteristics Found in the Reflowed Samples Observed

Figure 5.13 shows the Components with Tombstoning effect, also known as Manhattan effect or Chip lifting. It is in author’s suspicion that the cause of the Tombstoning effect was force imbalance due to temperature differences and is a rare feature, observed when numerous SMT components are reflowed or aged. Some of the SJs from the component type ‘0603’ went through this. The Tombstoning effect is caused when surface tension at one side increased and the component stays unconnected to one of the pads.

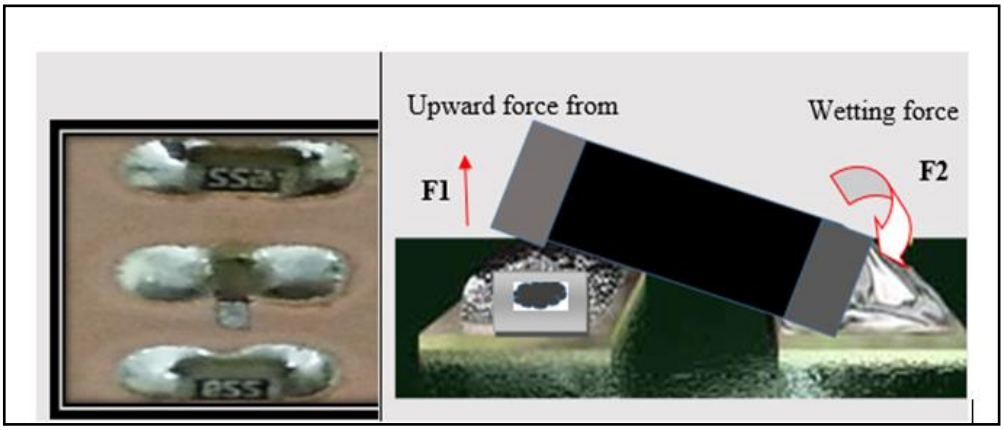


Figure 5.13: Components with tombstoning effect due to force imbalance

During reflow soldering, the metallisation process of the molten solder exerts a self-centring force that aids component alignment, is this same force that contributes to the tombstoning effect. The effect can be avoided using the right placement method with fully processed PCBs

which would help produce a proper energy balance of the wetting forces during reflow soldering (Ip Kee Huit and Ralph, 1995) and (Zhan, Azarian and Pecht, 2008; Lee et al., 2015; Schoeller, 2009). Equation 5.2 gives a characteristic energy balance equation.

$$\textit{Energy Balance}, (E_b) = \frac{(w.h.Ts.\sin(\alpha_w))}{(mg_c(1/2)+y_c)} \tag{5.2}$$

, where:

w = Width of the component

h = Height of the component

Ts = Surface tension of solder

mg = Weight of the component

α_w = Wetting angle

y_c = Component displacement vertical distance, measured from its centre of gravity when rotated to its equilibrium balance point.

5.5 Chapter Summary

The study of the ‘Effect of Strain Rate’ on the thermomechanical reliability of surface mounted Sn-Ag-Cu lead-free Chip Resistor solder joints on Cu substrate, and used in electronic manufacturing is presented in this chapter. In this work, the data obtained from the aged and non-aged samples of the three types of chip resistors used and sheared at different 'Strain Rates' were compared for correlation purposes. The results obtained have demonstrated the significant effects of elevated temperature and 'Shear Rate-dependent deformation' exposure on solder joints. An appropriate mathematical model may be required to predict the variation of the properties with ageing time and ageing temperature. Following the experimental outcome and in the light of the results evaluation and discussions, the key findings from the study are summarised as follows:

- Shear strength of solder joints at room temperature and those aged at 150^0C for 250 hours were found to be independent of the 'Shear Rate' used.

- Similar 'Shear Strength' is observed for ‘aged and non-aged’ solder joints –which implies that solder joints can sustain high-temperature ageing.

- A decreasing trend in the strength values were observed. Hence, the shear strength values are relatively decreasing as the strain rate was increased. The significance of this is that as expected, with elevated temperature ageing, the material and mechanical properties of solder joints if evolved at a higher rate of shear can experience larger changes and degradation at nearly a constant rate.

- Solder joints fractured through both ductile and brittle fractures. There was no observed change in the fracture mode with increasing shear rate and ageing temperature used.

Chapter 6: Effects of Component Standoff height (CSH) on Thermomechanical reliability of surface mounted Ball Grid Arrays Solder joints

6.1 Introduction

This chapter presents a research carried out on the effect of component standoff height (CSH) on Thermomechanical Reliability of solder joints. CSH is the height of the solder joint formed between the die and the substrate. The constituent parts of a CSH include the solder alloy, IMC between the solder alloy and the die, and the IMC between the solder alloy and the substrate. The CSH determines the mechanical integrity of the solder joint formed using the BGA assembly technology presented in Chapter 3, Figures 3.12 and 6.1 for BGA81 components.

In this investigation, two different techniques were used to obtain different CSH: a) varying pad sizes and b) varying reflow peak-temperatures. The former was done using BGA81 components and later with BGA169, the assembly which is presented in Figures 3.13 and 6.2.

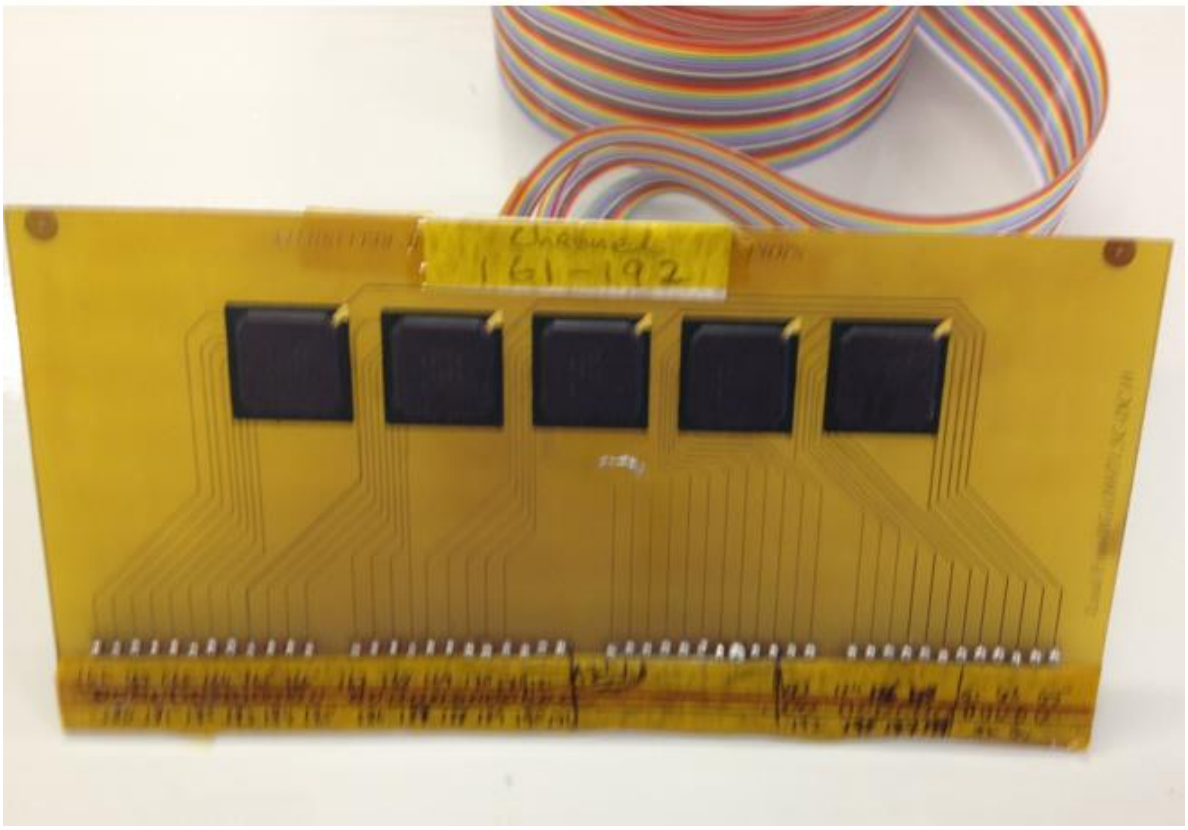


Figure 6.1: Part of the BGA81 assembly technology used for the investigation trial

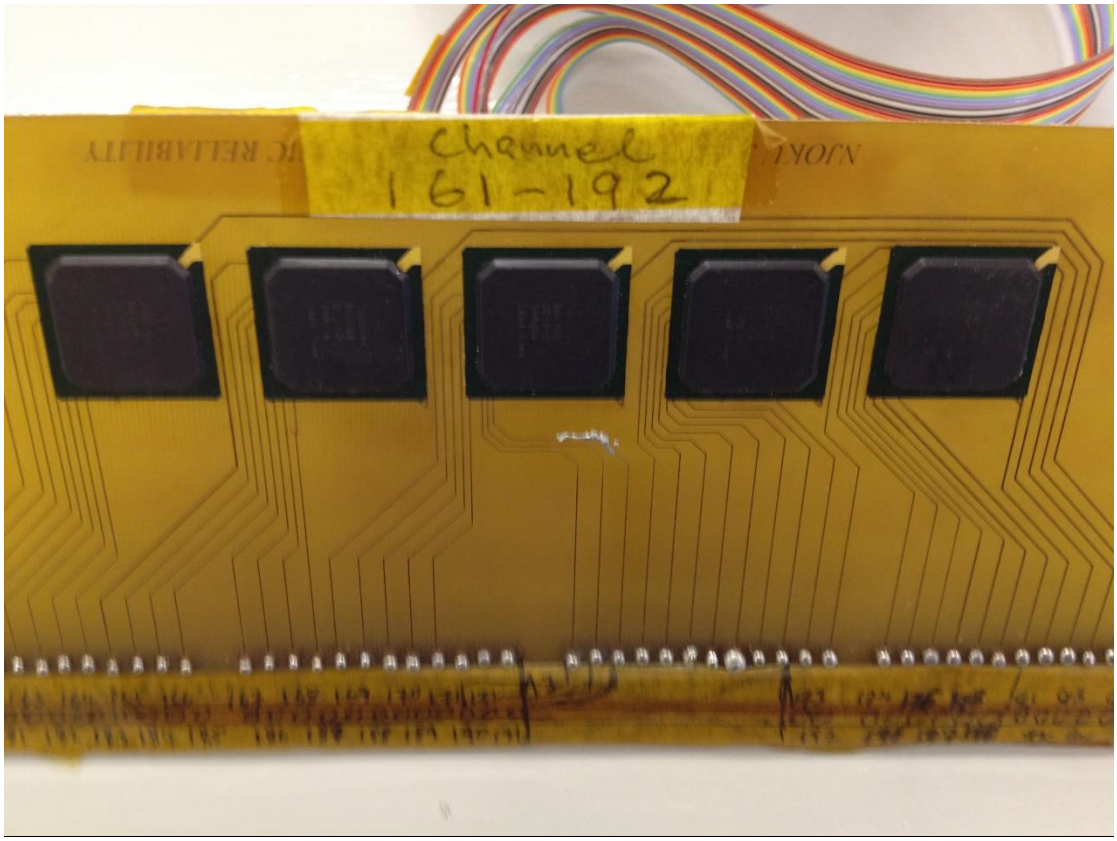


Figure 6.2: Part of the BGA169 assembly technology used for the investigation trial

6.2 Component Standoff Height

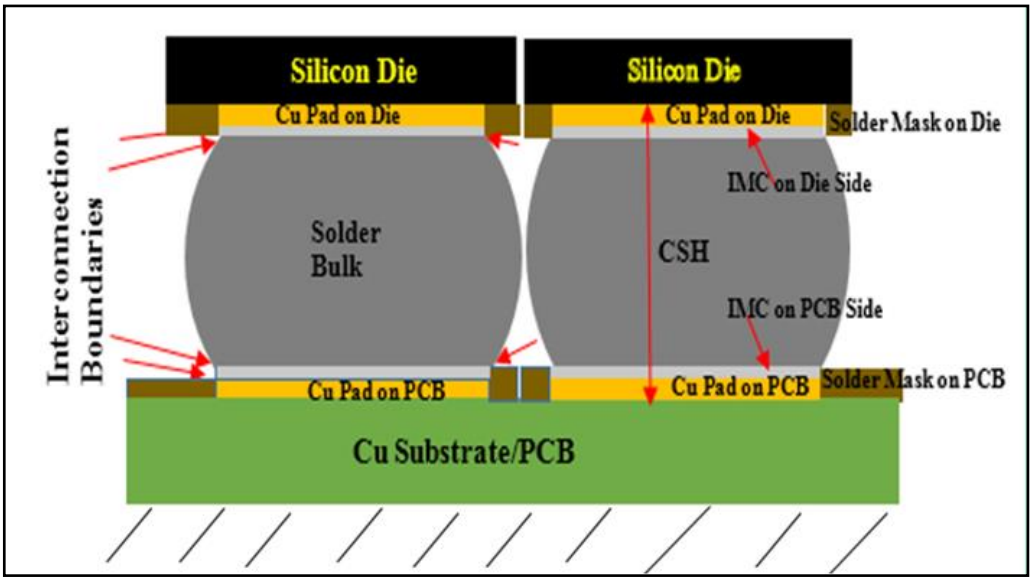


Figure 6.3: Interfacial intermetallic and CSH of solder joint

As shown in Figure 6.3, CSH represents the solder joint height between the component and substrate. It is necessary that the nature and type of the substrate PCB be evaluated to enhance the formation of a good solder joint with outstanding CSH. Research has shown that PCB undergoes a severe deformation during the reflow (soldering) process where the peak temperature drives up to 250°C (Chung and Kwak, 2015). Therefore, it is important to estimate the BGA component attachment on PCB and the PCB deformation at HTEs for thermomechanical durability/reliability after the reflow process. It is also evident that BGA is prone to warpage during surface mount assembly (Vandevelde et al., 2009) and (Njoku, Mallik, Bhatti and Ogunsem, 2015), which produces higher CSH at the corners than the centre of the package.

Consequently, it becomes necessarily important to evaluate the impact of CSH on solder joint reliability. Indeed, CSH has been the focus of many recent studies. Previous research studies suggested that higher CSH offers better thermal cycling reliability. However, (Yao, Qu and Wu, 1999) found that thermally loaded BGAs with taller solder joints will have a shorter life than BGAs with normal shape and size of solder joints. They pointed out that the failure mode of BGAs with thermal enabling load is different from typical BGAs with no thermal enabling capacity, and the former is dominated primarily by bending as opposed to shear.

In another study (Hariharan, 2007), (Ahat et al., 2002) and (Amalu and N.N. Ekere, 2012) looked into the effect of joint height (CSH) on microstructure and tensile strength of SJs made of different solder alloys. Their results showed that CSH influences both microstructure and tensile strength of the joints significantly, but the solder alloys produced different trends, and the results were inconclusive. However, (Lo et al., 2008) and (Sangwine, 1994) studied the effect of bond pad size and shape and package weight on the CSH, using experimental and simulation works. As expected, preliminary results showed a decline in CSH with the increase in package weight. Their numerical simulation result revealed that the CSH is maximised by reducing the bond pad area. Lo et al., 2008 also reported that bond pad shape (circular or rectangular) had minimal effect on CSH.

6.3 Research Design and Experimental Details

6.3.1 Experiment Setup, Procedure and Tests

The experimentation for this study is presented in two parts. The first part outlines the experimental configuration and materials for an investigation with varying pad size, where BGA81 components were used. The second part presents the study with varying reflow peak temperature (and a constant pad size), where the candidate BGA169 components were used. These details as said earlier are found in Chapter 3, sections 3.2.6.1 and 3.2.6.2, Figures 3.12 aand 3.13 respectively.

6.3.2 Experimentation for BGA81 Components with Varying Pad Sizes

The impact of CSH on the reliability of FC-BGAs solder joints was evaluated experimentally using test vehicles comprising of 9x9 full matrix array FC-BGA components of eutectic solder ball configurations, with a ball diameter of 0.36 mm and solder alloy composition of 95.5Sn-4.0Ag-0.5Cu (SAC405). The test vehicles make are from an FR4 epoxy substrate material with tin-plated surface finish. During the surface mount assembly, a no-clean solder flux was rubbed on on the PCB before component placement. The flux will serve as adhesive glue to hold the component in place and as oxide remover during reflow. After the BGAs placement on substrates using an automatic pick-n-place machine, the whole assembly was reflow-soldered using a six-zone convection reflow oven. At the end of the reflow soldering, the shear test was performed using the Dage bond tester. Finally, the measurement of CSH and the microstructure examination process are carried out using SEM.

6.3.3 Experimentation for BGA169 Components with Varying RPTs

In this section, an experiment was conducted using BGA169 components with varying Reflow Peak Temperatures (RPTs) and a constant pad size. The Lead-free BGA169 surface mount devices, which consist of, solder balls made up of Tin/Silver/Copper alloy composition (SAC405) with percentage proportion of 95.5% Sn, 4% Ag and 0.5% Cu, was mounted on FR-4 Substrates. The package ball diameter is 0.76 mm (30 mils) and contains 169 solder balls in each die package. The materials used for the experiment include SnSF FR-4 substrate board of 23×23 mm in dimension, 1.52 mm thick, with 1.5 mm pitch and 0.584 mm (23 mils) pad diameter. Rosin flux application help in placing and aligning the BGA component die on the

substrate boards and for oxide removal during soldering. The pad diameter was kept constant throughout the whole experiment. More details of the materials and experimental test vehicle preparation for BGA81 and BGA169 components are given in Chapter 3, section 3.2.6, and the BGA components are in Figure 3.21 (a) and (b) respectively.

6.3.3 Shear Test of BGA Samples

A multipurpose 4000 series Dage Bond Tester for the BGAs shear test was used for the two types of test vehicles prepared. The test specimens were held in position within a sizeable fixture before the BGA components were 'Sheared' at a 'Shear Speed' and a 'Shear Height' of 200 µm/sec and 60 µm respectively. The shear location is identified in Figure 3.34, Section 3.4.5.1 of Chapter 3. Results of the shear forces were taken directly from a computer system connected to the machine. A detailed description of the multipurpose 4000 series Dage Bond Tester and the shear process for the BGA components is in Chapter 3, section 3.4.5.

6.3.4 Measurement of Component Standoff Height

A 100% measurement accuracy of CSH was also, carried out using SEM presented and described in Chapter 3, section 3.6 and Figure 3.38. The measurement unit of the SEM has a specified accuracy of ±. (0.0030%)(Yunus et al., 2003). For each pad diameter, three CSHs were measured, and their average taken. Figure 6.4 shows sample SEM micrographs of BGA solder ball interconnections.

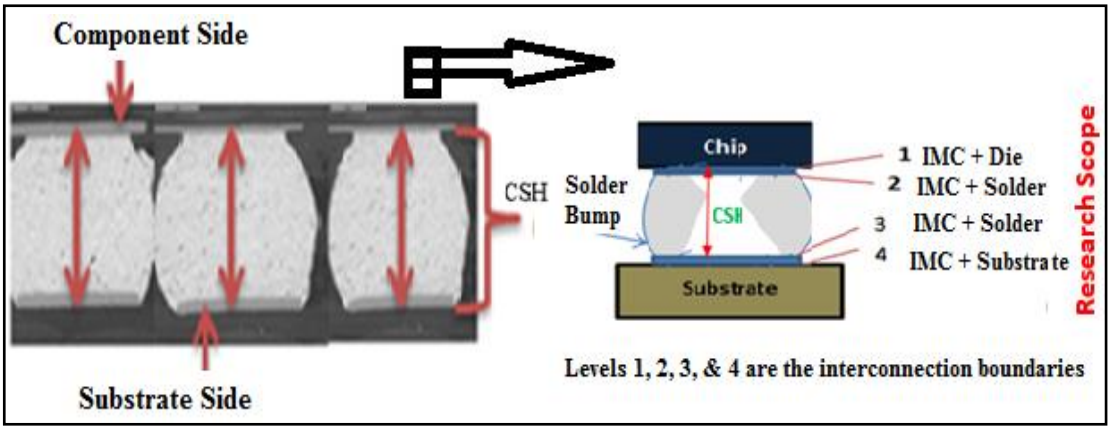


Figure 6.4: SEM micrographs of BGA solder interconnections

6.3.5 Fracture Surface Analysis

The fractured nature of the 'Sheared' solder joints (SJs) was studied using the SEM. It was carried out to reveal additional information on the factors that might be responsible for the failure of the SJs at the application of the shear force. The SEM exposes the microstructure of the solder joints (Figure 6.4) to show the different layers of the solder alloy diffusion into the substrates, types of compounds formed, nature of impurities and to identify bond's defects. The description of the SEM machine for the fracture surface analysis is given in Chapter 3, sections 3.6 and 3.6.1.

6.4 Results and Discussions for BGA81 with Varying Pad Sizes

This article presents results of BGA81 components assembled with varying pad sizes and constant temperature. Six different pad sizes were selected and tested for the integrity of their adhesion strengths, and CSH formed from resulting surface metallisation and metallurgical bonding between the material (solder/substrate) interfaces.

6.4.1 *Relationship between CSH and Pad Size*

Figure 6.5 shows the CSHs as a function of bond pad diameter; and as expected, the observed data show that CSH reduced with increased pad diameter. This finding matches well with the numerical simulation results reported by (Lo et al., 2008), which suggested the maximisation of CSH by reducing the bond pad area. Nonetheless, (Amalu and N. N. Ekere, 2012) have also studied the contribution of CSH on the damage of BGA solder joints subjected to computer-simulated temperature cycling. The paper established the relationship between the CSH and the pad sizes as an inverse proportion, such that:

$$CSH \propto \frac{1}{f(\phi\, pad)} \tag{6.1}$$

The formula in Eq. (6.1), indicates that as the pad diameter increases, the CSH decreases. However, in this experimental study, due to high variations in the data, it is impossible to predict the exact relationship between pad diameter and CSH (Njoku, Mallik, Bhatti and Ogunsemi, 2015).

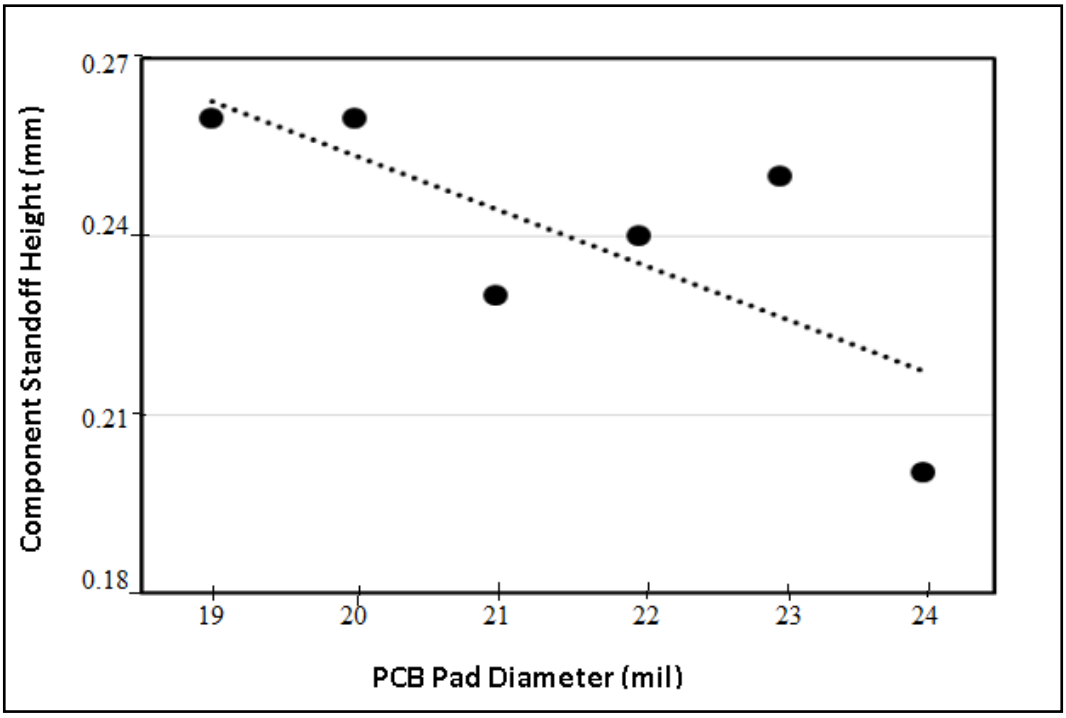


Figure 6.5: Component standoff heights (CSH) of BGA at different PCB pad diameters

Table 6.1: CSH and SSS for as-soldered BGA81 solder joints at varying pad diameters

S/N	PCB Pad Diameter (mil)	CSH, mm	F1 (N)	F2 (N)	F3 (N)	F4 (N)	Average Shear Force(N)	Shear Strength (MPa)
1	19	0.26	439.01	521.74	583.33	612.59	539.16	65.35
2	20	0.26	617.13	663.1	645.83	523.17	612.31	74.22
3	21	0.23	601.81	627.95	683.9	642.26	638.98	77.45
4	22	0.24	644.85	686.47	620.99	632.41	646.18	78.32
5	23	0.25	705.44	724.21	627.4	701.21	689.57	83.58
6	24	0.2	714.62	709.12	693.4	681.18	699.58	84.79

6.4.2 Effect of CSH on BGA Solder Shear Strength

As the primary focus of this study is to find the impact of CSH on solder shear strength (SSS), the measured CSHs are then used for further investigation.

Figure 6.4 shows the shear strength of BGAs solder joint as a function of component standoff height. In this diagram, the CSHs arrangement progressed from low to high values, irrespective of the size of their pad diameters. The data resulted in five CSHs, as the 19 and 20 mil pads produced same CSHs (Table 6.1). The solder shear strength (SSS) values were calculated directly by determining the surface area of the entire 81 solder balls of the BGA package and dividing it by the shear force recorded from the Dage Bond Shear Tester.

Figure 6:6 shows that although BGA shear strength (τ) values showed an initial decline with increasing CSH, such that;

$$\tau_{strength} \alpha \frac{1}{f(CSH)}, \text{ in expectation} \qquad (6.2)$$

However, the shear strength was recovered at even higher CSH. The results indicate that the component standoff height of 0.25 mm is as reliable as 0.2 mm for the designated BGA81 component used. However, the CSH with a data set of 0.25 mm, seems not to fit into the trend and its cause may be attributive to an increase in the wetting angle of the joint leading to an increase in the joint's shear strength. While a decrease in CSH will increase the shear strength as clearly demonstrated in Equation 2.6 of Chapter 2. Notably, the solder joint of BGAs and CSPs typically is a round convex shape, with the joint height determined by the surface tension of solder, pad dimension, solder mask layout around the pad, wetting angle and component weight and these factors combine to influence the SSS.

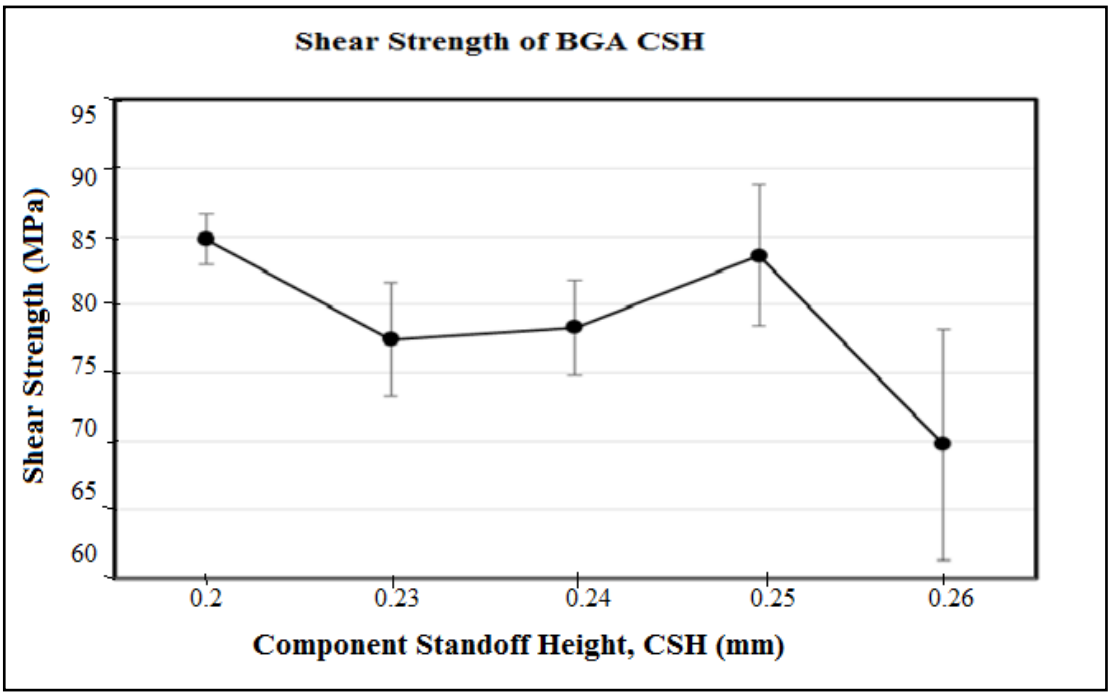


Figure 6.6: Shear strength of BGA solder joint as a function of CSH

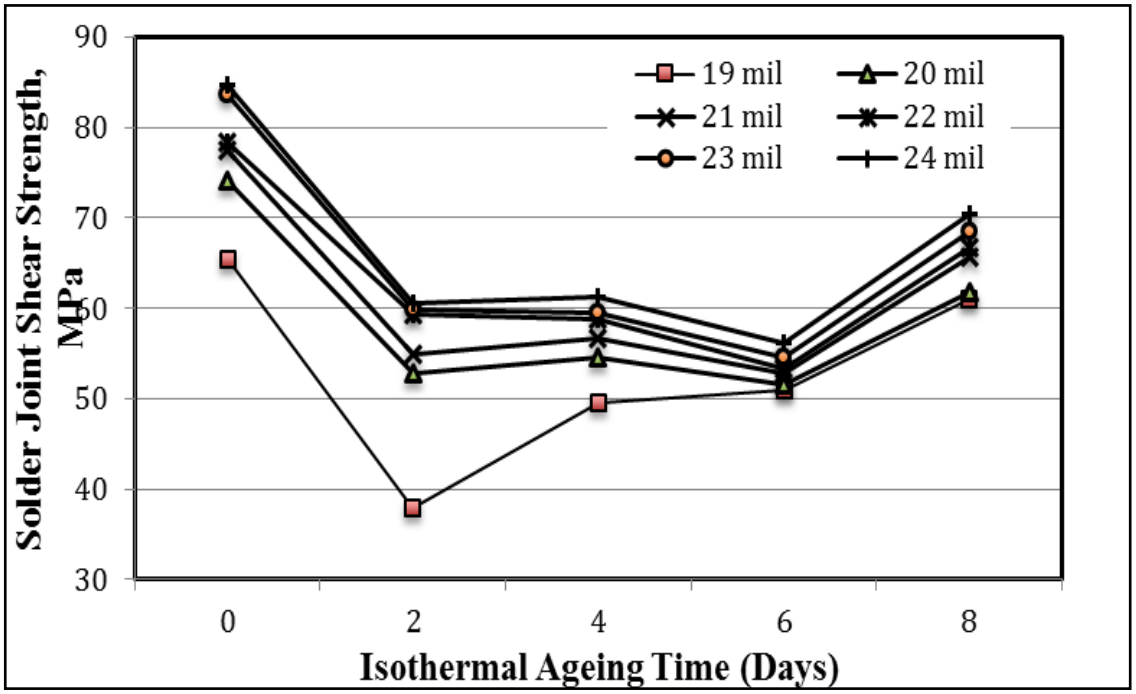


Figure 6.7: Solder joint shear strength as a function of isothermal ageing time (ageing temperature 150°c), for different pad diameters (in mils)

6.4.3 Effect of Isothermal Ageing on Solder Joint Shear Strength

Some of the assembled BGA81 components were isothermally aged at 150°C for up to 8 days. Figure 6.7 presents solder joint shear strength as a function of ageing time, for different pad sizes. The plot demonstrates stress relaxation phenomenon from day one up to the sixth day. Stress relaxation is due to the applied heat annealing the solder materials. The applied heat enables even distribution of pre-stress accumulated in the joints during the reflow soldering process of the component on the PCB. Some reflow profile has 4 minutes cooling time, which is not enough to dissipate all the soldering stresses. Solder material also undergoes significant structural, morphological change during reflow soldering. It observes grain growth.

The size of the grains depends on reflow profile parameter settings as well as the type of paste. Initial thermal ageing provides the needed time and heat for the grain to shrink and for the accumulated pre-stress to become more evenly re-distributed. The grain-shrinking and re-distribution lead to the stress relaxation, which decreases the strength of the solder joint by making it more ductile. After the sixth day, the solder material observes another stage of morphological change. It loses more elasticity and becomes more plastic. The transformation from elasticity through yield region to plasticity accompanies an increase in mechanical strength. In practical terms and as envisaged from environmental conditions, more intermetallic compound may precipitate and disperse in the solder microstructure. The intermetallic compound is reported to grow with an enhanced temperature increase. It is also known to increase the strength of solder joint.

The plot also demonstrates that for all pad sizes, the shear strengths of solder joints follows the same profile. Studies by (Mallik and Mehdawi, 2013), observed a similar trend for Sn-3.5Ag BGA solder joints, mounted on a flexible substrate. The first decrease in the shear strength of the SJs may have resulted due to the coarsening of grains (Xiao, Nguyen and Armstrong, 2004; Koo and Jung, 2007). The coarsening of grains in the microstructure of the solder joints is explained by a process called ‘Ostwald Ripening’ (Rauta, Dasgupta and Hillman, 2009), whereby, solder particles dissolve, and redeposit over time onto larger solder particles. The process is spontaneous and transpires because of the occurrence of bigger and more thermodynamically stable grains than is found in smaller specks. The entire process begins when the little reactions on the surface of the grain structures become energetically less stable than the ones found inside.

However, and owing to the lower surface to volume ratio phenomena, the smaller grains attract higher surface energy than is by larger grain structures. The result of this would be a catalytic reaction that will generate a potential difference at the grain boundaries forcing the molecules from small grains to diffuse through the grain boundaries and attach themselves to the larger ones. The bonding process would result in the continuous growth of the larger grains; the smaller ones in exchange would continue to shrink in their number. The speed at which these particles migrate-to-bond is energy and time-dependent rate. Therefore, grain growth is very slow without the application of sufficient thermal or mechanical energy. Hence, the application of heat energy allows for more rapid movement of molecules through diffusion and increases the speed of grain growth. There is a reduction in the number of grain boundaries because of grain coarsening effect, which allows dislocations (crystal defects) to move smoothly through the boundaries. Because of 'dislocation', however, the solder joints would deform rapidly at much lower shear loads. Also, diffusion allows for more rapid movement of molecules.

The reduced number of grain boundaries (due to grain coarsening) allows dislocations (crystal defects) to move easily through the boundaries, which resulted in the solder joints deformation at much lower shear loads. Also, (Xiao, Nguyen and Armstrong, 2004) reported softening of Sn3.9Ag0.6Cu solder alloy when aged at 180°C. However, the age-softening period was much shorter (1 day compared to 6 days) than what was observed in this study, which might be due to oxidation on BGA pads and of the different solder alloy during ageing, resulting in bad solder joints. After six days of ageing, the solder joints shear strength was found to increase. The rise in shear strength could be from precipitation hardening (Mallik and Mehdawi, 2013). In the related study on the Sn-Ag-Cu solder joints, (Xiao, Nguyen and Armstrong, 2004) also observed the precipitation of hard Ag3Sn particles after one day of ageing at 180°C.

6.4.4 Fracture Behaviour of BGA81 Solder Joints

The fracture behaviours of BGA solder joints as investigated, can fail in various modes. For example, depending on the intensity and speed of applied load, the joint of solder balls could default through pad lift, interfacial fracture (solder/intermetallic or intermetallic/pad) and bulk solder failure (Newman, 2005). Among these failures, interfacial fractures are predominantly brittle, and bulk solder fractures are (tend to be) ductile in nature. However, various researchers (Newman, 2005; Koo and Jung, 2007) also frequently observe solder ball failure through mixed fractures. The mode of solder joints failure and crack propagation was observed to be similar

in some samples but predominantly more in aged samples than it is for as-reflowed test specimens. Results depict IMC fracture on die pad interface, bulk solder fracture and pad lifting or cratering. In most cases, the majority of the solder joints in all the various test specimens observed (for as-reflowed and aged), showed brittle IMC failure or fracture mode after being subjected to a shear rate of 200µm/s. Ductile failure mode in the bulk solder with pad lifting also observed. However, (Biunno and Barbetta, 1999) identified similar results in their advance approach to discovering BGA failure modes using analytical tools such as DMM, SEM and EDS. Also, (Newman, 2005) as well as (Kim, Huh and Suganuma, 2003) pointed out that the thicker the IMC layer, the lower the joint integrity between the solder component and the base metal.

However, the solder bump cut with the die pad during shearing have some traces or small volume of solder left on the PCB pad. The fractured traces were measured for ductility and brittleness. However, the difficult nature of damages found in the surface fracture as shown from Figures 6.8 to 6.11, demonstrate that the failure mode is occasioned by brittle fracture occurring at the boundary connecting the IMC layer and the solder bulk. It also shows that the failure modes are by crack initiation, propagation, and pad lift. The morphology of the failed surfaces is best associated summarily with a brittle fracture. Further observations on most aged samples show that the nature of propagation of the solder joint failure during shearing is strongly impacted also at the boundary of interconnection of the die pad and solder joint, within the bulk solder and at the interface between the substrate pad and solder joint. As discussed earlier, these failure modes are similar to those observed from the as-reflowed test specimens.

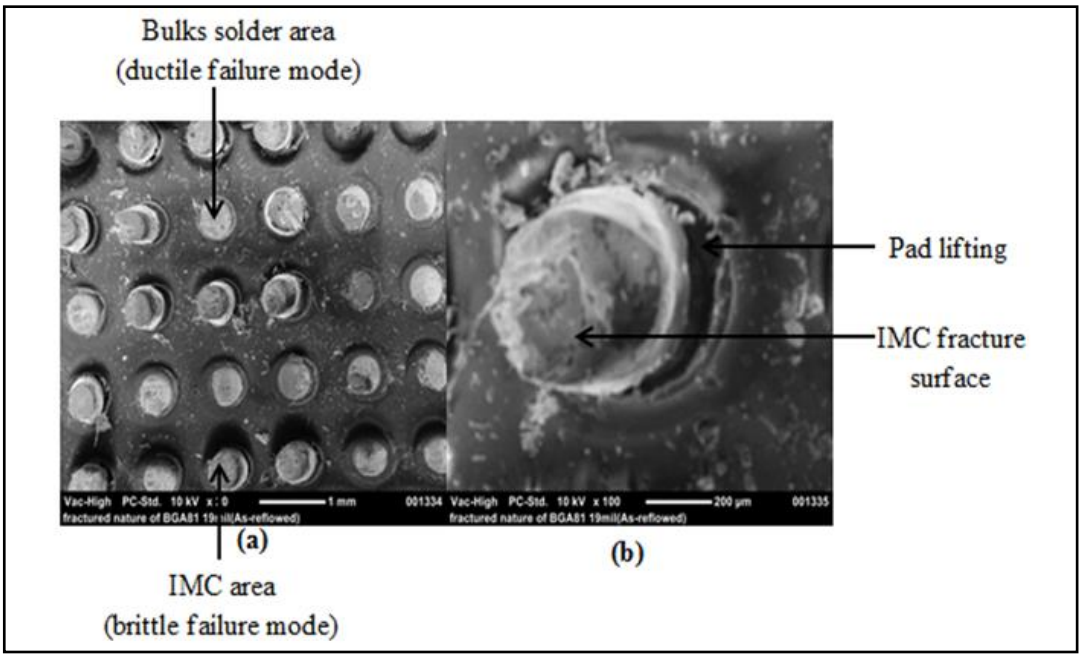


Figure 6.8: SEM of failure mode classification, for as-reflowed 19mil pad, with bulk solder/IMC fracture, (b) IMC fracture and pad lifting

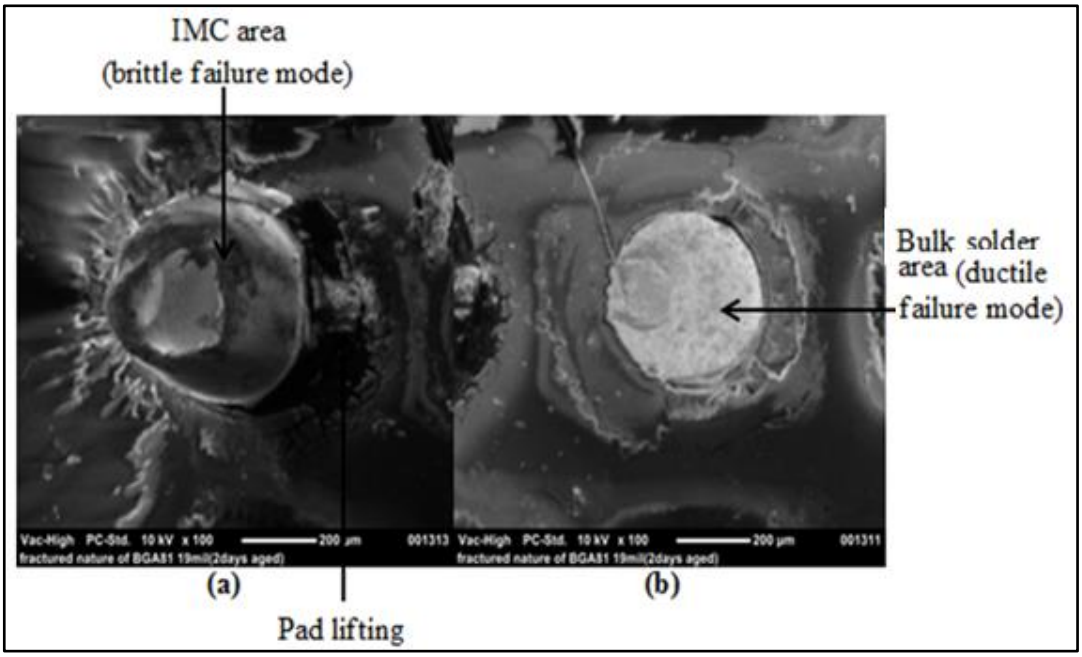


Figure 6.9: SEM images of failure classification, for 2-days aged 19mil pad size, with (a) IMC fracture and pad lifting solder joint, and (b) bulk solder fracture mode

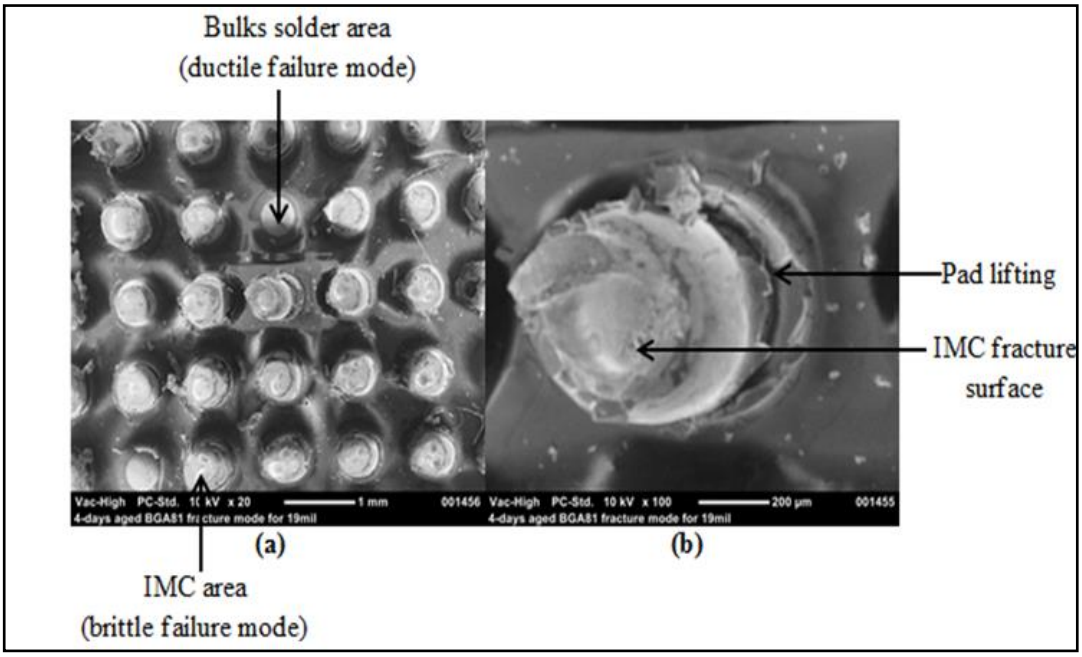


Figure 6.10: SEM of failure mode classification for 4-days aged 19mil pad size, with (a) bulk solder/IMC fracture, (b) pad lifting/IMC fracture

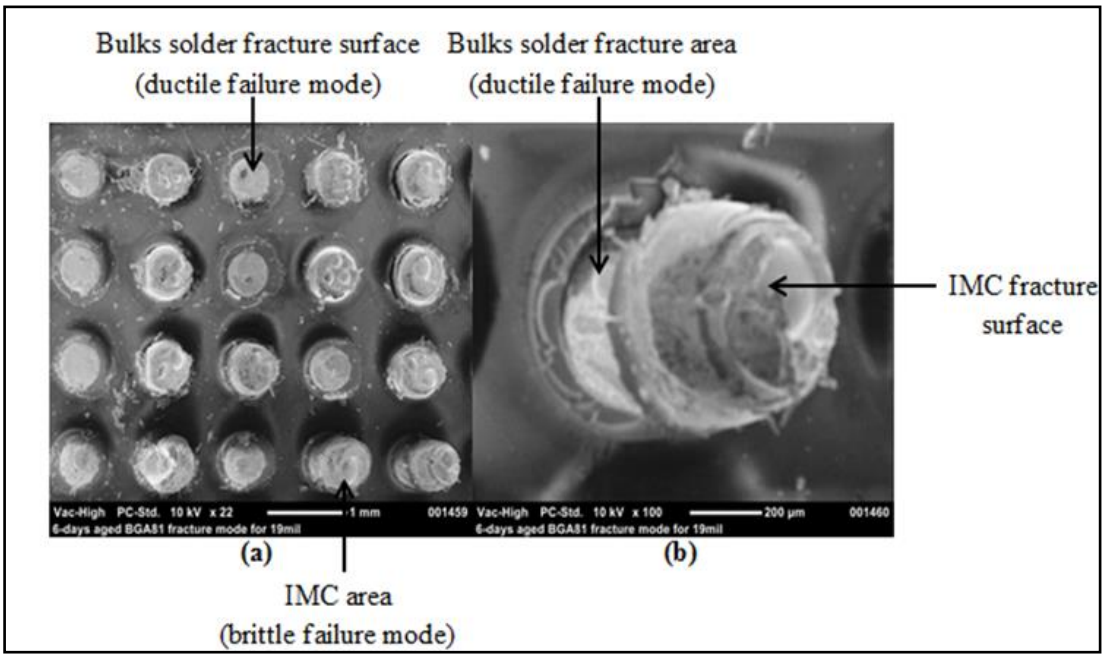


Figure 6.11: SEM of failure mode classification for 6-days aged 19mil pad size, with (a) bulk solder/IMC fracture, (b) IMC/bulk solder fracture

6.5 Results of BGA169 Components with Varying RPTs

This section presents results of BGA169 components assembled with varying Reflow Peak Temperatures (RPTs) and regular or constant pad size. Four reflow soldering peak temperatures were selected and also tested for the integrity of its adhesion strength and CSH formed from resulting surface metallisation and metallurgical bonding between the material (solder/substrate) interfaces.

6.5.1 Effect of Reflow Peak Temperature on Shear Strength and CSH

Table 6.2: Solder joint shear strength and CSH of bga169 as a function RPT

Peak Temp T±5 (°C)	As-Reflow Av. Shear Strength (MPa)	Aged Average Shear Strength (MPa)	As-Reflow Av. CSH (mm)	Aged Av. CSH (mm)
225	26.11	21.03	0.288	0.418
235	32.18	8.29	0.4	0.425
245	25.97	24.53	0.423	0.427
255	27.3	18.02	0.427	0.428

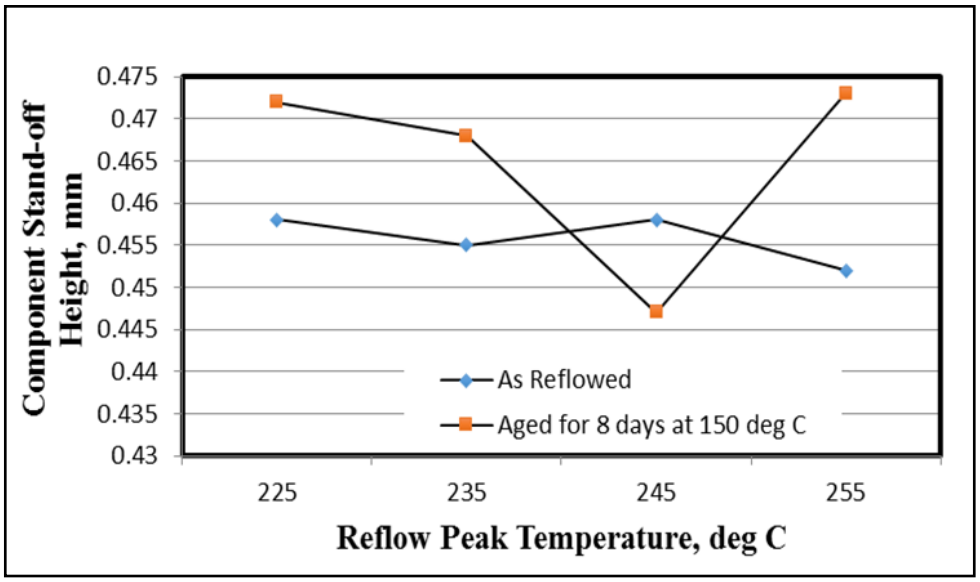


Figure 6.12: BGA169 CSH as a function of reflow peak temperature

Table 6.2 shows that for the peak temperatures 225, 235, 245, and 255°C, the shear strength for 'as-reflowed' BGA169 solder joints (SJs) was higher than those of the thermally aged solder

joints. It implies that the 'as-reflowed' test vehicles were at the considered peak temperatures able to form SJs that are more reliable. However, the lower shear strength values for the thermally aged test vehicles could be because of grain coarsening and IMC layer growth. The more the IMC layer growth, the more brittle the solder joint becomes, thereby leading to the brittle fracture of the aged solder joint at lower shear forces compared to the 'as-reflowed' solder joint. Table 6.2 also shows that the shear force for the 'As-reflowed' test vehicle is with 255˚C at its highest peak temperature. It implies that the proportion of IMC thickness required to form a reliable joint is possible only at the 255˚C peak temperature. The difference in the effect of peak temperature on the shear force is very minute for peak temperature 235 and 245˚C respectively, indicating that the peak temperature has no significant effect on the shear strength of the test vehicles at these investigative and analytical levels.

The results from the Table 6.2 also show the influence of peak temperature on the shear force of the thermally aged test vehicles. The table indicates that the strength of the solder joints reduced because of 'ageing' as compared with the 'as-reflowed' SJs for the test vehicles. The increase in the IMC layer thickness is a consequence of the ageing process and likely to be responsible for this because excess IMC formation results in brittle SJs. The shear strength initially increased between peak temperatures of 225 and 235˚C for the thermally aged samples before dropping as the peak temperature increases along 245 and 255˚C respectively. The best joint for the 'aged' test vehicle as observed from the result was the one formed at the 'as-reflowed' peak temperature of 235˚C. It is so because the difference in the shear strength after ageing is smaller when compared with the other three peak temperatures which have vast differences between the shear force values for as reflowed and aged SJs. The solder joint formed at 235°C has shown that it can operate reliably in actual electronic assembly applications. The joints, when exposed to high-temperature extremes continuously for longer times, would survive the load stress without loss of joint integrity.

A close observation at Figure 6.10 above showed that the peak temperatures from 225 °C to 255 °C do not have any significant effect on the CSH of the as-reflowed test vehicle. The effect of the peak temperatures on the CSH of test vehicle isothermally 'aged' at 150 °C for 200 hours was analysed using the Figure 6.12. The result showed that the CSH obtained was of higher value than that obtained for the 'As-reflowed' test vehicles. It indicates that the ageing of SJs not only weaken them (reduced shear strength) but also deformed them.

6.5.2 Fracture Behaviours of the BGA169 Solder Joints

The solder joints fracture surface after the bond's shear test were examined and analysed using the SEM to view images of the failed solder joint area. The SEM image in Figure 6.13 (a) and (b) shows that fracture occurred at the solder/substrate regions of the IMC for the 225±5°C 'as-reflowed' and 'aged' soldered assemblies. The fracture surfaces were rough along the edges and showed the indications of brittleness along the crack propagation path. The malleable (ductility) portion of the fractured solder joint remained intact on the substrate pads. The joints failed with cracks propagating along the solder/substrate IMC and into the Sn coated substrate pads, resulting in the lifting of about 75% of the pads during the joint's destructive-shear-tests. It shows a good material wetting ability of the solder alloy with the substrates, which is an essential feature of good mechanical and electrical bonding.

At 235±5°C peak temperatures, the 'as-reflowed' solder joint SEM images (Figure 6.13 (c)) showed that fracture occurred from the propagation of a crack along the edges of the solder/substrate part of the joint. The fractured surface shows slightly smooth edges of the solder joint after the damaging (destructive) shear tests indicating a ductile fracture. The crack extended, cutting across about 90% of the pad side of the substrate, indicating good bonding of the solder with the substrate. The aged solder joint (Figure 6.13 (d)) also fractured along the solder/substrate part of the IMC with rough patches of the solder alloy clearly visible on the thin IMC layer over the substrate pads. This phenomenon is similar to the findings by (Alam et al., 2007) whereby solder on the pad side experienced brittle fracture while the solder bulk itself undergoes ductile deformation. The flexible (ductile) nature of the joints confirms the reason for the high shear strength of the solder joint. Figure 6.13 (e) shows that the fractured nature of 245±5°C peak temperature for 'as-reflowed' solder joint displays similar traits to that of the previous peak temperature of (235±5°C). The aged solder joint (Figure 6.13 (f)) fractured across the edges leaving brittle fragments on the edges, but the solder begins to show some signs of ductility as the crack extends towards the centre of the solder joint.

Finally, Figure 6.13 (g) shows the fractured nature of the solder joint for 'as-reflowed' at 255±5°C. The solder joint failed with the propagation of cracks from the centre of the solder towards the solder/die IMC layer region of the joint. The solder joint showed a considerable degree of ductility, which indicates a strong joint that can be reliable, with a shear strength value of 32.18 MPa. The thermally-aged solder joint (Figure 6.13 (h)) experienced brittle fracture along the IMC layer between the solder and the substrate. The brittle fracture is

considered a defect from the result arising from the increase in the IMC layer thickness because of the ageing treatment, which explains the reasons behind the low shear strength of the joint compared to other joints examined. The micrograph of the preceding discussions is found in Figure 6.13, which depicts the nature of failed boundary of the SAC405 BGA169 solder joints mounted on SnSF pads with constant pad diameter and reflow-soldered at varying peak temperatures of 225±5 °C, 235±5 °C, 245±5 °C and 255±5 °C respectively. They were then aged isothermally at 150°C for 200h. The non-aged solder joints microstructures represented by ((a), (c), (e), & (g)), is compared with the micrographs of the aged samples represented by ((b), (d), (f) & (h)) as shown in figure 6.13. For clarity, the enlarged forms of these micrographs are displayed further in sections 6.5.2.1 and 6.5.2.2 (Figures 6.14 and 6.15) for the non-aged and aged samples respectively.

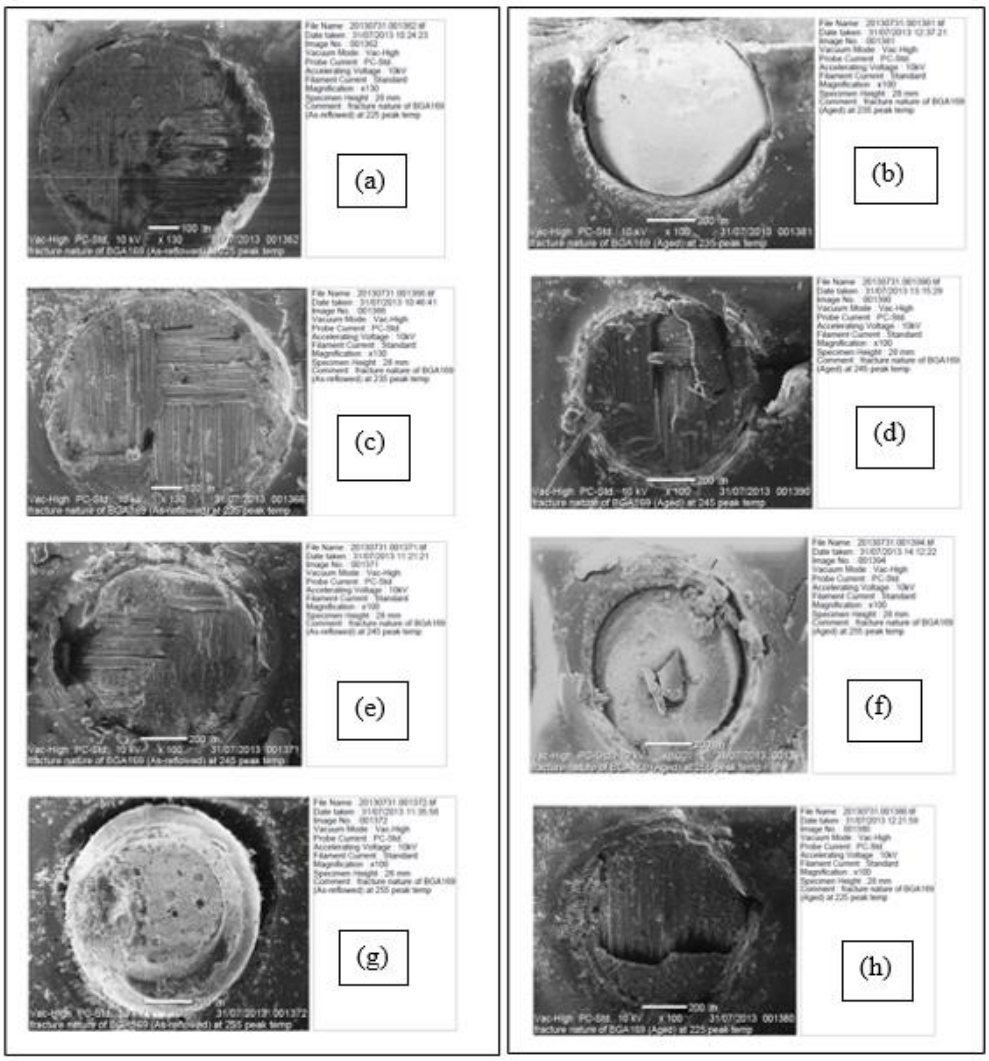
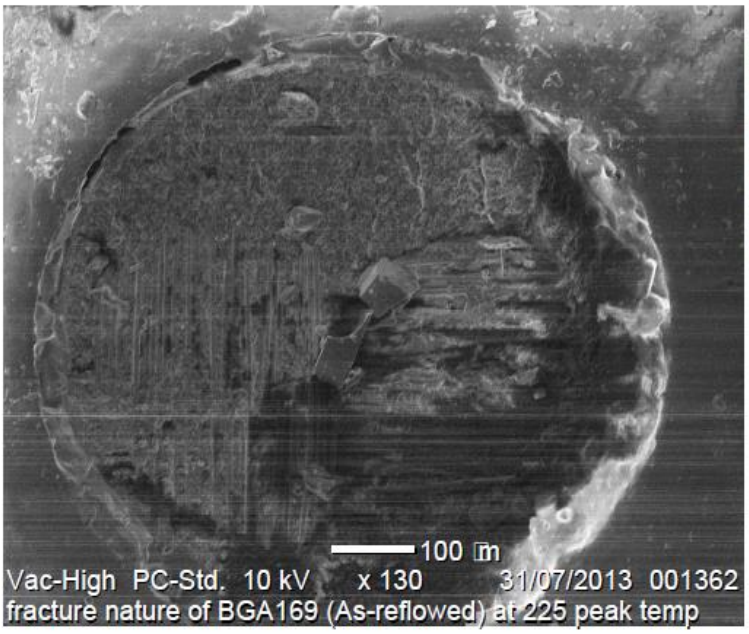


Figure 6.13: Aged and non-aged micrograph of BGA169 solder joints

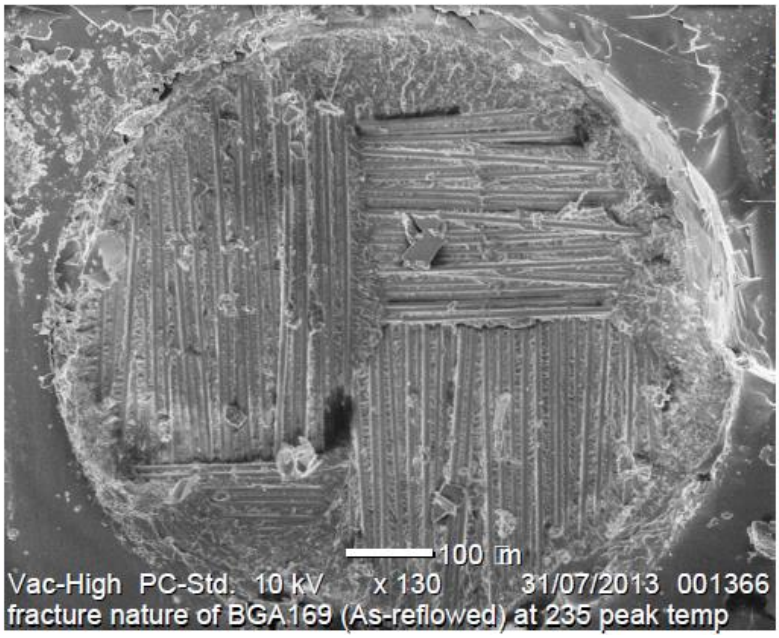
6.5.2.1 Micrographs of Non-Aged BGA169 Samples Enlarged

(a)



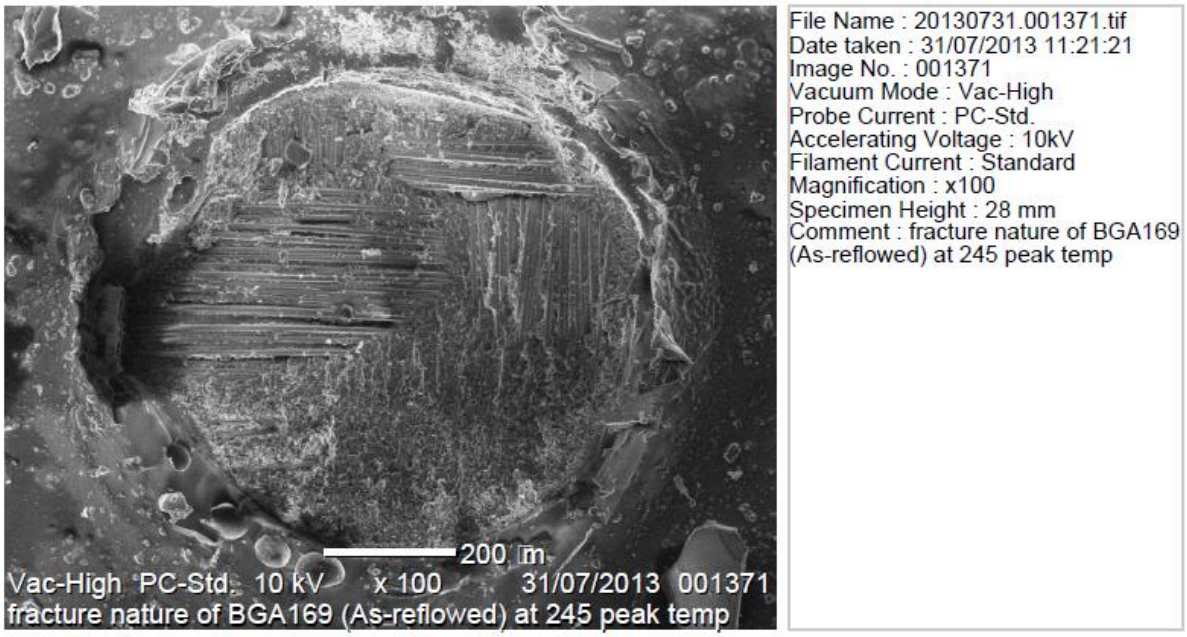
File Name : 20130731.001362.tif
Date taken : 31/07/2013 10:24:23
Image No. : 001362
Vacuum Mode : Vac-High
Probe Current : PC-Std.
Accelerating Voltage : 10kV
Filament Current : Standard
Magnification : x130
Specimen Height : 28 mm
Comment : fracture nature of BGA169 (As-reflowed) at 225 peak temp

(c)



File Name : 20130731.001366.tif
Date taken : 31/07/2013 10:46:41
Image No. : 001366
Vacuum Mode : Vac-High
Probe Current : PC-Std.
Accelerating Voltage : 10kV
Filament Current : Standard
Magnification : x130
Specimen Height : 28 mm
Comment : fracture nature of BGA169 (As-reflowed) at 235 peak temp

(e)



(g)

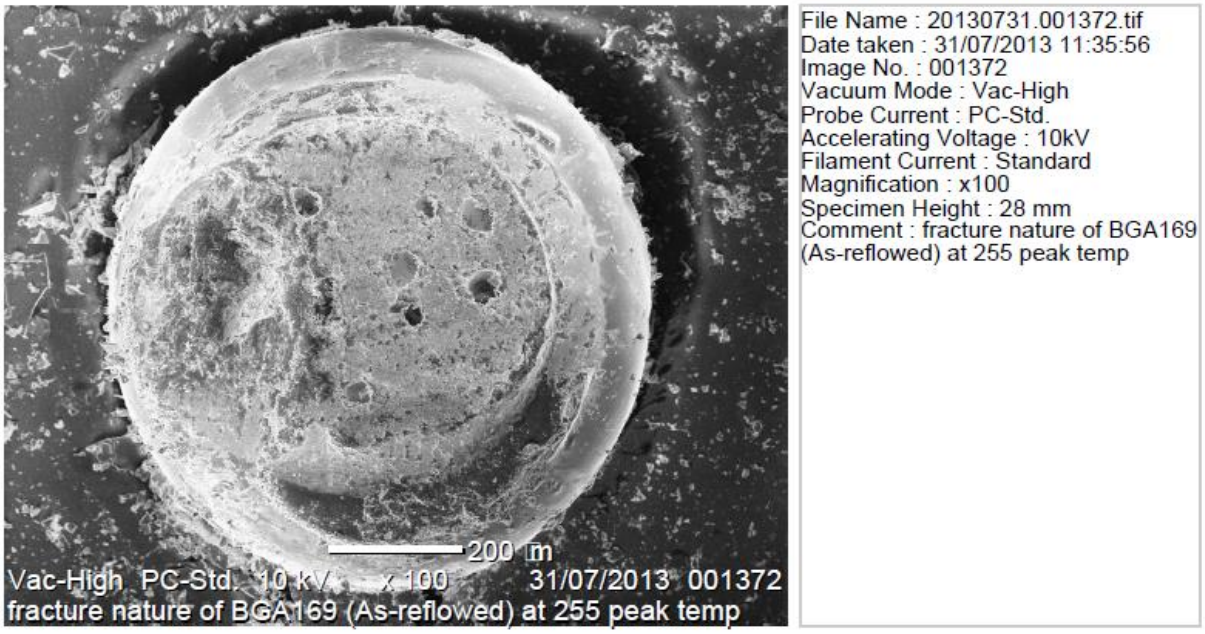
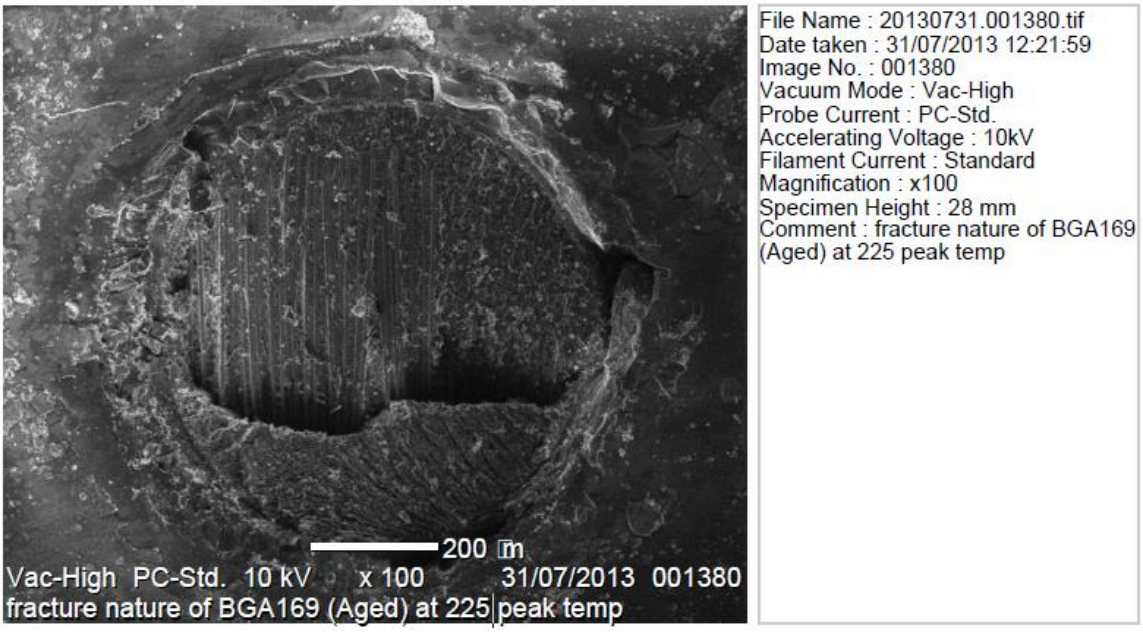


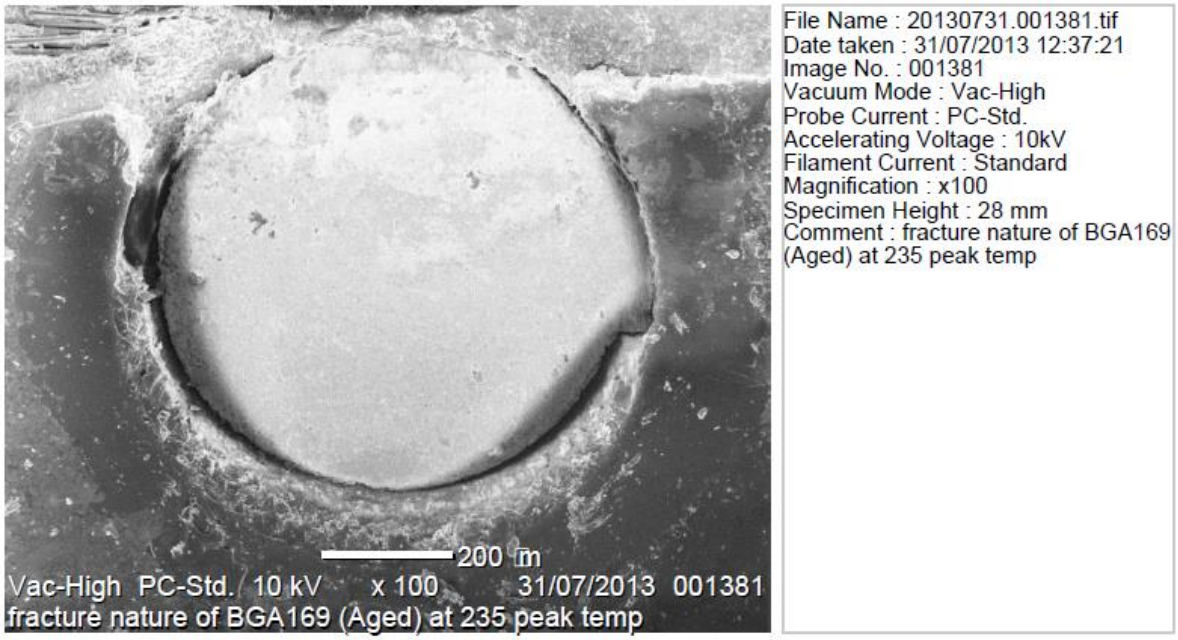
Figure 6.14: Non-aged micrograph of BGA169 solder joints enlarged

6.5.2.2 Micrographs of Aged BGA169 Samples Enlarged

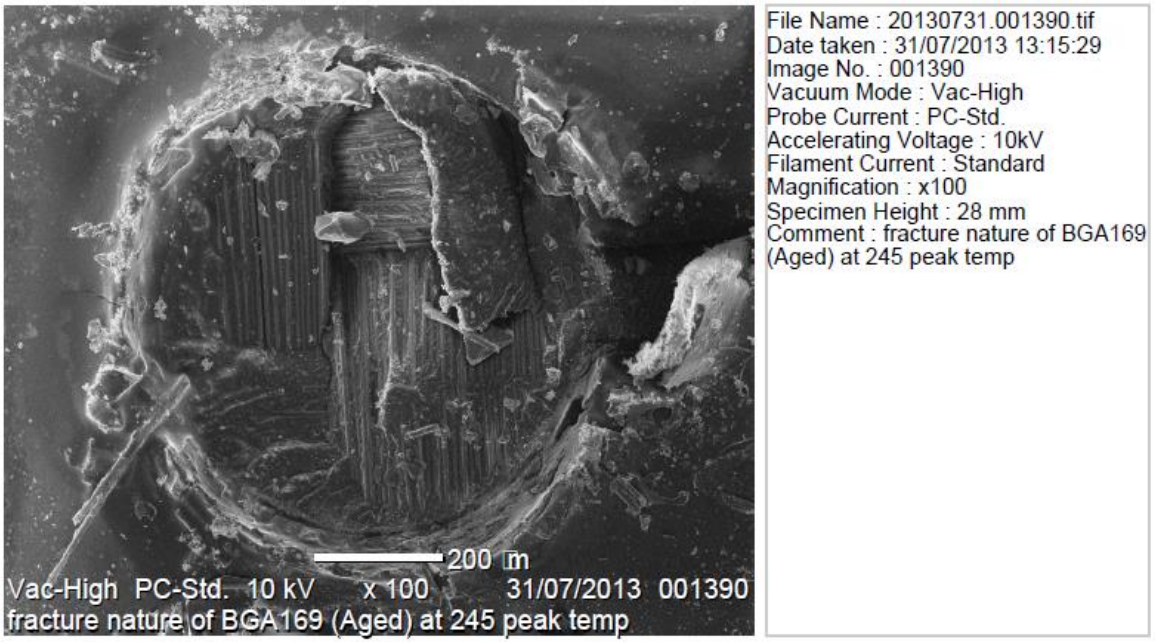
(b)



(d)



(f)



(h)

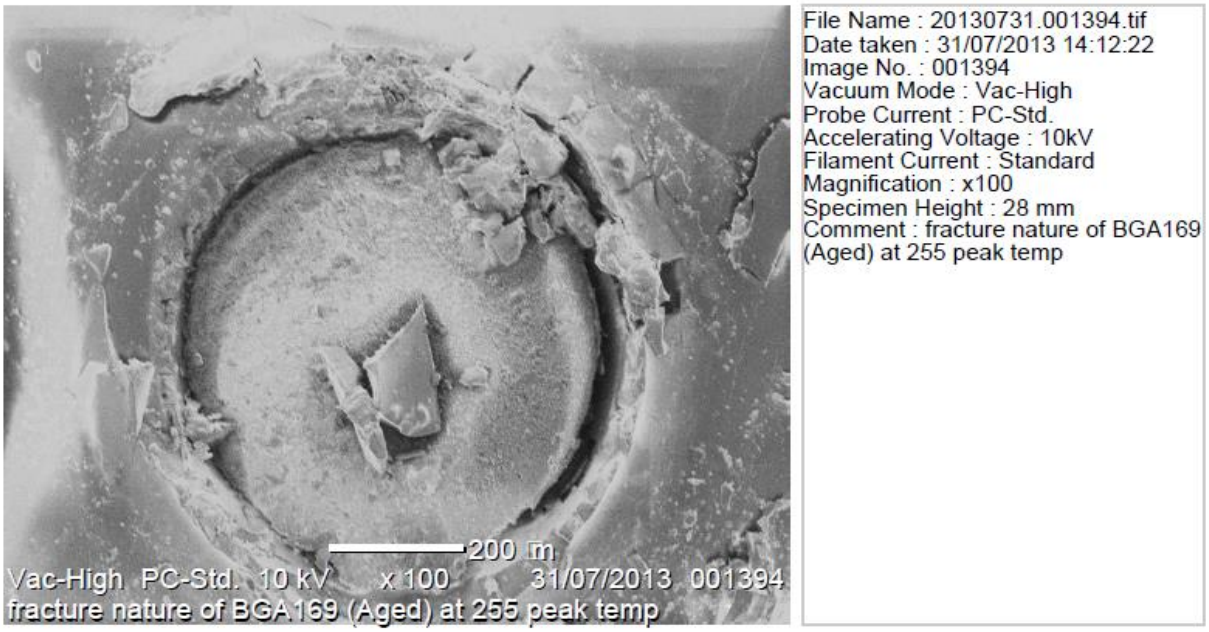


Figure 6.15: Aged and non-aged micrograph of BGA169 solder joints enlarged

6.6 Chapter Summary

This research has demonstrated that varying the bond pad diameter can control the solder standoff height between the electronic components and substrate. The investigation shows that the component standoff height has a significant contribution to the structural reliability of the electronic assembly. In specific terms, the finding from the study indicates that it is possible to achieve adequate and more acceptable solder shear strength at higher component standoff height. Solder joints of components which have higher shear strength will produce assembled device with greater reliability, as such, joints will withstand high shock that electronic devices experience when dropped from a great height. The analysis of the failed joints under shear test, showed that the failure mode is occasioned by brittle fracture occurring at the boundary between the temperature ageing IMC layer and the solder bulk. Another failure mode observed was pad lifting.

The CSH does not on itself influence the shear strength of the lead-free BGA169 solder joint. Its impact on the shear strength is dictated by the reflow-peak-temperature and ageing treatment of the assembly. The reflow of the BGA169 solder assemblies at 235±5°C resulted in the formation of a reliable solder joint with CSH range of 0.423 to 0.427mm, which has a shear strength that does not degrade after subjecting the solder joints to 150°C isothermal ageing for 200h.

The by the microstructure changes introduced by the reflow and ageing conditions influenced the fracture behaviour of the lead-free BGA169 solder joint. The as-reflowed solder joints fail with crack propagation from the middle of the solder towards the die side, while the thermally aged solder joint fail with crack propagating along the solder/substrate IMC region. The as-reflowed solder joints showed more ductile than brittle behaviour on fracture, while the isothermally-aged solder joint showed more brittle behaviour on the fracture. However, achieving balance in the brittle and ductile traits by controlling the growth of IMC is essential for increasing the reliability of the solder joint.

Chapter 7: Effect of Solder Type, Reflow Profile and PCB Surface Finish on Formation of Voids in Solder Joints

7.1 Introduction

It is common sense that increase in voids per unit volume of the solder decreases the joints thermomechanical integrity. Thus, an investigation, which will provide information on techniques and practices to adopt to minimise void formation in solder joints is necessary to improve solder joints thermomechanical reliability. The formation of voids in solder joints of electronic components is termed voiding (Aspandiar, R. F., 2006). Voiding in solder joints is caused by many factors which influence their formation and growth; and these include solder paste type, reflow profile settings and the type of surface finish on PCB. For example, low pre-heat temperature and short pre-heat duration enable the formation of more voids in solder joints. Higher temperature and longer pre-heat ensures that all the volatile component of the solder paste is driven out of the composition. This investigation employs X-Ray technology to determine the number of voids in the lead-free solder joints of the area array BGA package used. The study on the BGA package, however, will provide a better understanding of the science of voids formation in the lead-free solder joints. It will identify the significant factors that enable void formation and will advise on techniques and practices to adopt to minimise voids formation in BGA solder joints to the acceptable limit.

7.2 Research Design and Experimental Details

This chapter presents an investigation, which seeks to determine the effect of solder paste type, reflow profile and PCB surface finish on the formation of voids in solder joints in BGA assembled on substrate PCB. The investigation objectives include but are not limited to:

- Generate experimental designs, using the full factorial DoE, in which paste type, reflow profile parameter settings and PCB surface finish are the control factors.
- Employ three factors on two levels of full factorial designs in the study.
- Determine/identify the combination that will produce the least voids in the solder joint.

Three factors, which include paste type, reflow profile and PCB surface finish, are selected for investigation, and two levels chosen for each factor. The factors and levels used were taken from the literature review. The full factorial DoE planned for this experiment was used to carry

out the investigation. The design consists of eight experimental runs and has its schematic presented in Figure 7.1.

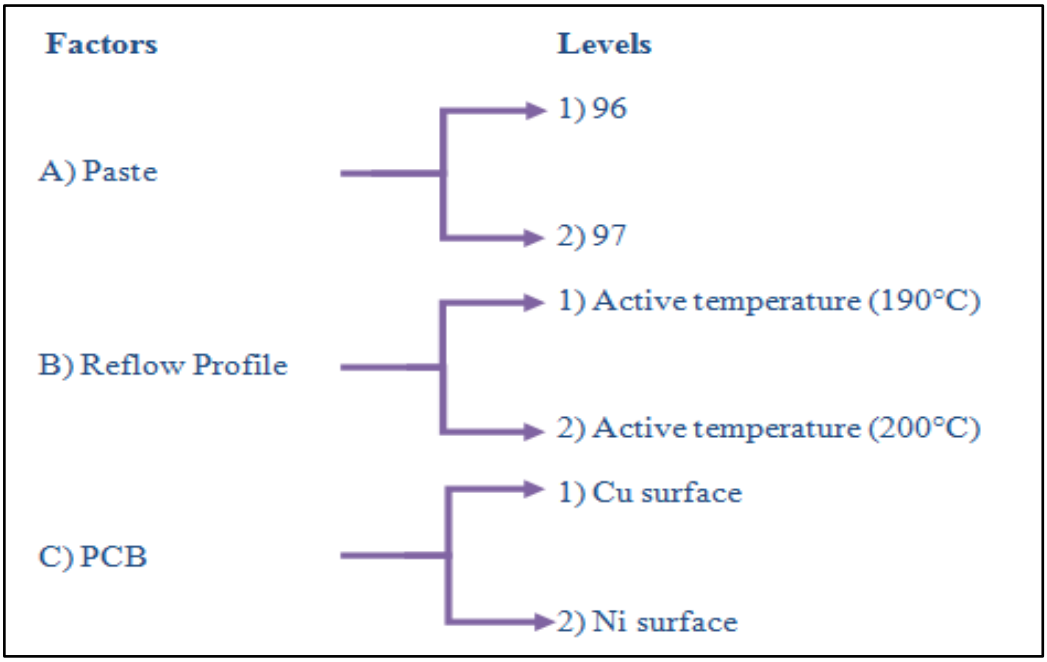


Figure 7.1: Control factors and their level

This design is a three factors on two level design, $2^3 = 8$. The full factorial design is presented in Table 7.1, while Figures 7.2 - 7.5 display the reflow set parameters and the profile used in this experimental study.

Table 7.1: Full factorial design of experiment for the Study

Experiments	A (Paste)	B (R. P.)	C (PCB)
1	1 (96)	1	1 (Cu)
2	1 (96)	1	2 (Ni)
3	1 (96)	2	1 (Cu)
4	1 (96)	2	2 (Ni)
5	2 (97)	1	1 (Cu)
6	2 (97)	1	2 (Ni)
7	2 (97)	2	1 (Cu)
8	2 (97)	2	2 (Ni)

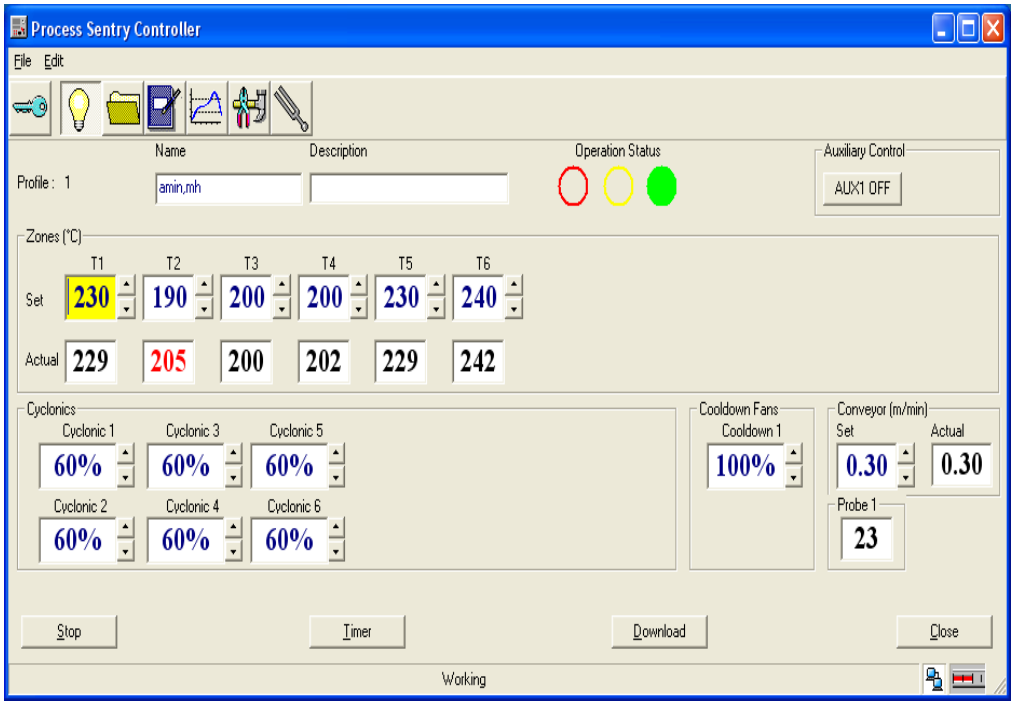


Figure 7.2: Set and Actual temperature of reflow profile 1, given by the system

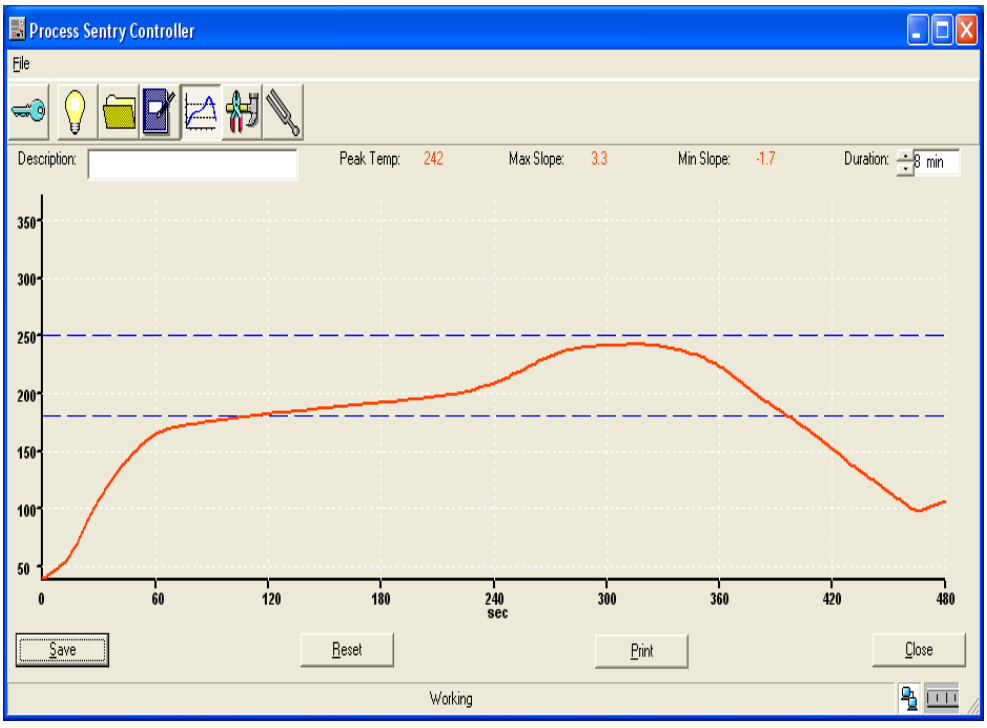


Figure 7.3: The measured reflow profile 1 using a thermocouple**.**

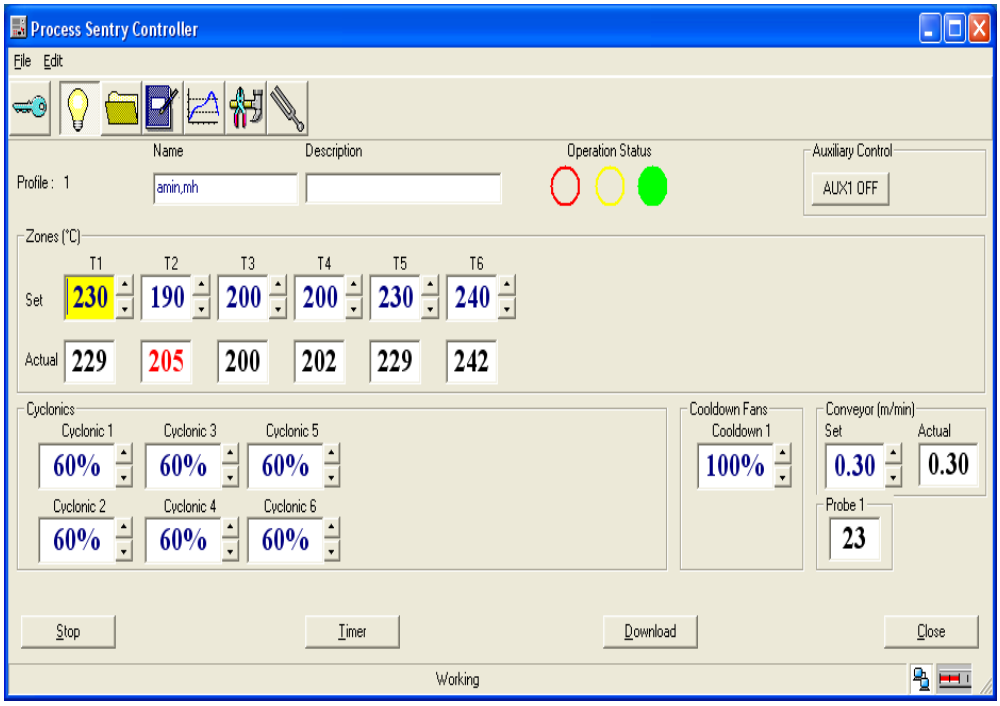


Figure 7.4: Set and Actual Temperature for the Reflow Profile 2, given by the system

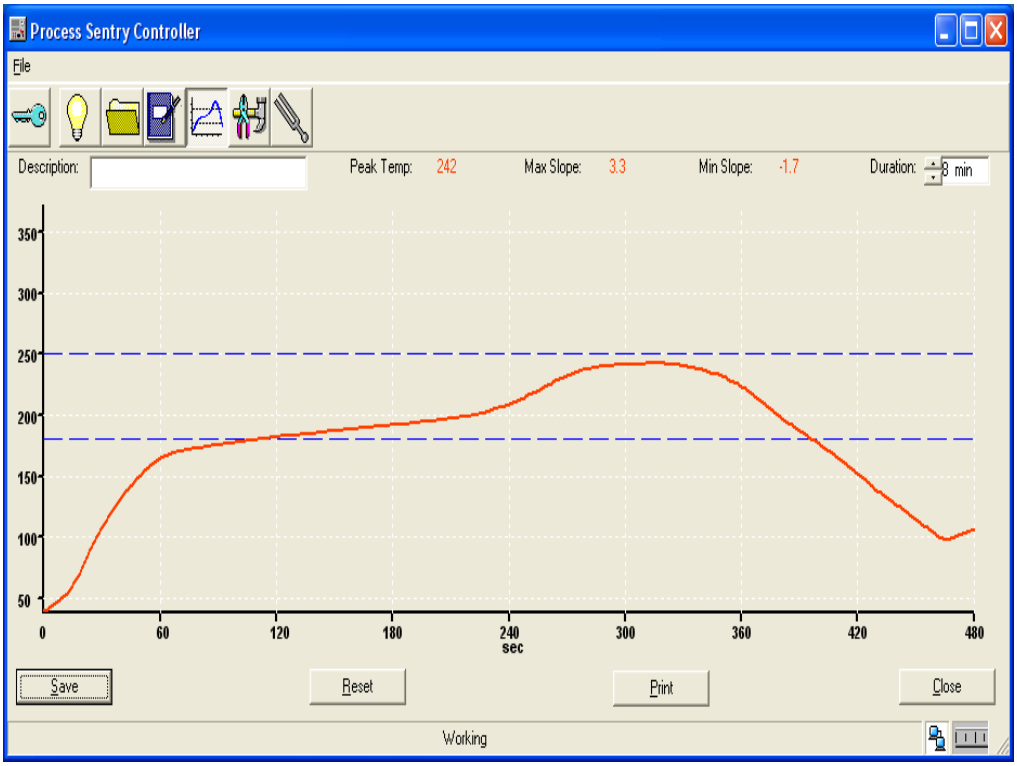


Figure 7.5: The measured Reflow Profile 2 using thermocouple

Although the T1 temperature for the set and the actual temperature is showing about 330°C, the thermocouple-measured temperature is not showing that high temperature. Because terminal 1 was very much outside the temperature impact, about 230°C was set to maintain the expected terminal one temperature. The maximum duration used for the full reflow was 8 minutes. However, the general form of reflow process described in section 3.4.3 is employed.

Notably, the machine has six sections designed to obtain a useful variation of the temperature and the cooling section. First two parts count as a pre-heat terminal, second two sections as an activation section and the final two are the reflow terminal. The cooling section is different on this machine. Each operating temperature can be controlled manually or automatically using the computer system. For safety purposes, it has emergency stop button boldly shown in red. Two different types of operating temperatures were used to conduct these experiments, which are designated 'as-reflow' profile 1 and reflow profile 2. The machine process only starts when the required reflow input conditions are entered in the device. The machine readjusts its component systems to attain the inputted temperature conditions. The test vehicles are then placed in the convection oven for the reflow soldering of the SJs of the assembly. Apart from the reflow set parameters used, two solder paste types with different Particle Size Distributions (PSD) (Zhang, Zhang and Wang, 2010) were selected for the investigation. The pastes are discussed in section 7.2.1 of this chapter.

7.2.1 Type 1 and 2 Solder Paste Used

A report by (Zhang, Zhang and Wang, 2010) states that PSD plays a significant role in the amount and nature of voids formed in solder joints. Thus, two solder paste types with different PSDs were chosen for the investigation. Both of them are AGS particle size three solder paste. They are 96SC LF318 AGS and 97SC LF700 AGS.

The Type 1 solder paste (96SC LF318) consists of 96 SAC (95.4Sn 3.8Ag 0.7Cu, 217°C). LF 318 is a no-clean, lead-free solder paste. Both for reflow and printing. It has a board process window and excellent humidity resistance.The laser-cut, the electropolished, or the electroformed stencils and the metal squeegees are used for the printing process.

The particle size chart is shown in Table 7.2 while the solder paste types are described in two categories as Type1 and 2, respectively.

Table 7.2: Particle size chart

Source: (Mallik et al., 2008, Schmidt et al., 2008; Amalu, Ekere and Mallik, 2011)

Particle Size Chart

Mesh Size	Microns Size	Particle Type
-200+325	75-45	2
-325+500	45-25	3
-400+635	38-20	4
-500	25-15	5
-635	15-5	6

The metal content of the paste is 88.5%, and the particle size is 20-45 µm, and printed on the pad at a speed of 150 mm/s. Similarly, the other solder paste (Type 2) is (97SCLF700) (96.5Sn 3.0Ag 0.5Cu, 217°C). It is also a no-clean solder paste, which has similar characteristics with the former. Full details of the test vehicle, materials, factors and levels used for the experiment is described in Chapter 3, Figure 3.13.

7.3 Results and Discussion

In this section, discussions on void percentage quantification are in two perspectives. These are the theoretical and the x-ray techniques. The theoretical concept treated voids as a spherical entity. The x-ray characterised voids percentage with 'Favourable or Unfavourable' terminologies is derived from statistical analysis and comparison.

7.3.1 Void percentage quantification

The theoretical concept behind the percentage quantification of the proportion of voids in a solder joint bump is on the assumption that the void is spherical and its volume is comparable to the measurable volume capacity of spheres (4/3 * Pi * Radius^3).

Let the volume of void in the solder joint be designated by V_v and expressed as $V_v = \frac{4}{3}\pi r^3$.

Let the volume of the solder joint bump be designated by V_b and expressed as $V_b = \frac{4}{3}\pi R^3$.

Where r and R are the radius of the void and bump, respectively. The expression for the volume fraction, V_f, can be derived thus:

$$V_f = \frac{V_v}{V_b} = \left(\frac{d}{D}\right)^3 \quad (7.1)$$

Where'd and *D'* are the diameter of the void and bump, respectively. For a total of n number of voids in a single solder bump, the total void volume is given by:

$$V_{VT} = \sum_{1=0}^{n} V_{vi} \quad (7.2)$$

If the average volume of the n number of bump is $\bar{V}$, the Eq. 7.2 becomes:

$$V_{VT} = \sum_{1=0}^{n} V_{vi} - \sum n\bar{V} = n\bar{V} \quad (7.3)$$

Substituting Eq. 7.3 in 7.1, obtain:

$$V_f = \frac{n\bar{V}}{V_b} = n\left(\frac{d}{D}\right)^3 \quad (7.4)$$

$$V_f = \frac{n\bar{V}}{V_b} = n\left(\frac{d}{D}\right)^3 \quad (7.4)$$

Eq. 7.4 in percentage is termed void volume percentage,$\%V_v$, and expressed as:

$$\%V_v = 100\,V_f = 100\frac{n\bar{V}}{V_b} = 100n\left(\frac{d}{D}\right)^3 \quad (7.5)$$

Equations 7.4 and 7.5 are the expressions used to determine the volume fraction and the volume percentage of the voids, which is the key principle behind the measurements by the optical microscope. The $\%V_v$ by ordinary mathematical expression, however, and for a single volume of void and uncapped layer of gap, $L_g = (V_b - V_v)$ will be given by:

$$Void\ \% = \frac{V_V}{V_v + Lg} x\ 100\ \% \quad (7.6)$$

7.3.2 Solder Bump categorisation based on percentage of voiding

The percentage of voids in each test vehicle were analysed using an X-Ray machine after reflow soldering of the components on the PCB. Four sample results taken from each PCB surface finish for X-ray analysis were examined. The principle of the analysis is that the x-ray machine utilises the basis of equation 7.4 to determine the void volume fraction in each bump and compares it against a standard critical value. The machine determines the critical value. Based on the comparison, it passes or fails a bump. Similarly, based on the pass rate of the bumps in a PCB, it passes or fails the PCB assembly. The pass is classified as favourable solder bump while fail as unfavourable.

Thus, the analysis identified the experimental runs that produce the highest and lowest percentage of voids in solder joint bump. Consequently, the control factors, their levels and combinations are determined. The categorisation in addition to using the 'favourable or unfavourable' criteria also used the undersized and oversized principles. The schematics presentation of the test vehicle showing the 'Favourable and Unfavourable' Solder Bumped (FSB or USB) balls and 'Undersized and Oversized' balls are in Figure 7.6 and Figure 7.7 respectively. The characterisation and classification of the bumps are with colours.

The key is:

- Pass bumps are coloured green and termed FSB
- Failed bumps are coloured blue and characterised as USB
- Undersized bumps are coloured red.
- Oversized bumps are coloured yellow.

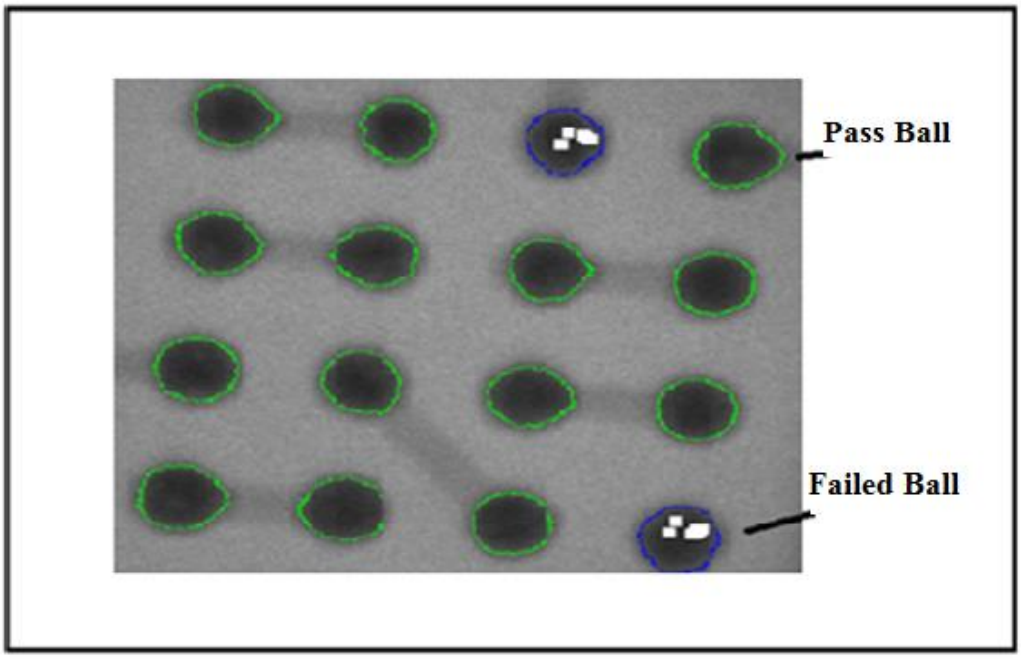


Figure 7.6: Shows a test vehicle with passed and failed bumps in a PCB assembly.

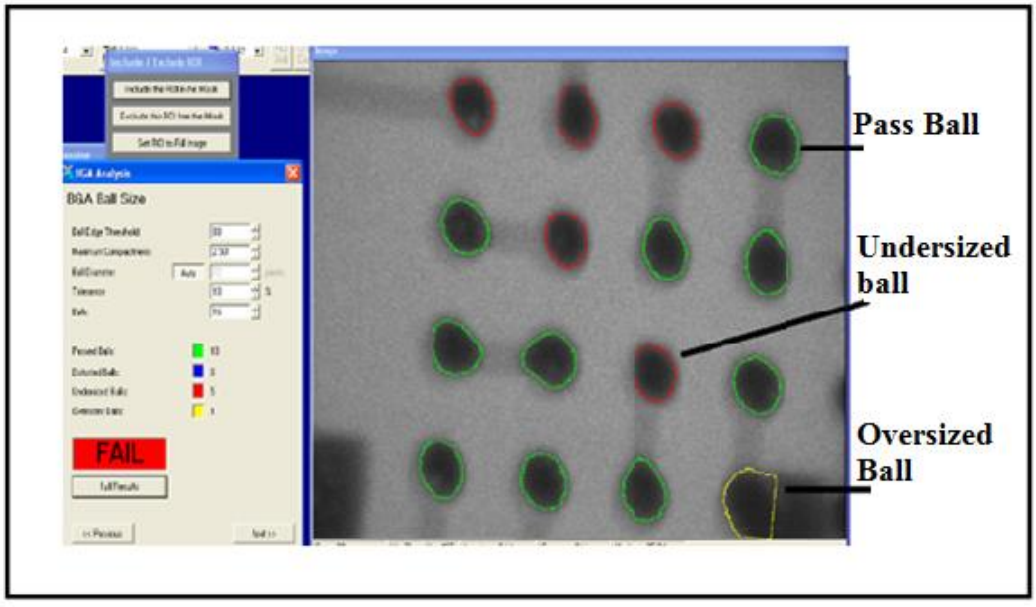


Figure 7.7: Shows a test vehicle with the classified undersized and oversized balls.

During the experiment, 16 balls were selected from each of the corners to analyse the voids. Four results obtained and analysed from each of the setups. The results of the eight experimental runs are presented in Table 7.3 to Table 7.9 for both the FSB and USB joints.

Table 7.3: FSB and USB ball for copper board with paste 96 and reflow Profile 1

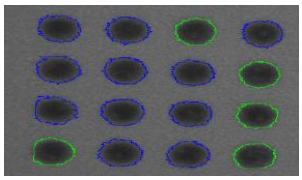
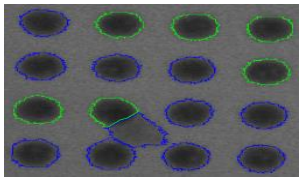
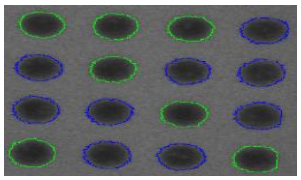
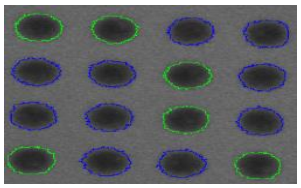
1. 2. Experiment	FSB	USB	Under/Over size SB	Test vehicle Picture
Paste 96 Copper Board Profile Reflow 1 Corner 1	5	11	0	
Paste 96 Copper Board Profile Reflow 1 Corner 2	6	10	0	
Paste 96 Copper Board Profile Reflow 1 Corner 3	7	9	0	
Paste 96 Copper Board Profile Reflow 1 Corner 4	6	10	0	

Table 7.4: FSB and USB ball for copper board with paste 96 and reflow Profile 2

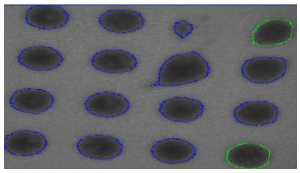
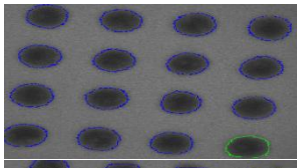
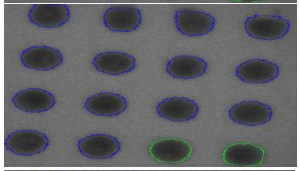
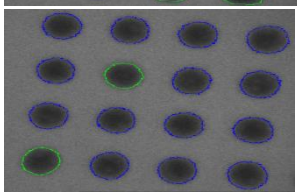
3. Experiment	FSB	USB	Under/Over size SB	Test vehicle Picture
Paste 96 Copper Board Profile Reflow 2 Corner 1	**2**	**13**	**1**	
Paste 96 Copper Board Profile Reflow 2 Corner 2	1	15	0	
Paste 96 Copper Board Profile Reflow 2 Corner 3	2	14	0	
Paste 96 Copper Board Profile Reflow 2 Corner 4	2	14	0	

Table 7.5:: FSB and USB ball for Ni surface board with paste 96 and reflow Profile 1

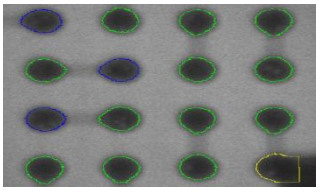
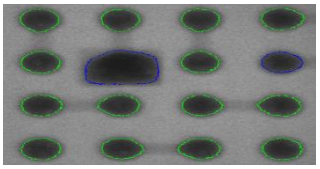
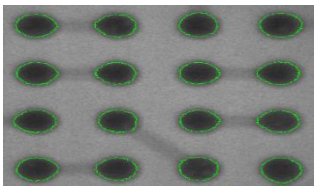
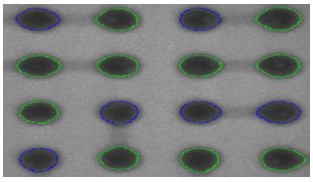
4. Experiment	FSB	USB	Under/Over size SB	Test vehicle Picture
Paste 96 Ni Board Profile Reflow 1 Corner 1	12	3	1	
Paste 97 Ni Board Profile Reflow 1 Corner 2	14	2	0	
Paste 96 Ni Board Profile Reflow 1 Corner 3	16	0	0	
Paste 96 Ni Board Profile Reflow 1 Corner 4	10	6	0	

Table 7.6: FSB and USB ball for Ni surface board with paste 96 and reflow Profile 2

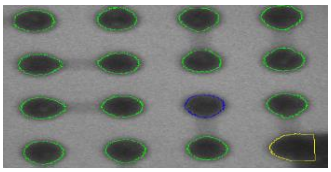
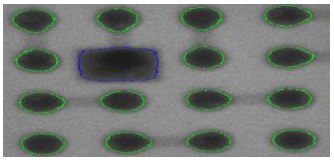
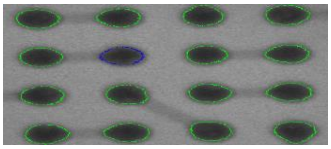
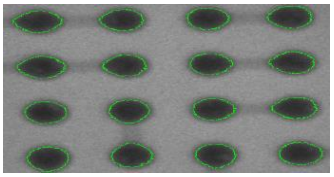
5. Experiment	FSB	USB	Under/oversize	Test vehicle Picture
Paste 96 Ni Board Profile Reflow 2 Corner 1	14	1	1	
Paste 96 Ni Board Profile Reflow 2 Corner 2	15	1	0	
Paste 96 Ni Board Profile Reflow 2 Corner 3	15	1	0	
Paste 96 Ni Board Profile Reflow 2 Corner 4	16	0	0	

Table 7.7: FSB and USB ball for Cu surface board with paste 97 and reflow Profile 1

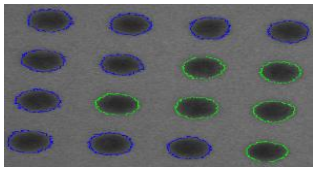
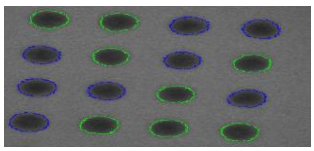
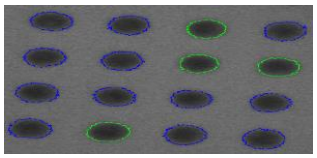
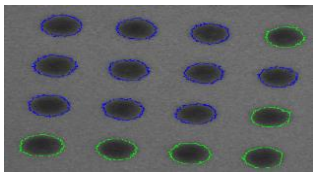
6. Experiment	FSB	USB	Under/Over size SB	Test vehicle Picture
Paste 97 Copper Board Profile Reflow 1 Corner 1	6	10	0	
Paste 97 Copper Board Profile Reflow 1 Corner 2	8	8	0	
Paste 97 Copper Board Profile Reflow 1 Corner 3	4	12	0	
Paste 97 Copper Board Profile Reflow 1 Corner 4	6	10	0	

Table 7.8: FSB and USB ball for copper board with paste 97 and reflow Profile 2

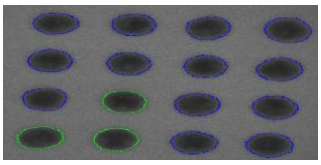
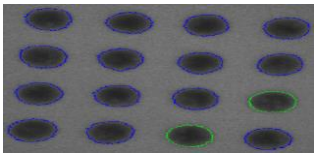
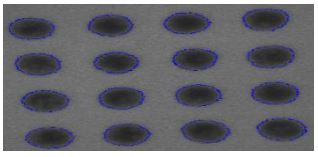
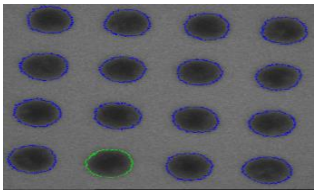
1. Experiment	FSB	USB	Under/Over size SB	Test Vehicle Picture
Paste 97 Copper Board Profile Reflow 2 Corner 1	3	13	0	
Paste 97 Copper Board Profile Reflow 2 Corner 2	2	14	0	
Paste 97 Copper Board Profile Reflow 2 Corner 3	0	16	0	
Paste 97 Copper Board Profile Reflow 2 Corner 4	1	15	0	

Table 7.9: FSB and USB ball for Ni surface board with paste 97 and reflow Profile 2

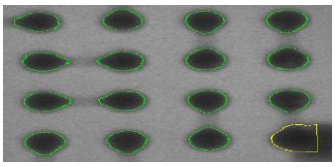
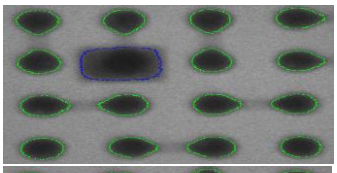
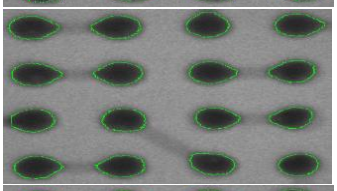
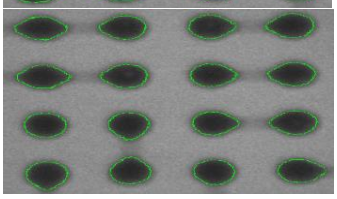
2. Experiment	FSB	USB	Under/Over size SB	Test vehicle Picture
Paste 97 Ni Board Profile Reflow 2 Corner 1	15	0	1	
Paste 97 Ni Board Profile Reflow 2 Corner 2	15	1	0	
Paste 97 Ni Board Profile Reflow 2 Corner 3	16	0	0	
Paste 97 Ni Board Profile Reflow 2 Corner 4	16	0	0	

Table 7.10. Provides the summary of the presentations in Table 7.3 up to Table 7.9 respectively.

Table 7.10: Experimental data using full factorial design method.

Expt.	A(paste)	B(RP)	C(PCB)	R1	R2	R3	R4	Ave. FSB	% of FSB
1	1	1	1	5.00	6.00	7.00	6.00	6.00	37.50
2	1	1	2	12.00	14.00	1600	10.00	13.00	81.25
3	1	2	1	2.00	1.00	2.00	2.00	1.75	10.93
4	1	2	2	14.00	15.00	15.00	16.00	15.00	93.75
5	2	1	1	6.00	8.00	4.00	6.00	6.00	37.50
6	2	1	2	10.00	13.00	14.00	15.00	13.00	81.25
7	2	2	1	3.00	2.00	0.00	1.00	1.5.00	9.375
8	2	2	2	15.00	15.00	16.00	16.00	15.50	96.88

The observed information from Table 7.10 indicates that experimental run 8 has the highest average FSB pass rate while experiment run 7 has the worst FSB pass rate. It means that for a minimum voiding in solder joints to occur, the solder paste, reflow profile and PCB pad surface

finish should all be at level 2. Thus, the paste should be 97, and the activation temperature should be 200^0C while the pad surface finish should be Nickel. A bar and line graph model chats for the experimental outcome are further presented in Figure 7.8 and Figure 7.9.

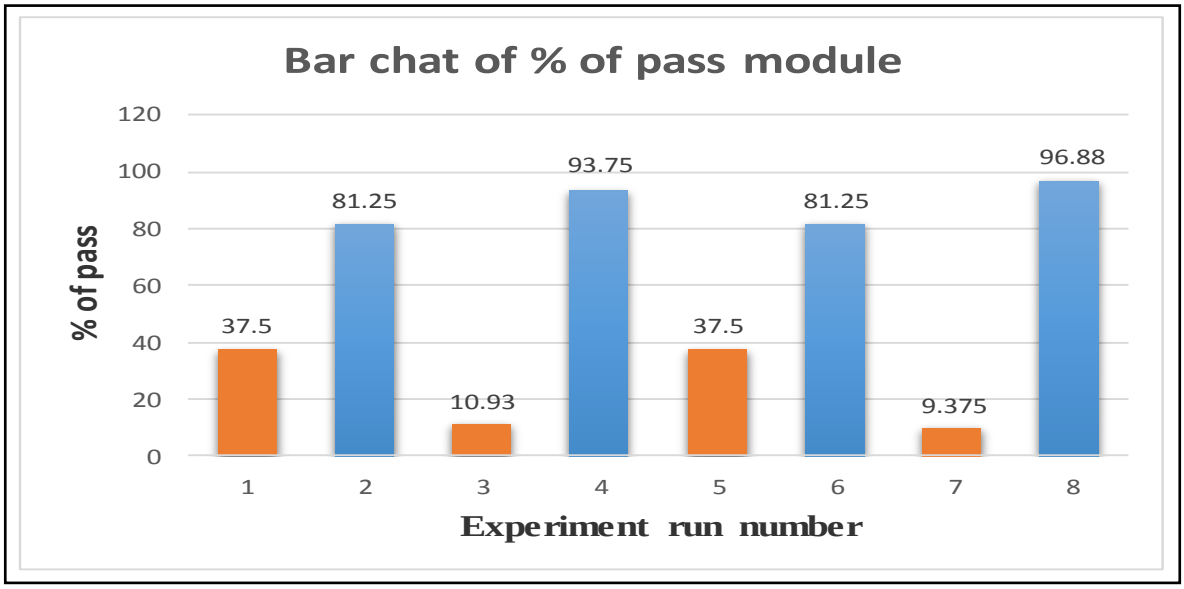


Figure 7.8: Bar chart of experimental run number vs. percentage (%) of FSB/pass

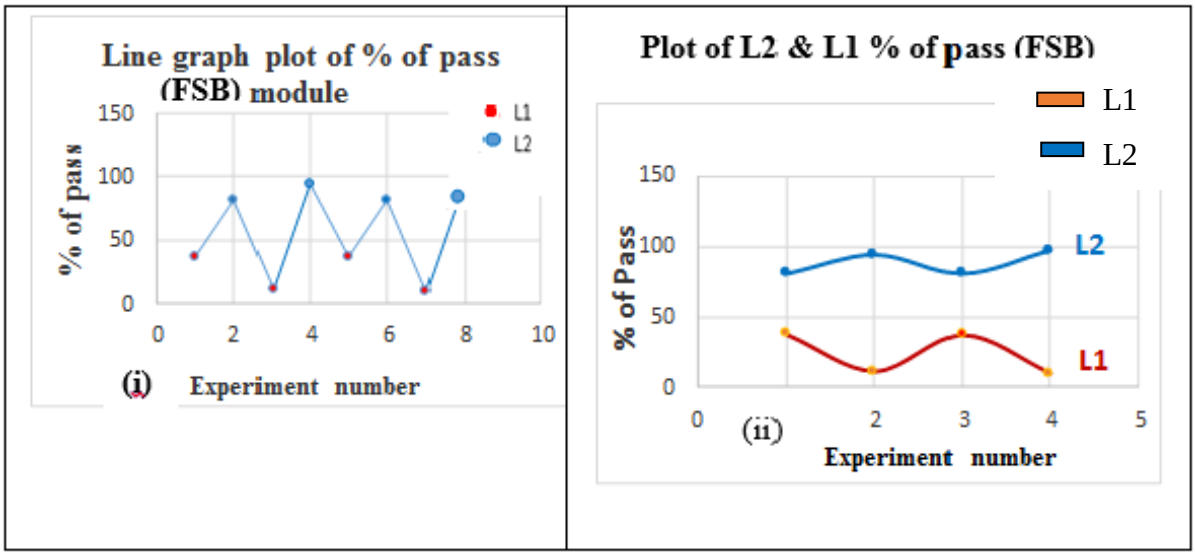


Figure 7.9: Line graph plots of experimental run number vs. % of pass (FSB)

The figure thus provides evidence that level 2 of the two levels compared remains a defining and most significant experiment run factor (2, 2, and 2). The level 2 has an FSB percentage

pass with a substantial reduction in voids in the area array solder joints used. This information can be useful to assembly industries and component manufacturers for product optimisation. The reduction could have been caused by high peak reflow profile activation from elevated temperature and the nature of the solder flux/paste chemistry used; as one material shows less voiding in test samples than its alternative. Also, due to thermal heat convection in solder joints, metallisation processes and diffusion of metallic oxides that occur during reflow soldering, voiding can be a pool of high uncertainty. For this reason, the results of the CTE mismatch, the spread of molten solder flux and the growth of intermetallic can be almost unavoidable as depicted in Figures 7.8 and 7.9. The graph varies in both solder paste activator levels, and these may have resulted from temperature gradient experienced by solder paste during the reflow process. The worst case scenario for level 1 occurred at experiment run number 7 while for level 2 occurred both at two and six respectively.

Literature survey found that voids have an affinity to accumulate around the interface between the package component and the solder joint base metal. Also, voids of larger size forms at the interface, and the position has the potential to increase stress concentration. Stress risers degrade both thermal and electrical performance of solder joints. Void location leads to a reduction in the cross-sectional area near the bonding interfaces and can adversely affect the reliability of solder joint during operation. Hence (Previti, Holtzer and Hunsinger, 2011) in their study on the four ways of reducing voids in BGA/CSP packages to substrate connection opined that zero voids though hard to achieve had remained an important key factor influencing the effect of voids on solder joints reliability performance.

Furthermore, Previti et al. (2011) also consider soak zone as the most challenging and critical part of the reflow profile which could help to reduce voids and may constitute a source of possible and greatest area of defects. However, the solder paste/flux constituents may deplete if extreme soak temperature (usually160 to 180 ^{0}C) are applied, which might lead to eventual solder powder re-oxidation of the solderable surfaces causing improper coalescence, head-in–pillow and voiding in the solder joint. In the event of very low soak temperature, the flux chemistry may either be fully utilised or be activated resulting in excess residues and improper solder wetting characteristics due to lack of device de-oxidation which may be moisture sensitive. Nevertheless, further investigations by industries have shown that solder joint integrity is not impacted by the effect of voids unless they fall into particular geometry configurations and or location.

7.4 Chapter Summary

This research has presented the effect of solder type, reflow profile and PCB surface finish on the formation of voids in solder joints in electronic assemblies. The need to minimise the presence of voids in solder joints of electronic assembly is studied. Thus, this investigation has presented technique which when utilised can result in the production of solder joints in electronic assembly with least percentage of voids. The investigation has demonstrated that paste type, activation temperature used in reflow soldering process and the pad surface finish on the substrate PCB all play a part in determining the percentage of voids in solder joints of the electronic assembly. Besides, the results of the study show that for minimum voiding in lead-free solder joints of Ball Grid Array, the paste type 97 should be used instead of type 96. However, an activation temperature range of 200 degrees Centigrade should be utilised instead of 190 degrees Centigrade and a Ni surface finish on the PCB pad would be better than Cu surface finish. The results of this investigation would be valuable not only to microelectronics packaging and to design engineers but also to those involved in the development of new miniaturised electronics product with improved reliability.

Chapter 8: Long-Term Reliability of Flexible BGA Solder Joints under Accelerated Thermal Cycling Conditions

8.1 Introduction

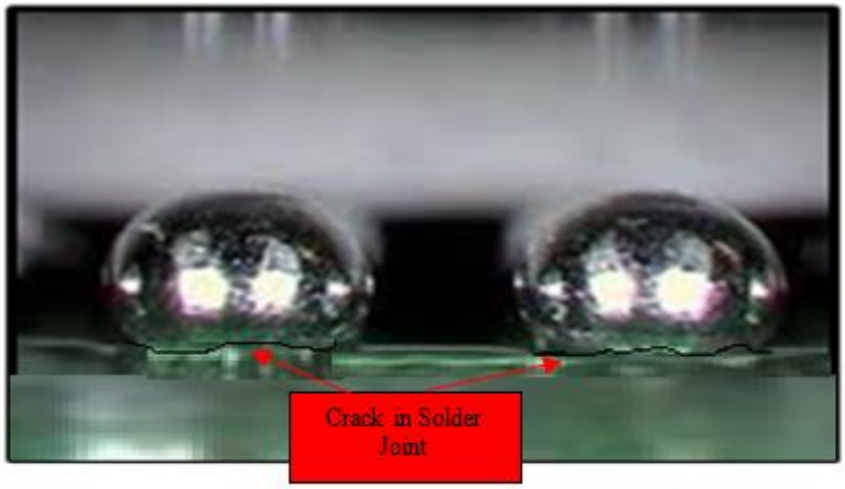
As mentioned before in this thesis, BGAs are high-performance electronics miniature packages, mounted on a substrate at its bottom surface using solder balls. The tiny Solder Joints (SJs) at the floor part of BGA help not only to provide electrical and mechanical connections but also to diffuse heat away from the chip. With further reductions in the size of SJs, the reliability of the joints has become more and more critical to the long-term achievement of electronic products. Therefore, the need to investigate the reliability of flexible BGA solder joints using accelerated thermal cycling is crucial to the electronics industry.

The aim of the research is to measure the safety of flexible BGA SJs using accelerated thermal cycling. Some objectives were used to achieved the aim this study. The objectives include, a) Designing accelerated thermal cycle tests using identified field operating conditions (mainly the temperatures); and the expected product lifetime for BGA SJs employed in microelectronic applications, b) Calculation of AF and test times using preferred thermal cycle test standard(s), c) Evaluating the shear strength of solder joints for different surface mount components; at various stages of thermal cycling, and d) Analysing the failure mechanisms and root causes of any failures observed from the accelerated thermal tests. A good understanding of thermal management in BGA solder joints will help in the achievement of a reliable flexible solder joint and its critical assessment following accelerated thermal cycling condition.

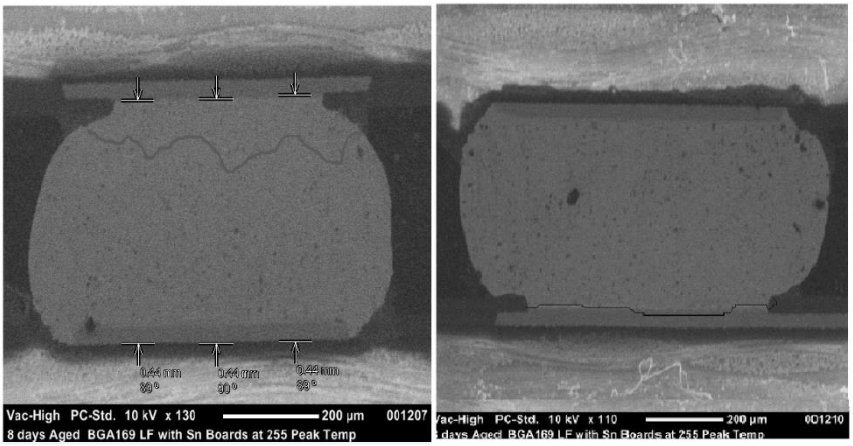
8.2 Thermal Management Issues in BGA Solder Joints

BGA packages are widely accepted for the use of devices in electronic design (Bhatia et al., 2010). It is a type of SMT used for packaging integrated circuits; they are made up of layers, which comprise of flip-flops or other circuits. In the manufacture of electronic circuits, BGA has offered numerous advantages, and as a result of this is used commonly among electronic manufacturers such as Intel Corp, IBM Corp, Hewlett-Packard Co or Nokia. At the process of providing a very high interconnecting density, they depend on BGA solder balls which are subjected to oxidation, eventual failure and cracking (Bhatia et al., 2010). BGAs are well known for their remarkably effective density and their high lead counts. The images of cracks in the joints of BGA solder balls and cross section are illustrated in Figure 8.1 as shown.

At high homologous temperature cycling conditions and other higher critical safety environments, the reliability of BGAs SJs is a great concern for both manufacturers and users alike. An assembled solder joint operating in high-temperature ambient is in isolation neither reliable nor unreliable. (Mallik and Kaiser, 2014). It matches so only in the context of the electronic components connected via the solder joints to some substrate that helps to form the mechanical bond (Engelmaier, Ragland and Charette, 2000).



(a) Source: (Dariavach et al., 2010)



(b) Source: (Author)

Figure 8.1: Images of (a) BGA balls cracks, (b) Cross-section of BGA solder joint crack

In electronic manufacturing, the determination of a more robust and reliable BGA solder joint is characteristic of the process variables, the use conditions, design life and acceptable failure probability of the BGA solder joints. A good BGA solder joint is a prerequisite to ensuring the

reliability in electronic manufacturing (Engelmaier, Ragland and Charette, 2000; Reiff and Bradley, 2005). Also, in electronic manufacturing, industries have characterised the interconnect reliability of CSP assemblies and that of the Commercial-Off-The-Shelf (COTS) ball grid array in accelerated thermal cycling test methods. However, the most universally used for the characterisation of devices as well as interconnections among the many environmental accelerated testing methodologies for evaluating the reliability of electronic systems is Thermal cycling (Ghaffarian, 2000).

In SJs, however, the deformation mechanisms of their adhesion strengths are majorly influenced by accelerated test parameters such as extreme temperatures, dwell times and temperature ramps. For the purpose of solder qualification and life prediction of electronic packages, Accelerated Thermal Cycles (ATC) test has been developed. ATC profiles mimics field use conditions of a BGA solder joint (Tunga et al., 2004), and serves as one of the common techniques used to evaluate the board level reliability of BGA solder joints. Testing specifications such as ramp rate, temperature range and soak time are technical and industrial standards (e.g. JEDEC's JESD22-A104-B) for temperature cycling. However, the temperature profile usually used are considered; these consists of four repeating linear segments which are the ramp-up, ramp-down, high-temperature dwell, and low-temperature dwell (Lau and SW Ricky Lee, 2004). ATC condition also governs these parameters, an essential tool which aids in the evaluation of solder joint reliability (Yang et al., 2012, 2010).

One of the common issues affecting SJs thermal cycling is thermal management enhanced through the interconnection of circuitry solder joints to supply current flow and increase power densities, which generate heat in the minuscule components. The majority of these (electronic) failures (65%) resulted from the thermomechanical state of the joints (Macdiarmid and Solutions, 2011); hence, a critical research is required to assess the accelerated thermal failures. Solder joint fatigue is one of the distinct failure modes that results from thermal cycling. An induced cycling temperature changes in the PCB can lead to fatigue failure. This failure starts with a formation of a crack, usually by the edge of the solder joint; this extends through the solder joint, and it eventually reduces the circuit performance and induces mechanical failure of the solder joint (Macdiarmid and Solutions, 2011). The problem of solder joint cracking in printed circuit boards has been an augmented interest directed towards the effect of high-frequency thermal cycling (Bangs and Beal, 1975). Thus, a device operation, especially at high

homologous temperatures is assured and manageable, if the life expectancy of the BGA on the flexible circuit board in use can be thermally determined.

8.3 Test Time Prediction

The actual test time prediction of the BGA SJs, in general, are determined by subjecting their test vehicles assembled on the PCBs to temperature cycling in relation with their acknowledged survival lifetime in the field. In the determination of an adequately predicted test time, the chamber temperature has to be optimised through several test trials to match with the product temperature to avoid component infertility or subsequent damage. Hence, an Acceleration Factor (AF) would be needed; thus, to calculate the AF, an equation must be used which is called the Coffin-Manson Equation. It is pertinent to note that most researchers (Amalu and N.N. Ekere, 2012; Arra et al., 2002; Borgesen et al., 2007) employed finite element based approach to the prediction of solder joint fatigue life. It does not only require a proper knowledge of finite element analysis technique and mechanics of materials but involves solder/stress damage parameters, Ψ whose dependence is hugely on mere numerical modelling and material property assumptions; which include plasticity, creep, temperature dependence, plane stress, 2D and 3D mesh characteristics. However, in this study solder joint damage mechanism and lifetime reliability prediction are achieved using laboratory-based ATC and analytical-based AF described earlier.

8.3.1 Coffin-Manson Equation

In electronic packaging, during the design for reliability, lifetime prediction is essential; hence, the Coffin-Manson's Equation (CME) is a major analytical tool used in establishing the practical evaluation of a thermal fatigue life of BGA solder joint (Webster, Pan and Toleno, 2007). Presented in Eq. (8.1) is the Coffin-Manson's equation described in the literature review for AF calculation (Vasudevan and Fan, 2008).

$$\mathbf{AF} = \frac{N_{field}}{N_{test}} = \left(\frac{F_{\mathbf{field}}}{F_{\mathbf{test}}}\right)^{-m} \cdot \left(\frac{\Delta T_{\mathbf{field}}}{\Delta T_{\mathbf{test}}}\right)^{-n} \cdot \left[e^{\frac{Ea}{K}\left(\frac{1}{T_{max,field}} - \frac{1}{T_{max,test}}\right)}\right] \tag{8.1}$$

, where,

AF = Acceleration Factor
F_{field} = Cycle Frequency in the field (cycles/24 hours)
F_{test} = Cycle Frequency in the Laboratory
ΔT_{field} = Temperature difference in the field
ΔT_{test} = Temperature difference in the Laboratory
$T_{max\ field}$ = Field temperature maximum
$T_{max.test}$ = Laboratory temperature maximum
Ea = Activation energy in electron [Volts (eV)] = 2185 for SAC, 1414 for SnPb
k = Boltzmann constant ($k = 8.617.10^{-5}$ eV/K)
e = 2.71828 (base of the natural logarithms)
m = Fatigue or Coffin-Manson's exponent (F_{field} cycles/24 hours (8/24) = 1/3)
n = Material constant (ΔT_{field} /24 hours) i.e. 85-20 /24 = 2.7

Further to Eq. (8.1), the AF however, is directly proportional to the Number of field temperature cycles and inversely proportional to the number of test temperatures. Thus, the Acceleration Factor (Lee, 2006) is further simplified in equation 8.2 and interpreted as:

$$AF = \frac{Time-to-\ failure\ at\ use\ condition}{Time-to-\ failure\ at\ test\ condition}, \quad \text{which implies:}$$

$$AF = \frac{N_{field}}{N_{test}} \tag{8.1}$$

, where:

N_{field} = Number of field temperature cycles
N_{test} = Number of test temperature cycles

Hence, to calculate the number of test temperature cycles, the Acceleration Factor as shown in Eq.8 3 for the number of test temperature cycles would divide the Number of field temperature cycles.

$$N_{test} = \frac{N_{field}}{AF} \tag{8.2}$$

8.3.2 Field Conditions

The 'field temperature' condition as used in microelectronics assembly and hence in this study was achieved using elevated temperatures as a corollary to the ground temperature. Thus, the harsh condition was used to depict or reflect the field temperatures. The field condition used is typical of microelectronics used in personal computers or laptops, where average temperature

ambient is 20^0 C. In summary, the tabulated field temperatures utilised in this investigation is in Table 8.1.

Table 8.1: Field condition employed in this research study

Low Temperature	High Temperature	Cycle / Hour
20^0C	85^0C	1

8.3.3 Predicted Test Time Calculation

The reliability of the BGA solder joint has an estimated time-frame determination for 25 years; however, to calculate the predicted test time, the acceleration factor is calculated with Equation 8.2. Hence, the required parameters to calculate the AF are shown in Table 8.2 respectively. The role of the AF is vital in life cycle/time predicting of a solder joint within few days of ATC/HATC condition. The TC, ATC, and AF equation are dependent upon the design parameters conceived of for the expected life cycle of the product. Such as substrate thermal conductivity, substrate thickness, CTE mismatch between the substrate and PCB, PCB thickness and environmental parameter including temperature range (ΔT), frequency of cycles (f), and peak/junction temperature (T_j) (Perkins and Sitaraman, 2008).

Table 8.2: Parameters used to calculate the AF

Parameters	**Value**
M	0.136
N	2.65
Ea/k	2185
F_{field}	8 Cycles / 24 hour
F_{test}	31 Cycles / 24 hour
ΔT_{field}	65K
ΔT_{test}	190K
$T_{max.\ field}$	358K
$T_{max.\ field}$	423K

In consequence, the Acceleration Factor obtained using the stated Coffin-Manson's equation is AF = 33.93, just for a 2-year duration in the application. However, the cycling period when extrapolated to say, 25 year life cycle duration, the acceleration factor necessary for this time frame would be 424.125. Before the AF calculation, however, the 'cycles' in the field were first calculated with Equation (8.3) as presented.

$$N_{field} = T_{field} \bullet F_{field} \tag{8.3}$$

, where:
N_{field} = Number of field temperature cycles
F_{field} = Cycle frequency in the field
T_{field} = Time in the field

However, the predicted test time for the field temperature cycle can be calculated using the Equation 8.4.

$$T_{test} = \frac{N_{test}}{T_{cycle}} \tag{8.4}$$

, where:

T_{test} = Time for test
N_{test} = Number of test temperature cycles
T_{cycle} = Time for a cycle

Table 8.3 gives the summary of all the results obtained from the calculations made. The reflow sample was examined, without going through all the vast process of the thermal cycling regime.

Table 8.3: Predicted test time

T_{field} (Years)	N_{field}	N_{test}	T_{test} (Hours)	T_{test} (Days)
0	0000	00.00	0.133	00.00
0.5	1460	57.97	32.93	1.40
1	2920	115.94	65.86	3.00
1.5	4380	173.91	98.79	4.12
2	5840	231.88	131.72	5.49
4.5	13140	521.73	296.37	12.35
8	23360	927.52	526.88	21.95
16.5	48180	1913.01	1086.69	45.28
25	73000	2898.5	1646.5	68.60

8.3.4 Thermal Cycling

In electronic assemblies, SJs continually evolve when exposed to isothermal ageing and thermal cycling environments as a result of the mechanical response, the failure behaviour and the microstructure of the BGA solder joints (Dusek, Wickham and Hunt, 2005). Some constraints on the thermal performance of a BGA package depends on including the utilisation of thermal balls, die size, the range of perimeter balls, and therefore the flexible printed circuit boards. However, the integrity of thermal methods in and around the BGA will be laid flat with thermal cycling as a result of the cracking of solder balls and delamination of the packages (Montgomery, 2012). However, it is an essential investigation and a most traditional method, used in evaluating the reliability of BGAs SJs interconnects technology.

8.3.4.1 Thermal Cycling Parameters Used

The recommended temperature cycles are $+25^0$C to $+100^0$C or 0^0C to $+100^0$C° C, so as to subject the BGA solder joints to an extended accelerated temperature/ageing with the aim of producing creep/fatigue damage to the BGA solder joints. The avoidance of thermal shock would require that the rate of change in temperature should be proficient and less than 20^0C/min (IPC, 1992) cited by (Lin, 2007). The period for one cycle result from the chosen thermal cycling parameters is shown in Chapter 3, Table 3.2, while Figure 3.14 of the same chapter shows an abstract of the thermal cycle profile used to achieve one of the objectives to this study. The experimentation process for making the required solder joint is in Chapter 3, Figure 3.16 as presented; and the images shown in Chapter 3, Figure 3.30 represent samples in the chamber ready for thermal cycling test.

8.3.4.2 Temperature Profile for Thermal Cycling

The determination of the 'Temperature Profile' for the ATC requires a careful selection of the normal and expected field temperatures condition. Figure 8.2 and Table 8.4 show a standard representative temperature profile and descriptions of the thermic cycle test conditions.

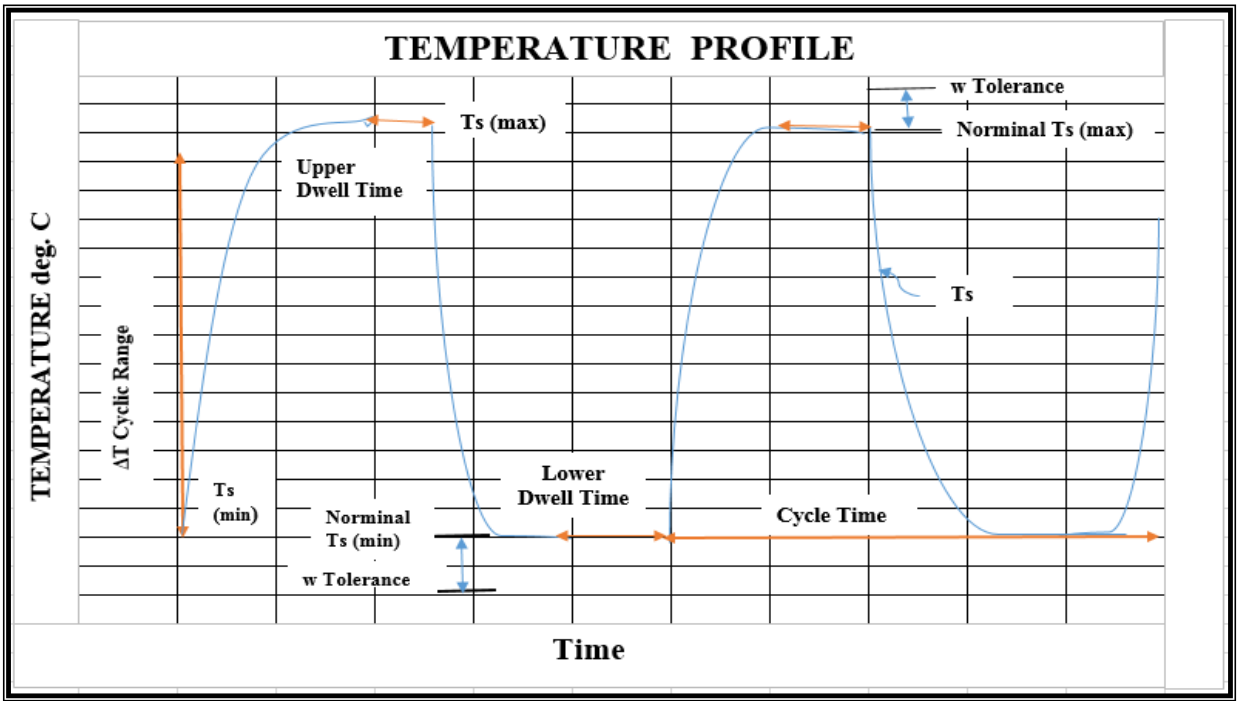


Figure 8.2: Standard temperature profile for thermal cycle test conditions

Source: (Pan et al., 2006)

These standards for the ATC 'Temperature Profile' are in consistency with the IPC-9701 standard for performance test methods and qualification requirements for surface mount solder attachments (IPC, 2002). The range of temperatures in use may vary from minimum to maximum based on device ambient temperature of operation and application context. To avoid equipment failure, the threshold temperature of a device should not be exceeded. The normal or standard operating temperature (De Gloria, 2014; Thaduri et al., 2013) for commercial, industrial, automotive and military devices/applications are outlined thus,

- Commercial: 0 ^{0}C to 85 ^{0}C
- Industrial: -40 ^{0}C to 100 ^{0}C
- Automotive: -40 ^{0}C to 125 ^{0}C
- Military: -55 ^{0}C to 125 ^{0}C
- Aerospace & Oil Well Logging: -55 ^{0}C to 175 ^{0}C

Table 8.4: Standard temperature profile parameters and descriptions

Profile Parameters	**Description**
Temperature Cycle Range	It is the maximum and minimum difference between temperatures sustained during temperature cycle test.
Temperature Sample (Ts)	The sample temperature during the temperature cycle.
Max Temperature Sample Ts (max)	It is the maximum measured temperature of samples.
Nominal Max Temperature T (max)	It is the nominal maximum temperature for a test condition required for Ts (max) samples.
Min Temperature Sample Ts (min)	It is the minimum measured temperature of samples.
Nominal Min Temperature T (min)	It is the nominal minimum temperature for a test condition required for Ts (min) samples.
Nominal ΔT	The difference between nominal T(max) and nominal T(min).
Dwell Time	It is an identified time range of the sample temperature between the T(max) and T(min).
Dwell Temperature	It is the upper T(max) above and the T (min) below the temperature at the end of each cycle.
Cycle Time	It is the total time for a complete temperature cycle.
Temperature Ramp Rate	It is temperature increase/decrease per unit time of the samples.

However, the operating temperature in the case of electrical devices may be the junction temperature (T_J) of the semiconductor (solder joint) device. In principle, the T_J is usually affected by the ambient temperature and power dissipation, expressed for any given solder joint integrated circuit or PWB using Eq.8.6 (Previti, Holtzer and Hunsinger, 2011).

$$T_J = T_a + P_D \; x \; R_{ja} \tag{8.6}$$

Where, T_J is the junction temperature in ^{0}C, Ta the ambient temperature also in ^{0}C, P_D the power dissipation in watt (W), and R_{ja} is the junction to ambient thermal resistance in ^{0}C/W.

8.4 Accelerated Thermal Cycling Test

The thermal cycling test was accomplished using the ESPEC'S-ARS-0680 environmental chamber presented in Chapter 3, Figure 3.30, which has a periodic change from cold to hot. The thermal cycling profile (shown in Figure 8.3) has an LCD digital minicomputer board as the programmable control unit that captures the programmed parameters in the chamber. Since the 'Chamber' design is Humidity and Temperature resistive, the author ignored the humidity, as it was not an objective to this research work. The temperature programme was in Celsius, and the accelerated thermal time converted from hours to minutes, as shown in Table 8.4.

Figure 8.3: Minicomputer image of a digital LCD board used to program the ATC

Table 8.5: The converted hours to minutes of the accelerated thermal time

T_{field} (Years)	T_{test} (Hours)	T_{test} (Minutes)
0.5	33	1975.8
1	66	3952.8
1.5	99	5940.0
2	132	7920.0
4.5	297	17820.0
8	528	31680.0
16.5	1089	65340.0
25	1650	99000.0

8.4.1 Thermal Cycling Procedure

The achieved accelerated thermal test was possible because of the underlying processes and operational steps given in bullet points. The control unit was first programmed to start from the room temperature of 20^0C before the cycle starts to operate from 0^oC to 150^oC respectively; for a total number of 76 cycles in 132 hours as shown in Table 8.6. The given process was concluded just a few seconds before the sudden broke down of the chamber.

- Step 1- The chamber oven for the temperature cycling was first switched on, and the ATC test piece was set up using the programme designated parameters to proceed.
- Step 2- The setup program was saved after being tested.
- Step 3- Four test samples were then put into the chamber and at the end of each cycle, the oven switches off automatically.
- Step 4- The first test sample was taken out after 19 cycles in 33 hours, leaving the remaining four samples to complete the number of cycles programmed.
- Step 5- At the end of 38 cycles in 66 hours, the chamber stopped automatically again and the second sample was taken out.
- Step 6- The third test sample was taken out at the end of 57 cycles in 99 hours, after the automatic stopping of the chamber.
- Step 7- The last test sample was taken out at the end of the programme for 76 cycles at 132 hours, which was the final period for the accelerated thermal cycling test before system breakdown.

Table 8.6: Number of hours of cycles for the accelerated thermal cycling test

T_{field} (Years)	T_{test} (Hours)	Cycle
0.5	33	19
1	66	38
1.5	99	57
2	132	76
4.5	297	171
8	528	304
16.5	1089	627
25	1650	950

The samples were removed from the chamber after thermal cycle completion and were kept at a room temperature of 20^{o}C, waiting for the next test (shear test) to be carried out.

8.4.2 Shear Test

The 'Shear Test' was performed, shortly, after the end of the accelerated thermal cycling. The shear test execution was with the aid of the modular multifunction 'Dage Bond Tester, Series-4000', which was used to determine the mechanical strength (shear strength (τ)) of the BGA balls on an FCB. A total number of ten (10) BGA solder joints were destructively sheared-tested on the designed FCB test vehicle, which had a total number of twenty (20) BGA solder joints. Each of the thermally accelerated samples, including the reflow sample, were firmly glued to the test board with the aid of a blob of glue, so as to give good and accurate result while shearing the SJs off their base metals.

The shear process was begun by first placing the BGA solder joints on the bench vice (see Figure 8.5). All sheared samples were under the same test conditions, including the reflowed samples. However, the cross-sectional area of the BGA solder joint was a difficult task to determine because of the miniature size of the BGA solder joint component. This development has a corresponding adverse effect on the graphical analysis of the joints' shear strengths. Ten randomly chosen BGA solder joints were shared to obtain the average interfacial strength. Thus, the data obtained in this test was further enhanced arithmetically and evaluated using the most basic shear force values required for the BGA solder joint to rupture. The shear area was 0.002879m^{2}. Tables 8.7 to 8.11present the values for each of the average shear forces and shear strengths for as-reflowed and aged samples. Important settings for the process of the shear test were set up, using a software tool. Figure 8.4 shows the settings used to achieve the shear force experimental data.

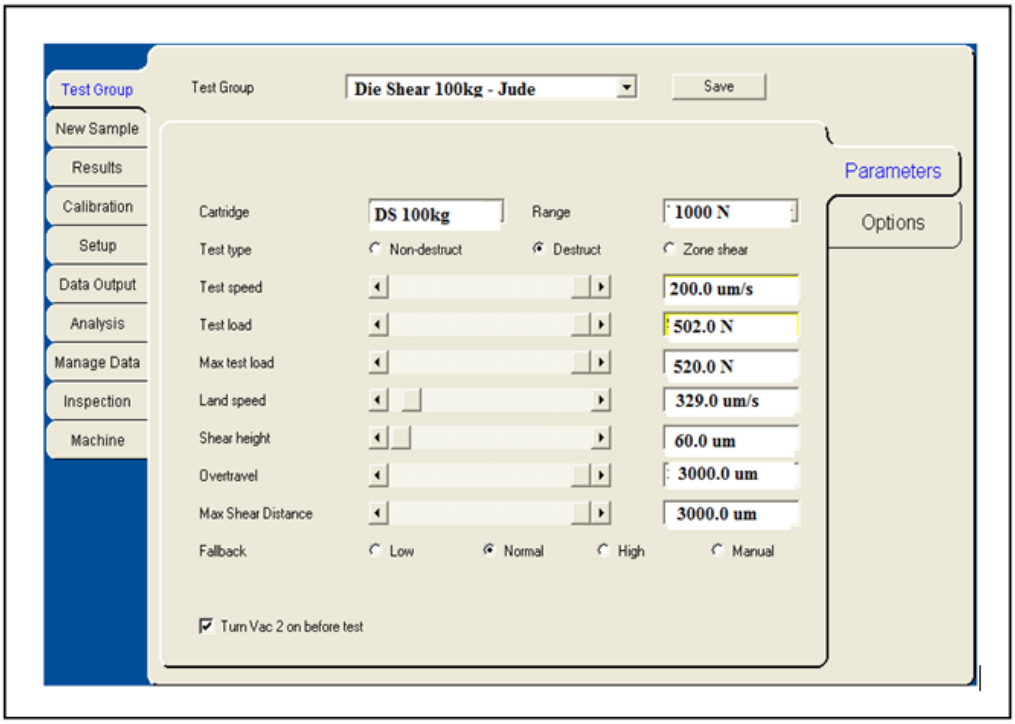


Figure 8.4: Profile settings used in achieving the laboratory shear test data

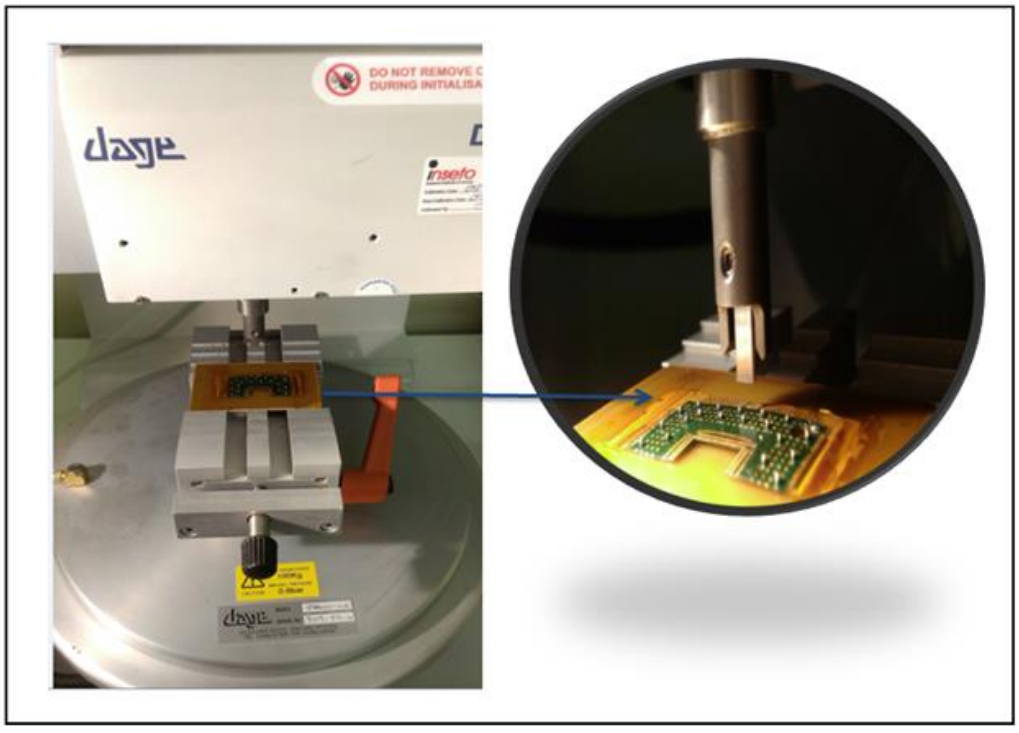


Figure 8.5: The test sample placed on the bench vice ready for shearing

8.4.3 The SEM Images of the FCB BGA Solder Joints

The JCM-5000 Neoscope Scanning Electron Microscope (SEM) machine was used to scan and record the digital images of the sample; it was used to examine for cracks in the BGA solder joint due to thermal fatigue. The FCB was once again divided into two equal parts, to minimise its size to fit the scanning vice. Next was to place the sample on the small vacuum area of the SEM, which is an airtight area for the scanning. Figure 8:6 to Figure 8:10 show the examined focused images of the BGA solder joint. Each of the joint pictures as shown below has the top view of the BGA solder joint tilted backwards and scanned at an angle of 81^{o}.

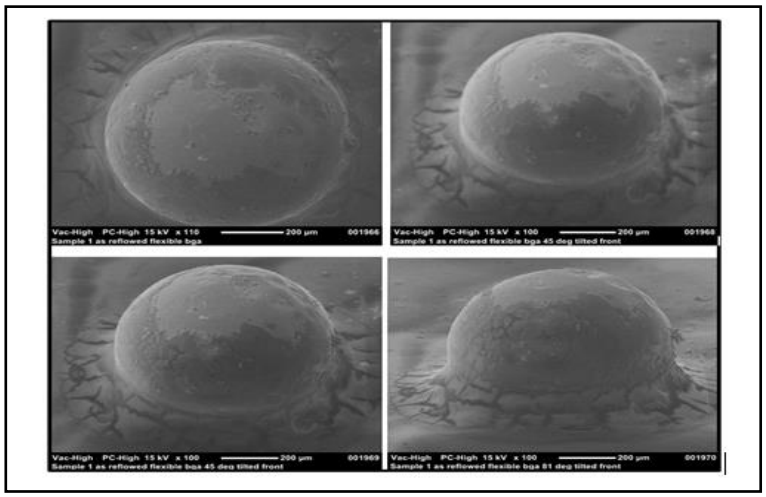


Figure 8.6: SEM images of the BGA solder joint test of the reflowed sample

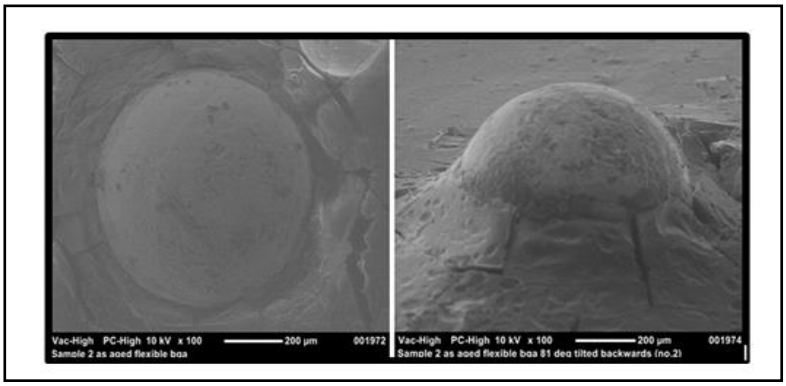


Figure 8.7: SEM images of the BGA solder joints test of the 33hours of ATC

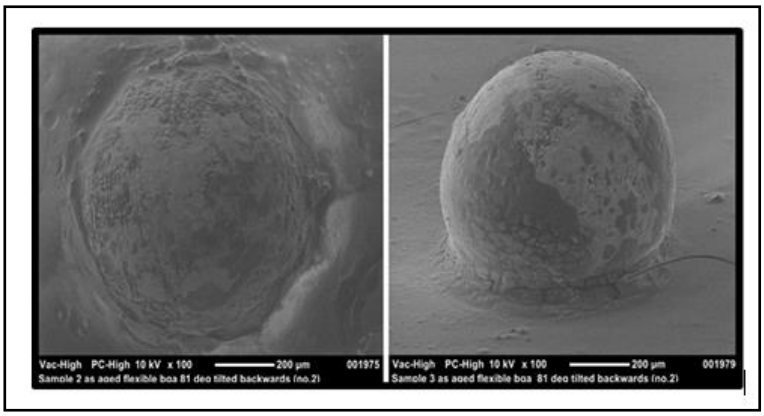


Figure 8.8: SEM images of the BGA solder joints test of the 66 hours of ATC.

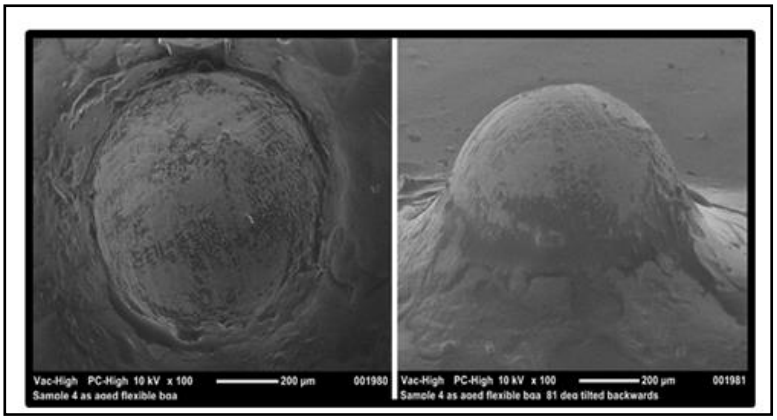


Figure 8.9: SEM images of the BGA solder joints test of the 99 hours of ATC.

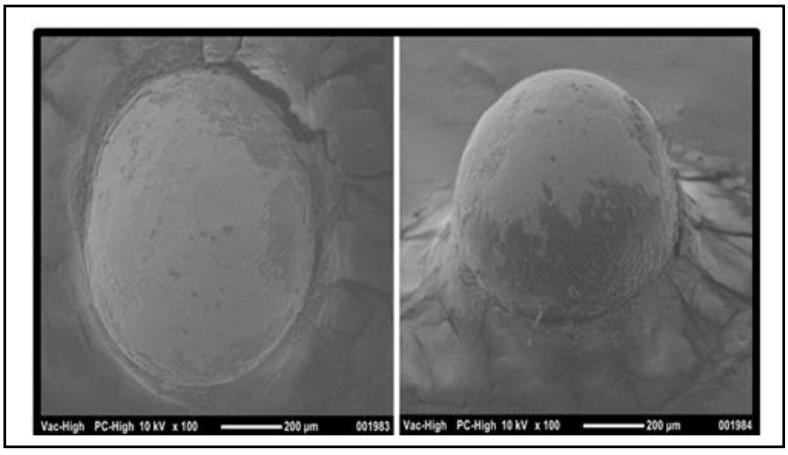


Figure 8.10: SEM images of BGA solder joints test for the 132 hours of ATC.

8.5 Results and Discussions

The results of this study are presented in two parts: the shear strength of the BGA solder joints, and the SEM surface fracture result of the solder joints.

8.5.1 Study on BGA Solder Balls Shear Strength

Table 8.7 to Table 8.11 present the measured shear force and strength values of the solder joint shear tests performed after different accelerated thermal ageing conditions. The shear strength (τ) values were calculated directly by first determining the surface area (A) of the solder ball's joint. The solder ball used in this study is lead-free, circular in shape, 0.76 mm in diameter and has alloy composition of Sn-4.0Ag-0.5Cu (SAC405). The method involves dividing the shear force (F) values with the shear area of the solder ball, using the expression illustrated in Equation 8.7.

$$\text{Average shear strength } (\tau) = \frac{Averarge\ Shear\ Force\ (N)}{Shear\ Area\ (M^2)} \quad (8.7)$$

$$\text{Cross-sectional area of solder joint, } (A) = \frac{\pi D^2}{4}\ (m^2) \quad (8.8)$$

From equation (8.8), the solder ball diameter, D is 0.76mm = 0.00076m. The cross-sectional area (A) is given by:

$$A = \frac{3.142\ x\ 0.00076^2}{4} = \frac{3.142\ x\ 5.776x10^{-7}}{4} = \frac{1.8148192\ x\ 10^{-6}}{4} = 4.537048 \text{ x } 10^{-7}\ m^2$$

Hence, the shear area (A) of the BGA solder ball on the flexible substrate is 4.537048 x 10^{-7} m^2, and this information is very useful in calculating the solder shear strength.

Figure 8.11 shows the graph of the shear strength variation on the number of shear test performed for all experimental runs.

Table 8.7: Average shear strength results for reflow soldering

Average Shear Strength Results for As-Reflowed			
S/N	Shear Force (N)		Shear Strength (MPa)
1	14.34		31.61
2	13.62		30.02
3	14.34		31.61
4	12.80		28.21
5	11.14		24.55
6	12.86		28.34
7	12.53		27.62
8	13.57		29.91
9	10.73		23.65
10	13.18		29.05
Average Shear Force (N)	12.911	Average Shear strength (MPa)	28.46

Table 8.8: Average shear strength results for 33 hours ageing

33 Hours Average Shear Strength Results			
S/N	Shear Force (N)		Shear Strength (MPa)
1	11.99		26.43
2	13.34		29.40
3	11.60		25.57
4	13.16		29.01
5	10.16		22.39
6	13.89		30.62
7	15.71		34.63
8	14.13		31.14
9	15.91		35.07
10	12.12		26.71
Average Shear Force (N)	13.201	Average Shear strength (MPa)	29.09

Table 8.9: Average shear strength results for 66 hours ageing

66 Hours Average Shear Strength Results

S/N	Shear Force (N))	Shear Strength (MPa)
1	13.36	29.45
2	13.28	29.27
3	12.39	27.31
4	9.64	21.25
5	12.32	27.15
6	12.16	26.80
7	10.84	23.89
8	13.27	29.25
9	12.53	27.62
10	12.49	27.53
Average Shear Force	12.228	Average Shear strength (MPa) 26.95

Table 8.10: Average shear strength results for 99 hours ageing

99 Hours Average Shear Strength Results

S/N	Shear Force (N)	Shear Strength (MPa)
1	10.57	23.30
2	10.79	23.78
3	12.90	28.43
4	10.05	22.15
5	11.89	26.21
6	13.66	30.11
7	13.87	30.57
8	12.89	28.41
9	11.71	25.81
10	11.33	24.97
Average Shear Force (N)	11.966	Average Shear strength (MPa) 26.37

Table 8.11: Average shear strength results for 132 hours ageing

132 Hours Average Shear Strength Results			
S/N	Shear Force (N)		Shear Strength (MPa)
1	12.92		28.48
2	13.10		28.87
3	10.06		22.17
4	12.61		27.79
5	14.10		31.08
6	11.12		24.51
7	10.57		23.30
8	11.84		26.10
9	13.41		29.56
10	13.12		28.92
Average Shear Force (N)	12.285	Average Shear strength (MPa)	27.08

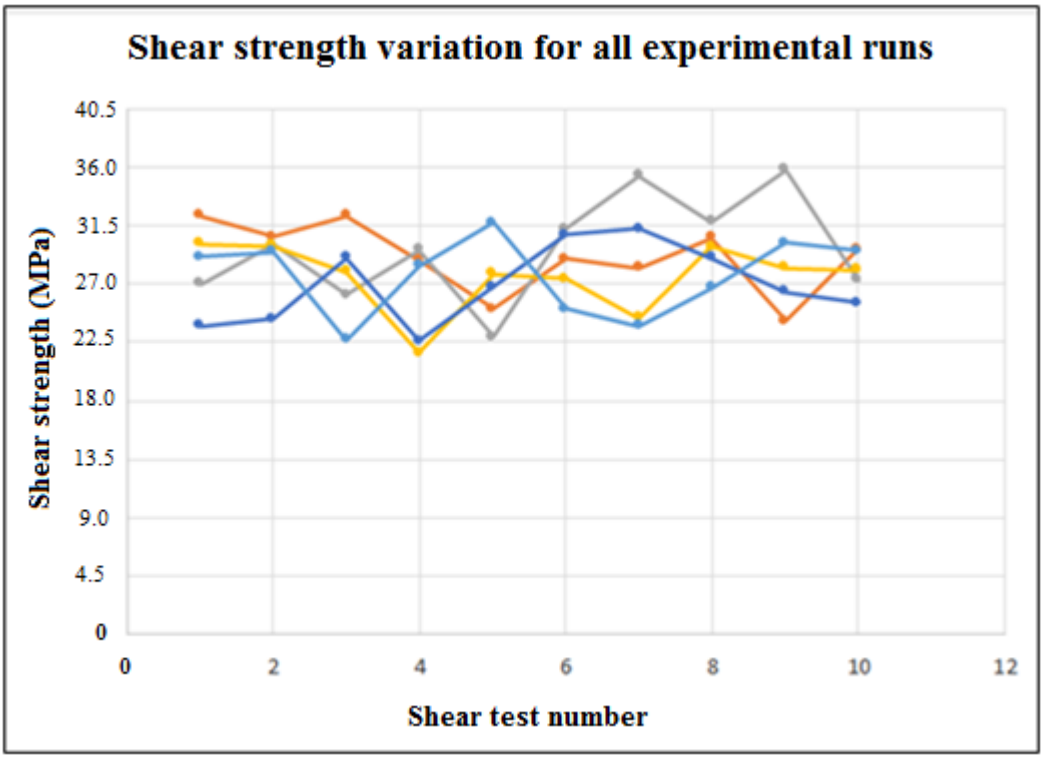


Figure 8.11: Pooled graph of shear strengths against shear test number

The plot in Fig 8.11 demonstrates that the shear strength of the solder joints increases as the ageing time increases. Some factors cause the rise in shear strength. Ageing causes accelerated

formation and growth of intermetallic compound (IMC), which is known to decrease the ductility and increase force and stiffness of solder joints. The IMC forms at the boundary of the interconnecting bodies which is the favourable site for rupture under load. The formation of the IMC signifies having a joint with an excellent bonding at the interface. Also, ageing causes a microstructural change of the solder joint materials which becomes very significant and critical at high temperature and long duration. The materials at the extended hostile condition would be made more coarse, and the bonding might become strain hardened, which will increase the mechanical stiffness at the expense of the ductility.

From the preceding discussions, however, the average shear strength calculation was carried out from the table of shear force/strength results. Thus for the basic form of a general shear stress expressed in Equation 8.7, the average shear strength is the proportion of the average shear force in Newton to the shear area in metre square. The above expression is further represented in Equation 8.8 as:

$$\tau = \frac{F}{A_C} \tag{8.8}$$

, where:

τ = The shear strength (N/m^2);
F = The force applied (N); and
A_C = Cross-sectional area (m^2) of material, with area perpendicular to the applied force vector

Considering the Eq. (8.8) however, the maximum shear strength created in a solid round bar (such as in solder joint) subject to impact shear is given in Equation 8.9:

$$\tau_i = 2\left(\frac{U_{ke}G}{V_{sb}}\right)^{\frac{1}{2}} \tag{8.9}$$

, where
$i = 1-5$, (for the solder joint studied).
U_{ke} = change in kinetic energy;
G = shear modulus;
Vs_b = volume of solder bump [LxWxH], L = CSH mm^2; and
$U_{ke} = U_{rotating} + U_{applied;}$
$U_{rotating} = \frac{1}{2} I \omega^2;$
$U_{applied;} = T\theta_{displaced;}$
I = mass moment of inertia;
ω = angular speed
T = torques (N.m)

Apart from determining the maximum solder joints' strength, it is thus imperative to ascertain the capabilities of their metallised bond. However, and more specifically the strength of their adhesion to the plastic itself or the substrate interface after long thermal cycling ageing of 132 hours at a high-temperature ambient of 150^0C. The novel approach in this regard is a characterisation method. The method seeks to measure the qualitative aspect of the joint by merely detecting the presence of solder paste surface fracture. After the shear test, its interfacial intermetallic thickness measurement followed.

The shear strengths were further calculated using Equation (8.9) by quantifying the binding force of the surface tensions. However, the Equation (8.10) is an alleyway to determining the degree of shear stress exposure; the solder joints studied underwent in the experimental shear device.

$$\begin{aligned} \tau &= \mu \frac{d_u}{d_y} \\ &= \mu \frac{2\pi Nr_r - 2\pi Nr_0}{x} \\ &= \mu \frac{2\pi Nr_r - 0}{x} \\ \tau_C &= \mu \frac{2\pi Nr_C \mu}{x} \end{aligned} \tag{8.10}$$

, where:

τ_r = Shear stress at radius r [N.m-2]

τ_c = Shear stress at critical radius [N.m-2]

μ = Viscosity of fluid [N.s.m-2]

N = Rotational speed of the shear device [s-1]

r = Distance from the centre of the disc [m]

x = Distance between the top and bottom disc [m]

Therefore, by determining the critical shear radius at which solder joints begin to detach, the critical shear stress of the joint can be determined. The ±shear strength of the solder joint in this investigation was measured on a Dage Bond automated test machine at a speed of 200µm/sec, with a shear blade tip 25µm from the metallised substrate bond surface pad which

is about a quarter of the solder bump height. The shear strength decreases with increasing cycle period.

Table 8.12: Average shear strength for as-reflowed and ATC test samples

S/No	T_{field} (Years)	T_{test} (Hours)	Cycle Period	Average Shear Strength (N/m^2)
1	AR = 0	0	0	4484.543
2	0.5	33	19	4585.273
3	1	66	38	4247.308
4	1.5	99	57	4156.304
5	2	132	76	4267.107

8.5.2 Study on BGA Solder Balls Shear Fracture Behaviour & Mean STD

The recorded readings (Table 8.12) are the shear strength results calculated from the shear force results obtained using the Dage Bond tester series-4000 as shown in Table 8.7 to Table 8.11; however, the results are statistically displayed to get knowledge of the observable behaviour of the BGA solder balls. This knowledge can be accomplished through the physics of failure based analysis and by understanding some statistical values of the result. Such as the maximum value for each test sample, the minimum value for each test sample, the range for each of the test specimens, the midpoint for each test sample, the mean for each test sample, the variance and the standard deviation from the mean for each test sample respectively. The standard mean difference score is a method adopted in analysing the shear test result whereby the variance and the standard deviations are calculated using Equations 8.11 and 8.12 in the order shown, followed by the data sheet results presented in Table 8.13 for the statistical evaluation and representation.

$$\text{Variance, } S^2 = \frac{\sum (X - \bar{X})^2}{n} \tag{8.11}$$

$$\text{Standard Deviation, } S = \sqrt{\frac{\sum (X - \bar{X})^2}{n}} \tag{8.12}$$

Table 8.13: Statistical evaluation of the shear test data (X) with variance and STD

Thermal periods	Thermal (Hour)	X Max	X Min	X Range	X Midpoint	X Mean	Variance	STD Deviation
0 (Reflow)	0.133	14.34	10.73	3.61	12.54	12.91	1.31	1.15
1.40 Days	33	15.91	10.16	5.75	13.04	13.2	2.94	1.72
2.75 Days	66	13.4	9.64	3.72	11.50	12.23	1.23	1.11
4.11 Days	99	13.87	10.57	3.82	11.96	11.97	1.57	1.25
5.50 Days	132	14.10	10.06	4.04	12.08	12.29	1.58	1.26

It was however in the interest and expectation of the author that the conducted shear strength experimental results in this research work would decrease ultimately with respect to time (Mallik and Kaiser, 2014). The reflow period of 0.133 hours led to a shear force of 12.908N. After 33 hours of thermal cycling at 0 to 150^0C, the resultant shear force was 13.201N, an increase of 29.3% growth, suspected to have come or risen from the temperature gradient.

At 66 hours of thermal cycling, the shear force was 12.228N, with a 97.3% decrease; at 99 hours, the temperature cycling at 0^oC to 150^0C had a resulting shear force of 11.966N with a 26.2% decrease. The declines suspected to arise from load affected by subjected temperatures or weaker interface strength of the BGA solder joint. Also, the 132 hours thermal cycling at 0 to 150^oC had a resulting shear force of 12.285N with an increase of 31.9%. The increased effect is possible to have resulted from the thickness of the applied solder paste (flux) used in the soldering of the BGA solder balls during the reflow soldering process.

Moreover, and due to the accelerated thermal condition of the BGA solder joints, the interconnection force between the FCB and the BGA solder balls would become weaker and fragile. Therefore, the resultant shear strength of the test sample randomly acts as observed with lower amplitude and localised resonances. As observed further, and in consequence of the ATC implication, the samples were significantly weaker than those without thermal ageing were. The failure mode was the cracking of the bond's copper-tin (Cu_3Sn) intermetallic located at the solder joint's interface. This failure mechanism starts with initiation in the bulk solder and around the corner between solder ball and pad. The cracks diffused directly into the interfacial layer of Cu_3Sn intermetallic compound and propagated across the entire interface. Also, microvoids were identified as the cause of the failure mode mentioned above and may

have been responsible for the formed Cu_3Sn IMC layer during solder metallisation, evolution and thermal cycling ageing. Similar results were found by (Munamarty et al., 1996; Engelmaier, Ragland and Charette, 2000; Tunga et al., 2004; Ghaffarian, 2000) under combined thermal cycling and vibration loading conditions employing PBGA and CSPs.

The assembled CSP test boards were thermally aged at 100-150^{0}C for up to 1,000h before drop test execution, followed by the bulk solder and the interfacial region investigation of its microstructural evolution. On the other hand, a statistical measure had to be taken, as seen in Table 8.13, for a clearer observation of the shear strength result, which is to determine the maximum and minimum value of the test samples; the range, the midpoint, the mean, and the variance respectively.

The observation showed that the heating (thermal-phase) period of one and one-sixth (1.4) days (33 hours) arose with a high variance among the BGA solder balls shear strength values. However, the reflow samples of (0.133 hours), three days (66 hours), Four and one-eighth (4.11) days (99 hours), six days (132 hours) had a small variance among the shear strength values. The obtained variance appears in the graph of Figure 8.12, with a linear regression line clearly depicted. Alternatively, the linear regression shown in Figure 8.12, can also be obtained using Equations 8.13 and 8.14.

$$r = \frac{n\sum xy - \sum x \sum y}{\sqrt{[n\sum x^2 - (\sum x)^2]}\sqrt{[n\sum y^2 - (\sum y)^2]}} \tag{8.13}$$

$$r^2 = \left(\frac{n\sum xy - \sum x \sum y}{\sqrt{[n\sum x^2 - (\sum x)^2]}\ \sqrt{[n\sum y^2 - (\sum y)^2]}}\right)^2 \tag{8.14}$$

, where

$r = r_{xy}$, the sample correlation coefficient; r^2 is a statistical measure of how close and fitted a data is to a regression line. It is called the coefficient of determination. It becomes the coefficient of multiple determination for a multiple regression if and only if n, x, and y are datasets. The set is such that $\{x_1...,x_n\}$ will contain n values; and another dataset $\{y_1,...,y_n\}$ will also contain n values. These values would represent the dependent and independent variables of the x-y component of the graph, including covariance and standard deviation.

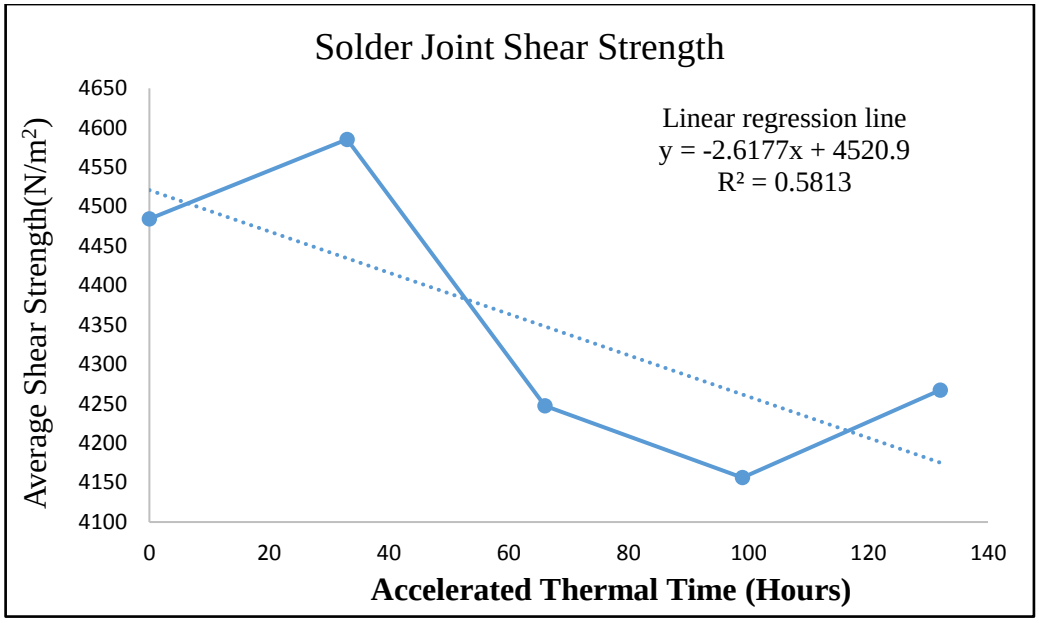


Figure 8.12: Graph of the average shear strength and the accelerated thermal time.

The correlation coefficient will differ from -1 to +1; of which, -1 indicates perfect negative correlation, and +1 indicates perfect positive correlation in close range determination (Asuero, Sayago and González, 2006; Ozer, 1985; Yachi and Loreau, 1999; Mukaka, 2012). Equation 8.11 is further illustrated using Pearson's regression lines for y as a function of x shown in Figure 8.13. The regression lines are given as y = gx(x) [red] and x = gy(y) [blue].

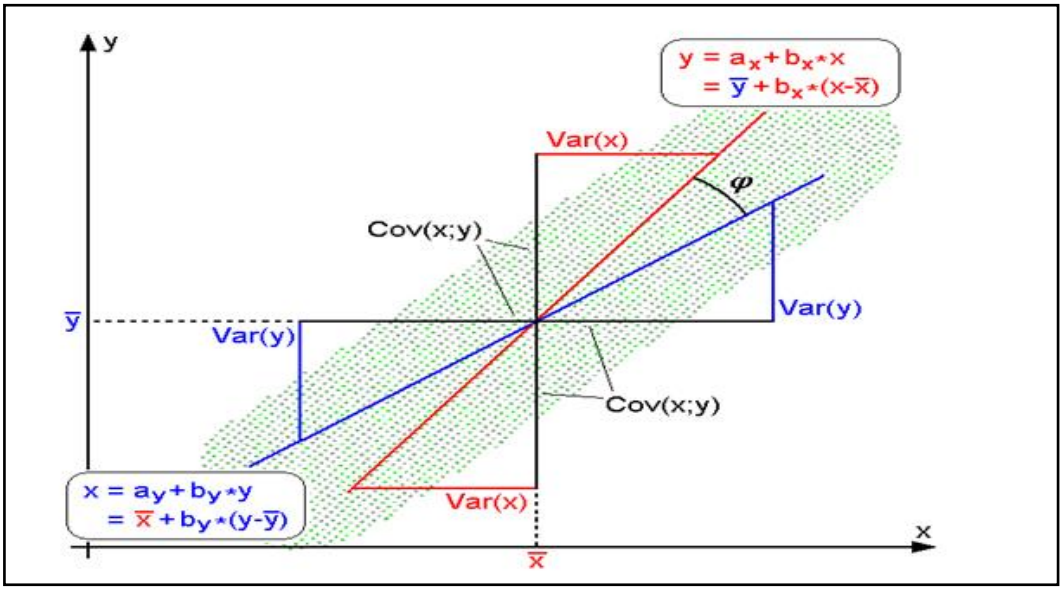


Figure 8.13: Pearson's regression lines for y as a function of x
Source: (Derek et al., 2013; Mari and Kotz, 2001).

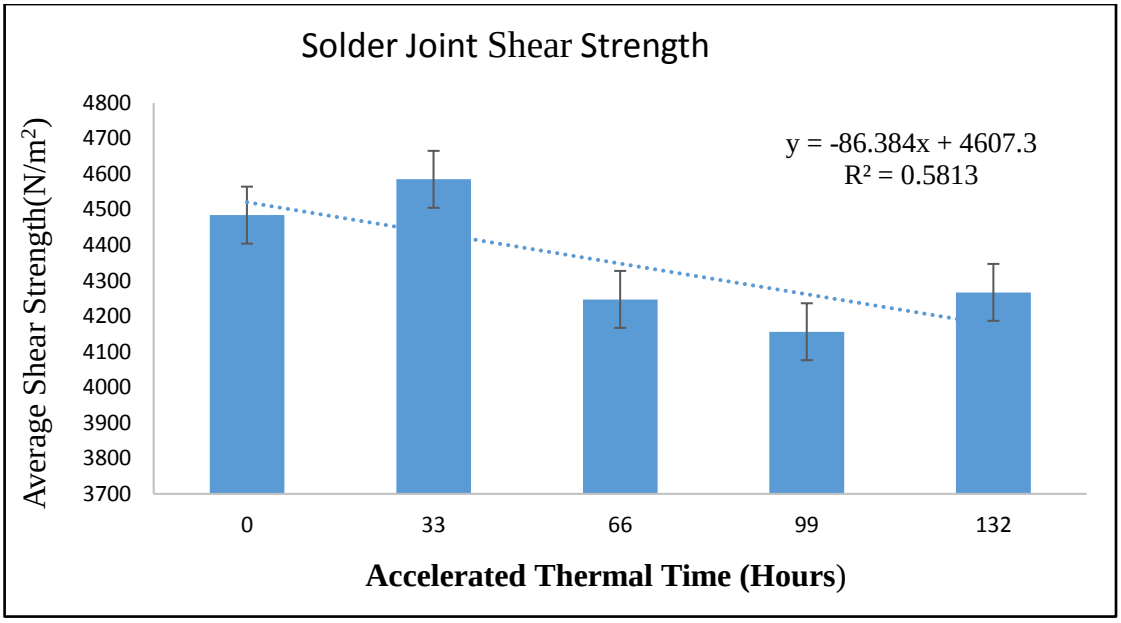


Figure 8.14: Bar charts of average shear strength and the accelerated thermal time (ATT)

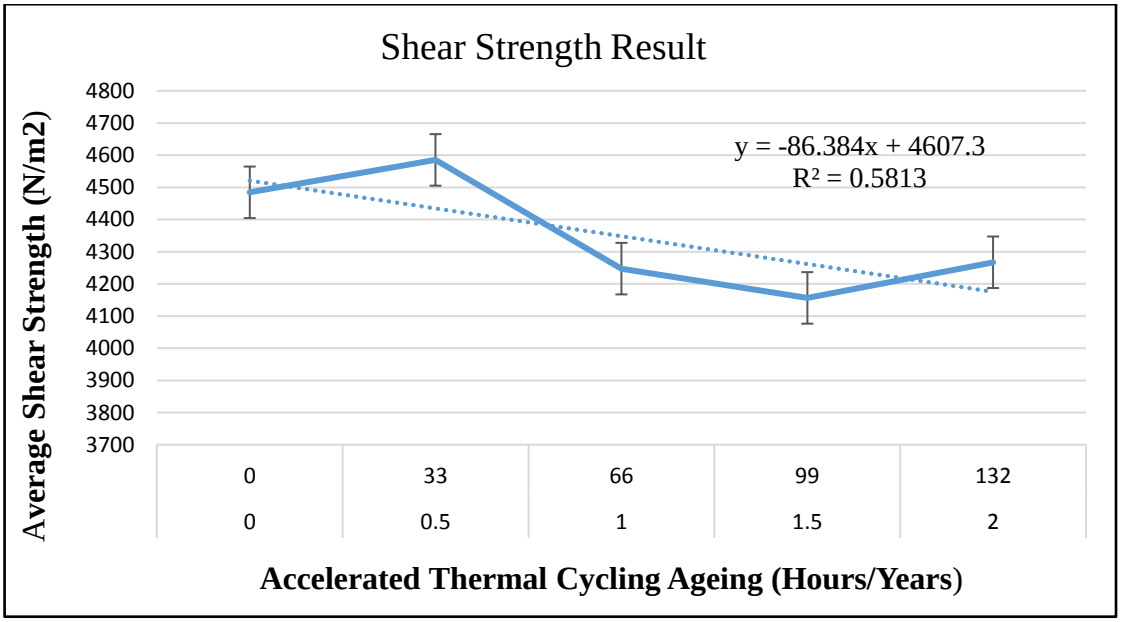


Figure 8.15: Skewed graph of average shear force and ATC –ageing time.

The graphs presented in Figure 8.12, and Figure 8.15, clearly show that the relationship between the mean shear strength and the accelerated thermal time was inversely proportional. The proportionate value falls under a linear regression graph presented in Figure 8.15 and expressed using Eq. 8.15 in the form,

$$y = a + bx \qquad (8.15)$$

, where:

Y is the dependent variable;

a, the intercept,

b, the slope of the line, and
x is the independent variable.

It is evident that the linear equation on the chart with the R-squared value of 0.9952 is very close to 1.0 showing a strong correlation. It indicates that the regression line of best fit in the given figure (Figure 8.16) is a fair estimate of the actual relationship between Concentration (x) and Absorbance (y), for the alloying compound evaluated. However, an accurate judgement and statistical prediction as to how well a regression line (Srinivasan, Pamula and Fair, 2004) represents a true relationship require information such as the number of data points collected (NC State University, 2004).

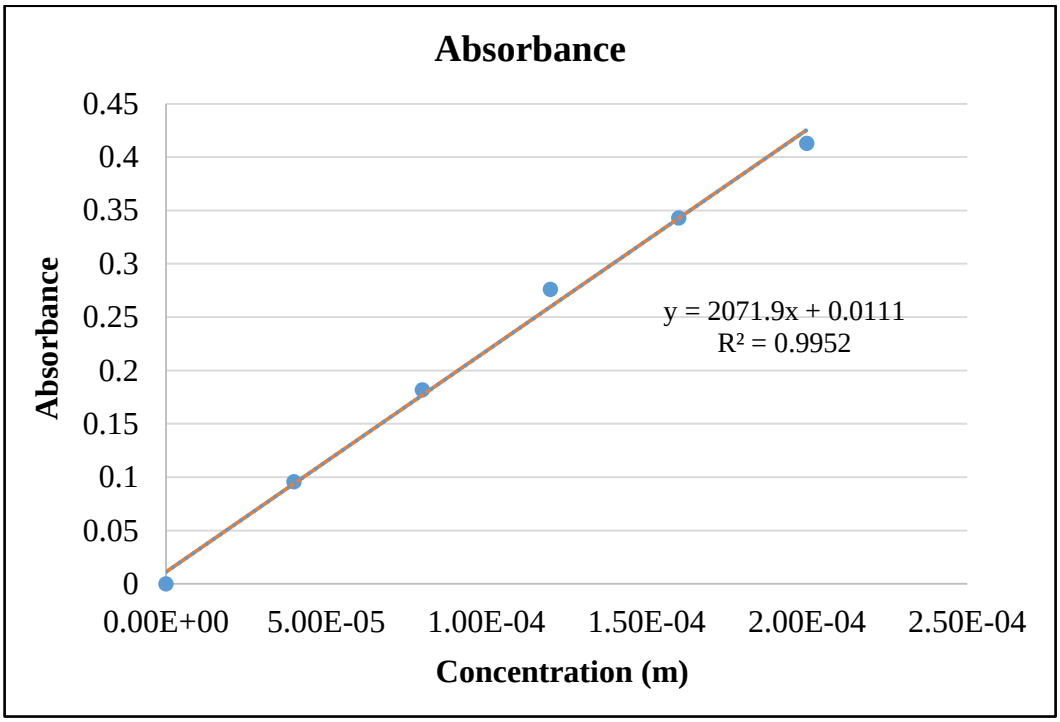


Figure 8.16: An estimation of true relationship between concentration and absorbance

Source: (Linear Regression - NC State University, 2004)

By the fluctuating curve pattern between the average shear strengths and the accelerated thermal time, the shear strength has the characteristic of a negative correlation to the ageing temperature cycling, and is considered to be nearly non-constant; hence the BGA solder joints are not entirely reliable. Thus the result of the shear test was dependent upon the solder material (flux) and also the condition of the solder joint layer about surface tension.

Having observed the relationship between the average shear force/strength and the accelerated thermal time, the author concluded that the relationship is partially nonlinear. From the observation, however, and by considering the correlation coefficient of r = 0.762 and the variance or coefficient of determination of $R^2 = 0.5813$ obtained from the regression line, the result shows a decreasing trend in the failure of the solder joint after only 33 hours in the field. This outcome suggests that the bonded joints are partially reliable and significantly affects the life cycle shown by a decrease in shear strength as cycle time and ageing increases. The steep drop and rise (Figure 8.12, and Figure 8.15) may have been caused by thermal fatigue, recrystallization and drop in flux chemistry of the solder joint as the temperature cools down from 150^0C to room temperature (of 20^0C down to 0^0C). Also, the thermal expansion mismatch otherwise known as CTE and different mechanical properties of the bonded materials such as the FCB (7ppm/^{0}C) and the FR4 board (18ppm/^{0}C) with a total maximum displacement possibility of up to -14µm can be responsible for low drift (Bhatia et al., 2010).

8.5.3 Study on the BGA Solder Balls Surface Fracture

The surface fracture observed during the SEM examination (Figure 8.17) shows that the interfacial reaction between the FCB and the BGA at the reflow stage with a peak reflow temperature of 236^{o}C indicates ductile fracture as represented in the SEM images given in Figure 8.18-8.22. The micrographs of the BGA solder joints, which were reflowed at 0.133 hours and thermally cycled for 33hours, 66 hours, 99 hours, and 132 hours respectively were observed to have experienced ductile-brittle fracture at the joints interfaces, including rapid but slightly partial shrink like crack propagation on the bulk solder interfaces. Yellow stripe also indicates the outcome as shown in Figure 8.18 through to Figure 8.22. These modes of fractures seemed to have resulted from the grain boundaries of the solder material (flux) at high temperature during the accelerated thermal cycling test. The observed ductile-brittle fracture determination emanated from the fracture surface appearance and the shear strength values. Images of the observed fracture modes were once again, presented in Figure 8.18 through to

Figure 8.22 for clarity. It is evident that more cycling/ageing time is required to enhance the growth of more intermetallic in the joint's common interfaces, which might lead to crack inducements and propagations that can be viewed clearly through a microscope.

Figure 8.23 shows some dark coloured areas on the BGA solder joint. The red circles represented the results of the depleted, deformed, and thick layers of solder material (flux), and these results outcome are attributive to the effect of substrate component interconnect at reflow and thermal/isothermal ageing. From the previous solder joints' parameter values (estimated), unsuitable flexible substrates stiffness and bump dimensions are critical to achieving a robust and more reliable solder joint on FCB. The use of soft FCB can lead to significant deformation of the PCB which, may occur during bonding process. This deformation has a direct influence however on the quality of the joints (Bhatia et al., 2010). A detailed presentation of the bench-top SEM image used for the examination of the solder joints' microstructure is in Figure 8.17. The information shows (a) Image of samples placed under a small vacuum of the SEM vice (b) sample size magnified, and (c) Image of solder-joint profile displayed on desktop and used for SEM test observation.

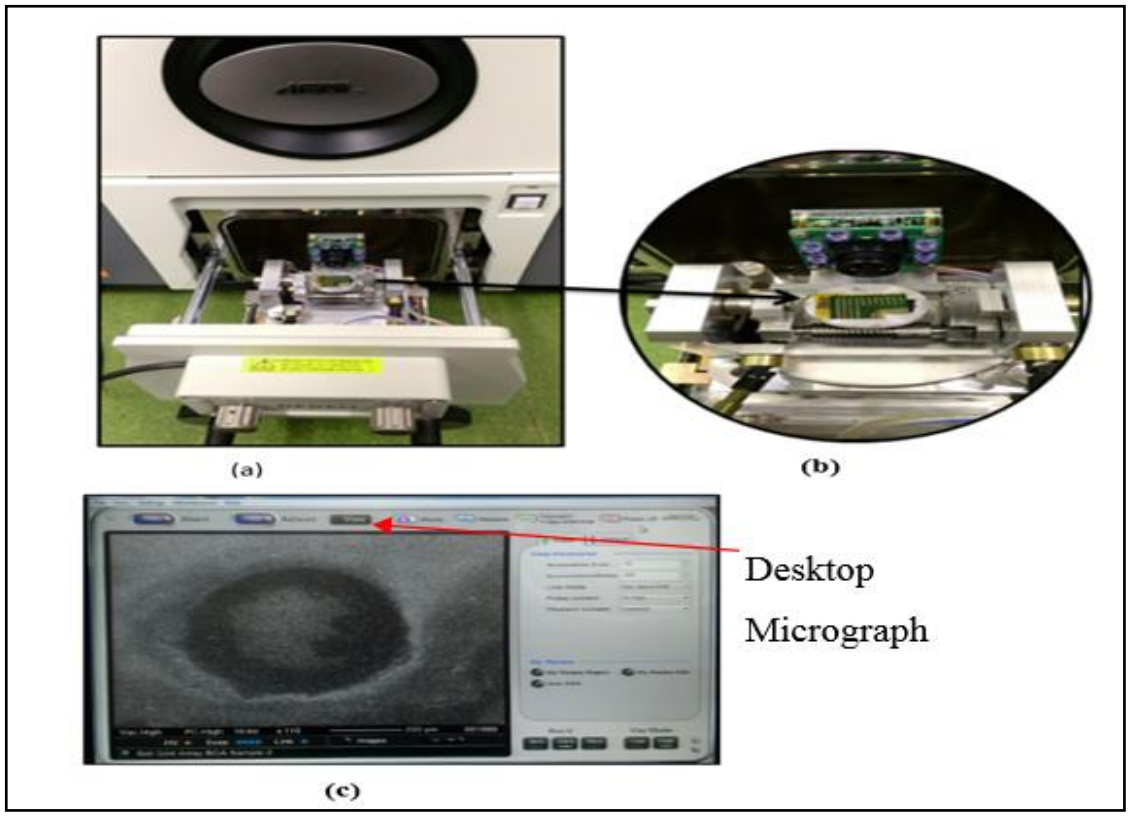


Figure 8.17: SEM surface fracture examination of BGA solder balls joints

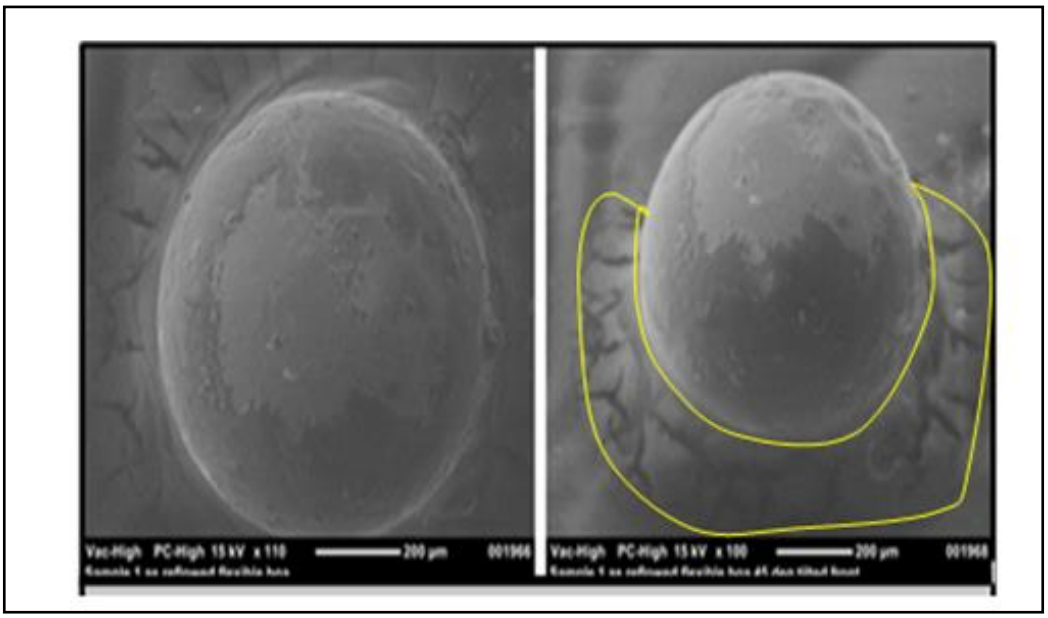


Figure 8.18: SEM images of solder joints as-reflowed at 0.133hours

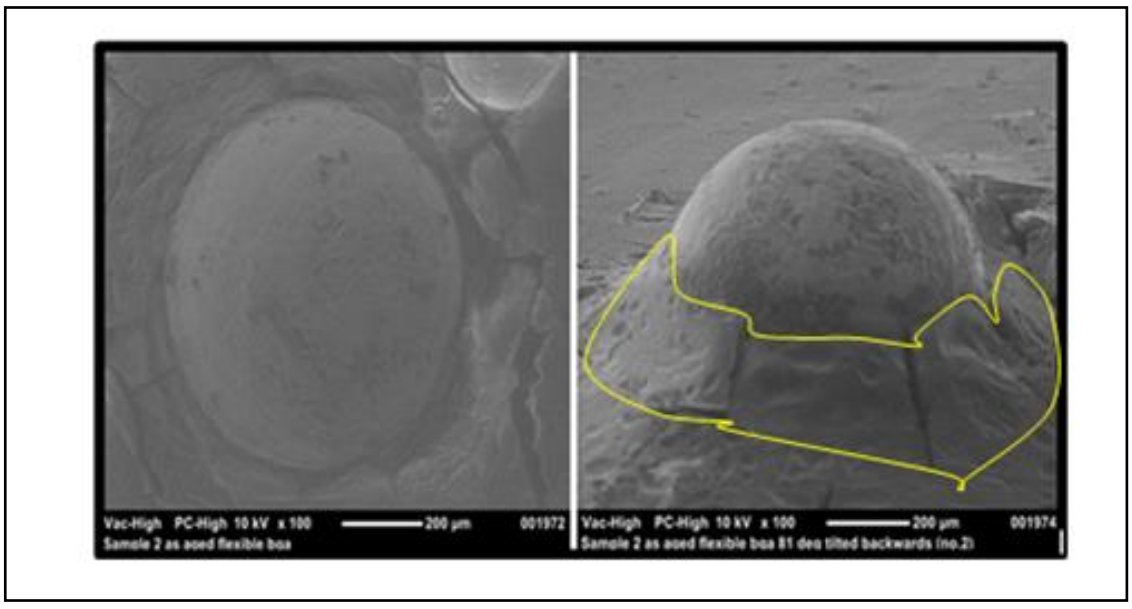


Figure 8.19: SEM images of 33 hours ageing sample

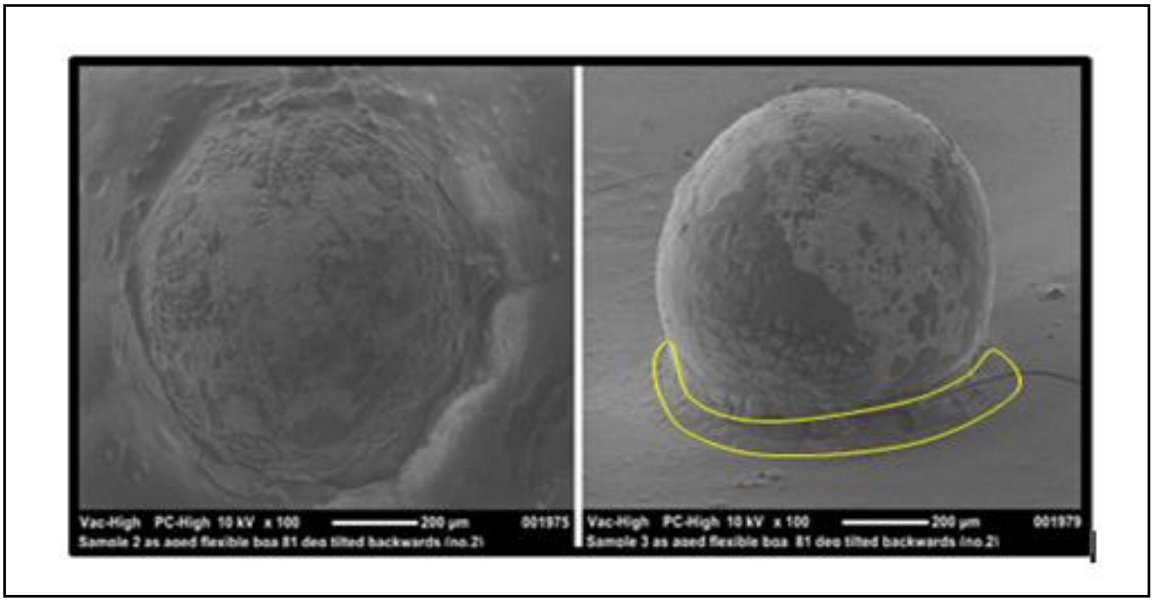


Figure 8.20: SEM images of 66 hours ageing sample

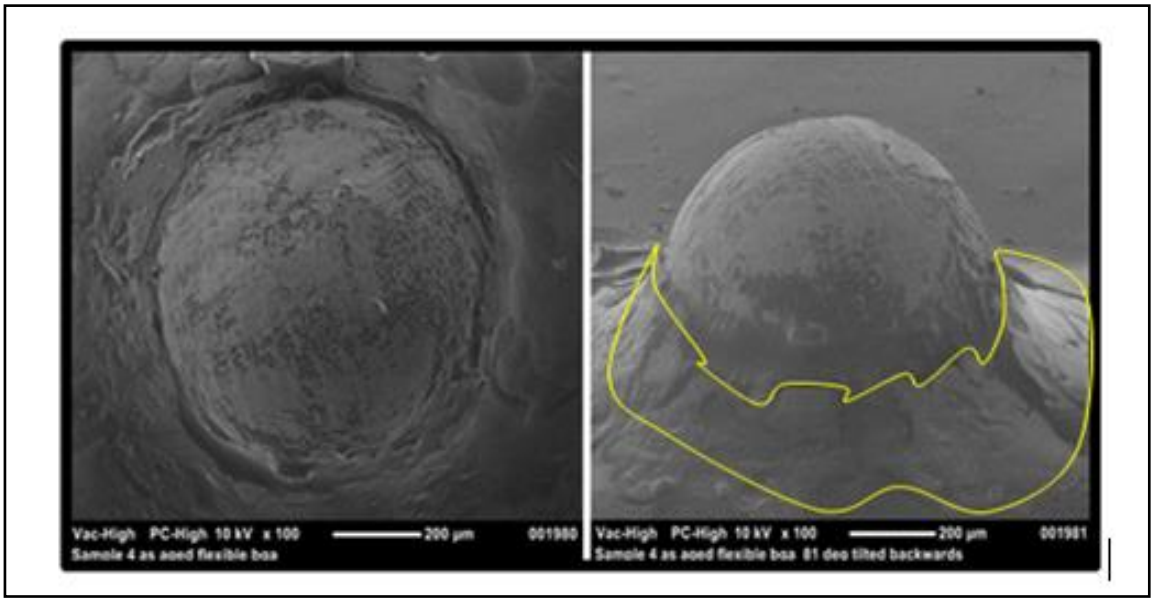


Figure 8.21: SEM images of 99 hours ageing sample

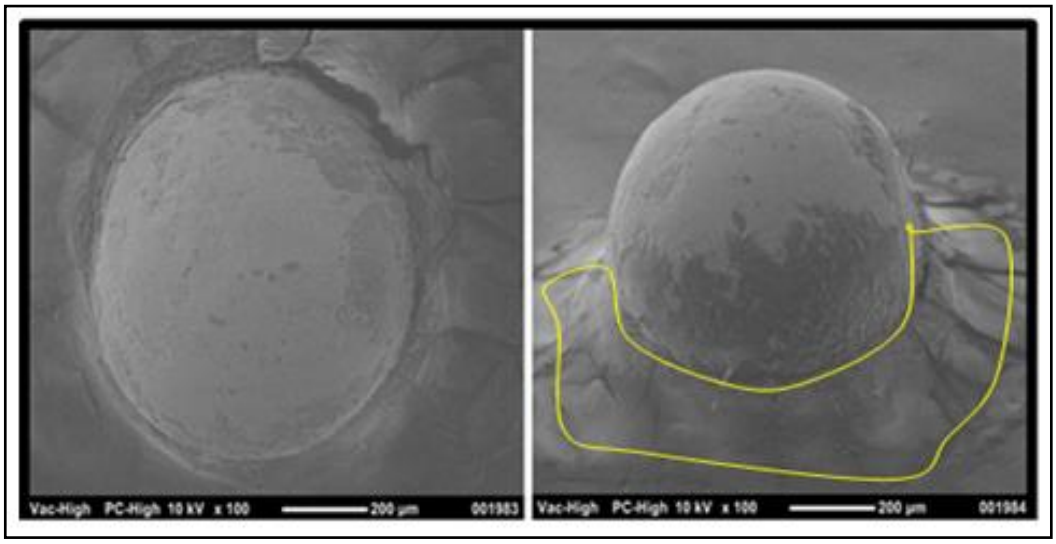


Figure 8.22: SEM images of 132 hours ageing sample

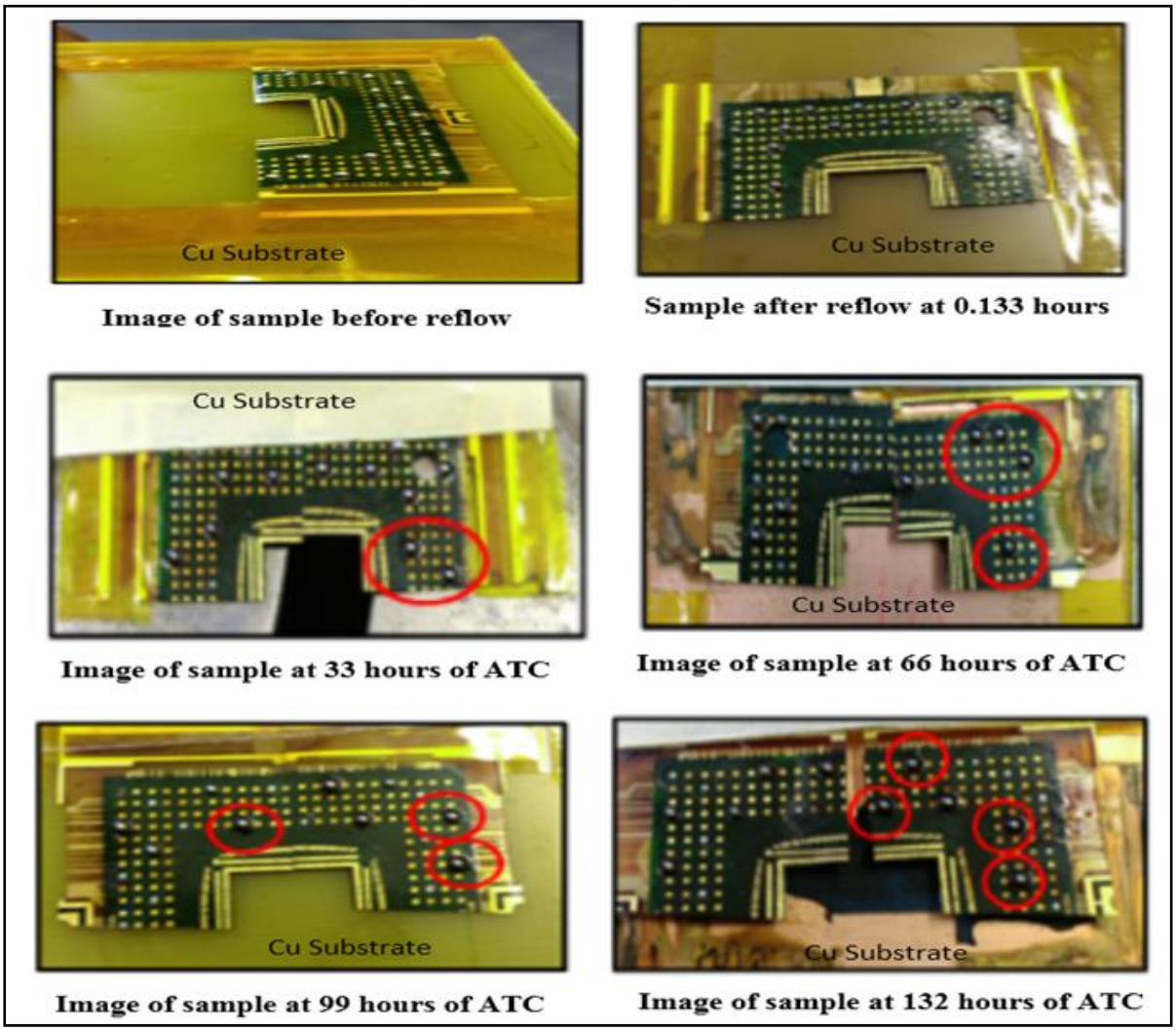


Figure 8.23: Images of excise and thick layers of solder material balls

8.6 Chapter Summary

In this section, a study on the long-term reliability of solder joints has been carried out, and the results of the laboratory tests are presented and analysed. Discussions were baesd on the tabulated data generated from the shear test results, and the SEM images of the BGA solder joints, examined for ductile-brittle effect. However, some improvements and gaps in the literature concerning this study are necessary. For example, performing an experiment to investigate the behaviour of BGA solder joints, by measuring the MTBF/MTTF will be supportive for a more critical evaluation and assessment of the reliability of the solder joint at extended operation in the field. The determination and examination of the effect of CSH and IMC layer thickness on the integrity of the SnAgCu lead-free solder balls joint metallisation with the flexible PCB used in this study would reveal the reliability requirements of the bonded materials, which will also benefit component manufacturers. The following conclusions are drawn based on the results of the investigation:

- Accelerated thermal cycling ageing affected the shear performance of the packages by changing (coarsening) the microstructure of the solder joints.
- The volume of the solder material (flux) influenced the relationship between the average shear force and the accelerated thermal time.
- An increase of 29.3 % shear strength, observed at 33 hours, can be controlled by the temperature gradient.
- The soldered samples at reflow exhibited ductile fracture during the shear test.
- After 33 hours, observed micrographs indicte ductile-brittle fracture surfaces, and as the cycle time increases, the surface of the PCB becomes more brittle.

Chapter 9: Results Summary, Conclusions, Contributions, Recommendations for Future Work, and Publications from the Study

9.1 Introduction

This chapter presents the summary of the results of work reported in this thesis on the thermomechanical reliability of lead-free solder joints used in the assembly of surface mount electronic components. From the results obtained, several conclusions were drawn and recommendations for future work are made based on the research output. In this chapter, publications and possible publications from the study are also presented.

9.2 Results Summary

In this study, the thermomechanical reliability of solder joints used in the assembly of 'Surface Mount' Electronic Components (SMECs) was evaluated. Results show that the reliability of solder joints depends hugely on their manufacturing process, thermal properties of the lead-free solder paste/balls, the reflow process parameters used and the component standoff height (CSH). Solder joint standoff height (CSH) plays a significant role in chip-packaging interaction and influences to retard the integrity of the soldered joint and the component if not properly optimised. Also, the standoff height of BGA component assembly can be controlled reliably using temperature variation and variation of diameter of the bond pad on substrate PCB. By decreasing the CSH, the shear strength of the solder joints increased. Thus, the CSH has a significant contribution on the structural reliability of solder joints in BGA assembly and chip size packages. The utilisation of the findings in design and manufacture of an electronic device, which when subject to shear and other related environmental loading conditions such as shock or impact loading, would result in the production of improved reliable products.

9.3 Conclusions

The conclusions drawn from the results of this study and the observations made in the course of this research work are summarised as follows:

1. The results from the evaluation of the thermomechanical reliability of surface mounted chip resistors Pb-free solder joints used in electronic manufacturing showed that shear strength of solder joints was found to be insignificantly independent of the shear rate used and that solder joints fractured through both ductile and brittle fractures. In essence, no change in fracture mode detected with increasing shear rate and ageing. Though similar observations

made in the shear strength values were obtained for aged and non-aged solder joints – implies that Pb-free solder joints can sustain high-temperature ageing. On analysis of the failed joints under shear test, the failure mode is occasioned by brittle fracture occurring at the boundary between the IMC layer and the solder bulk. Another failure mode observed was pad lifting. Moreover, the fracture locations induced by the shear test match with the failure locations during reliability testing; indicating a correlation between shear strength and time to failure could exist but thus require a larger sample size to prove this fact more coherently.

2. The results from the effect of Reflow profile using Taguchi DoE on the shear strength of surface-mount chip resistor solder joints showed that the reflow soldering parameters effects differ on the type and size of chip resistor. However, the characterisation and optimisation of the reflow parameter settings are key to achieving a higher shear force for solder joints of chip resistors. The result of the formation and growth of IMC depends on preheat slop and the cooling rate.

3. The results from the evaluation of the thermomechanical reliability of surface mount BGA81.1.0-Tn.ISO and BGA169.1.5-Tn.ISO solder joints shear strength (SJSS) showed that for both as-soldered and soaked assemblies' the standoff height of BGA components can be controlled reliably using variation in temperature and of the diameter of the bond pad on substrate PCB. By decreasing the CSH, the shear strength of solder joints increased. Thus, the CSH has a significant contribution on the structural reliability of solder joints in BGA assembly. From the research carried out in this thesis, the optimal CSH of 0.2.mm with a flexural stiffness of 109.59 MPa for a BGA81.1.0-Tn.ISO and CSH of 0.435mm with the temperature range of 225 ± 5^{0}C for a BGA169-1.5-Tn.ISO proposed. These results are consistent with a mathematical model developed by the author using Cantilever effect and Hooks laws (Njoku et al., 2015).

4. The work carried out on prolonged operations simulated by soaking the assemblies at an elevated temperature of 150^{0}C induced formation and growth of IMC in the solder joints. It also produced an evolution of solder microstructure and reduced the shear strength of the joint. These findings point out that lead-free solder joints in devices operating at high homologous temperatures are more likely to fail untimely than the ones in consumer electronics operating in normal ambient conditions.

5. A study on the production of assemblies with desired CSH showed that the use of SEM outweighs the Vernier Height Gauge (VHG) measurements. The devices production was evaluated using Tin surface finish (SnSF) and Copper surface finish (CuSF) to determine which of the two methods were easier to produce the desired CSH that is more dependable. The assemblies produced with copper board finishes (CuSF) collapse and bridge in most cases. These defects were not observed in the parts produced using PCBs with SnSF. This behaviour may have resulted from the differences in the substrates used. PCB with SnSF has a low capacity for heat absorption and conduction than the bare copper board. Thus, producing the assemblies with bare copper substrate were more difficult at high temperatures. The author suggests that this aspect of investigation requires PCB with SnSF.

6. The results from work done on long term reliability of flexible BGA solder joints under accelerated thermal cycling condition showed that accelerated thermal cycling ageing adversely affected the shear performance of the packages by changing (coarsening) the microstructure of the solder joints with a significant decrease in the shear strength of the values observed. This outcome could be attributive to the resultant effect of the relationship between the average shear force and the accelerated thermal time, influenced by the volume of the solder material (flux) and temperature gradient. The soldered samples at reflow exhibited ductile fracture during the shear test. A ductile-brittle fracture surfaces in the joints, also traced after 33 hours of thermal cycling ageing. However, as the cycle time increases, the surface of the flexible PCB became more brittle.

7. Results obtained from “X-Ray Analysis of Voiding in Lead-Free Soldering" using Taguchi's orthogonal array, and full factorial design of experiment show that solder bump size and shape substantially impact voids formation in solder joints. The long soaking period during reflow soldering induces a more adverse effect on solder voiding by reducing their impact. Smaller solder particles in solder paste tend to accelerate 'Voiding' formation in solder joints. 15% to 25% is an acceptable limit for the voiding. Although a limit on the acceptable level of voids has never been establishing as a different manufacturing company is using a different degree of limit for the safest course of action (Ladani and Razmi, 2009; Otiaba, Okereke and Bhatti, 2014; Ning-Cheng, 2002). The optimum condition results for full factorial design and the highest result from Taguchi’s design has less voiding level than acceptable limit of 15%.

8. On further analysis of the effects of voiding, 'Surface Finish' (SF) posed as a significant and critical factor in the experiment. The Copper surface PCB used produced more voids than the Ni surface PCB. Some previous research revealed that bare copper or OSP copper finishes PCB surface produced more voids than gold (Au), Ni or immersion silver (Ag) PCB surface finishes, because of different wetting speed for the different surfaces. Wetting speed will be a clean surface and the flux that wets the entire pad is slow on copper than is in gold. Slow wetting may be more of a high volatile trap in a molten solder, and therefore, insignificant and void creation is likely to increase due to higher surface tension associated with lead-free solders.

9.4 Contributions

This research work on the thermomechanical reliability of lead-free solder joints used in the assembly of surface mount electronic components added some valuable specific and general contributions to knowledge in the field of solder joint reliability and electronics component assembly, which are as follows:

9.4.1 Specific contributions

- Demonstrated that by optimising reflow-soldering parameters, the microstructure and mechanical strength of solder joints in SMC assembly can improve to increase the thermo-mechanical reliability of the joints.

- Demonstrated two techniques using temperature and pad size to decrease solder joints' CSH to achieve improved shear strength of solder joints in SMC assembly.

- Established an optimal CSH of 0.2.mm and 0.435 mm for BGA81.1.0-Tn.ISO and BGA169-1.5-Tn.ISO respectively.

- Established technique and procedure to decrease voids formation in solder joints and improve the joints thermo-mechanical reliability.

9.4.2 General contributions

- The experimental outcome on miniature Pb-free solder joint assessment after the ban on SnPb on 1st July 2006 in the EU region; has demonstrated that the alloy fractured through both ductile and brittle fractures. The alloy can sustain high - temperature ageing, up to 150 ^{0}C. The shear strength of the solder joints is insignificantly independent of the shear rate used.

- The experimental outcome using Taguchi DoE confirmed a simulation proposed model by (E. H. Amalu et al., 2011) that the reflow soldering parameters effects on solder joints shear strength differ on the type and size of SMT chip resistor used.

- The experimental outcome also from Taguchi DoE achieved higher shear forces of chip resistor solder joints via optimisation of both the preheat slope and cooling rate. It may be because the formation and growth of IMC mostly depend on these factors.

- The experimental outcome on BGA81.1.0-Tn.ISO and BGA169.1.5-Tn.ISO Pb-free solder joint assessment to show that for both as-soldered and soaked assemblies' the standoff height of BGA components can be controlled reliably using variation in temperature and of the diameter of a bond pad on substrate PCB.

- The recommendation of an optimum CSH of 0.2mm with a flexural stiffness of 109.59MPa for a BGA81.1.0-Tn.ISO and CSH of 0.425 mm with a temperature range of 225±5^{0}C for a BGA169-1.5-Tn.ISO with CuSF and up to 235±5^{0}C with SnSF PCBs. For good joint reliability, at least, 56% of each solder ball diameter for all SMT area array components (BGA, FC-BGA, and CSPs) should represent the CSH.

- The experimental outcome on the thermomechanical reliability of Pb-free solder joint assemblies soaked at an elevated temperature of 150^{0}C, induced formation and growth of IMC in the solder joints. It also caused the evolution of solder microstructure and reduced the shear strength of the joint.

- The recommendation on assemblies produced with copper board finishes (CuSF) are unfavourable because they collapse at elevated temperatures and cause bridging in most cases, but in contrast, observations made in bonded devices produced using PCB with SnSF are optimal for quality and durable appliances.

- The recommendation on solder flux activation, on flexible BGA assemblies at high temperatures above 150^0C under accelerated thermal cycling condition demonstrates that flux can cause the microstructure of the solder joints to coarse, and lead to a significant decrease in shear strength of the device.

- The experimental outcome on voids formation in solder joints demonstrates that solder bump size and shape significantly affect them, as observed, voids increase with a decreasing number of bump sizes. 15% to 25% recommendation is an acceptable limit for voiding in bumped solders. A long soaking period can reduce voiding in Pb-free solder joints.

9.5 Recommendations for Future Work

1. Further research/experiments are needed in solder reflow process using Taguchi design of experiment in an isothermal environment with temperature and humidity constant. The isothermal condition of 150^0 C was used for 48 hours and for 250 hours to see if the reliability gets affected or not. After analysing the results, the decision was that isothermal ageing with the specified conditions does not have an impact on the structural reliability of the SJs. The variation in the atmospheric condition introduces errors into the experiments, more especially during the reflow soldering process. The solder joint's microstructure was analysed for any changes, which might develop due to changes in the humidity.

2. An inclusion of more factors in the study is needed, for example, the stencil printing process, which serves as one of the important influences of voids in lead-free solder joints is a factor for an extensive studied. In consideration, the particle size of the paste can serve as a level of adhesive. The preheat temperature, flux activation temperature and the time spent in every zone should be reckoned to get a better understanding of the influence of reflow profile. Silver and gold finishing surface PCBs should be considerably in comparison with Ni surface PCB using lead-free solder paste, as their differences were yet unknown since the advent of lead-free solder paste in July 2006.

3. The isothermal ageing carried out on the effects of CSH on the shear strength of BGA under varying temperature and pad sizes was conducted at 150^0C for periods of 2days, 4days, 6days and 8days for 200hours. Future research works in this area could be carried out at different ageing temperatures for a prolonged period of about 2000hours. The result, which will enhance the comparative analyses between the ageing temperatures and times, and how they both influence the CSH and shear strength under varying pad sizes.

4. Experimental results obtained from work on CSH of solder joints showed that IMC plays a significant role in the shear strength behaviour and fracture mode of BGA solder joints. Future actions should consider the IMC layer thickness measurement, for the different pad sizes. The determination would further support the results analysis about the optimal shear strength and CSH values obtained.

5. Effect of the rapid (i.e. high speed) shear rate on solder shear strength is required. It will provide a full knowledge and proper understanding of shear-rate dependence behaviours of

dynamic solder joints as against the rate-independence reported in Chapter 5 of this thesis. From the observations and suggestions, the contrast may have resulted from the Dage Tester used in this research that has limited decades of time (e.g. 700μm/s = 11.67 strain rate sec-1) and may not be necessary for high-speed shearing. It is therefore recommended that a similar research study be conducted on 'effect of high-speed shear rate on solder shear strength' using a Dage Bond Tester that can cover at least four decades of time (104 strain rate sec-1).

6. Insufficient flux application when preparing some of the test vehicles led to inaccuracies in their results. Also, the shelf life of the flux utilised for this project work is not determined. Subsequent studies should consider the shelf life of the flux to avoid using contaminated products, including sufficient flux application for efficient reflow soldering.

7. Having examined the effect of CSH on the reliability of lead-free BGA169 solder joint at regular (or constant) pad sizes in this study, it is necessary to base future work on the study of the effect of varying pad sizes on the shear strength of BGA solder joints using the same BGA169. The study will help to establish the pattern of influence of the differences in the pad sizes on the reliability of the solder joint. The misalignment of some of the BGA components on the PCB was a critical issue during placement by a pick and place (PnP) machine. The author suggests that future works should be performed with a better vision-assisted PnP device to correct the misalignment issue of BGA packages on their PCB terminations. The advantage of a good choice of PnP is to allow the obtaining of better and accurate results.

8. The shear test of the BGA169 assembly should be carried out in future using higher load bearing cartridge and tools, which will be able to support weight range of over 2500N thereby eliminate the need to section the BGA169 assembly to reduce the shearing load during the mechanism of the destructive shear tests performance. The effect of IMC on the failed solder joints after the destructive shear test stands in the future as an area of improvement for this just-concluded study.

9. Further optimisation of BGA assembly is required using Taguchi orthogonal array $L_9(3^3)$. The analysis method could be on Signal-to-Noise ratio (S/N), with control factors as component type, aged duration and homologous temperature. However, much emphasis should be on the determination of the effect of ageing, operating temperatures and optimal

parameter settings for various types of BGA assembled on the same PCB. The use of a correction factor, which is beyond the scope of this study, may be needed due to thermal fluctuations to align the graph curves to the right trend for analysis purposes.

9.6 Publications from the study

- Jude E. Njoku1, Sabuj Mallik1, Raj Bhatti, Emeka H. Amalu and N.N. Ekere, Effect of CSH on Thermomechanical Reliability of Ball Grid Array (BGA) Solder Joints operating in High-Temperature Ambient, In 38th Int. *Spring Seminar on Electronics Tech.*, ISSE May 6-10, 2015, pp.231-236. IEEE, 2015, (Published).

- Jude E. Njoku, S. Mallik, R. Bhatti, E.H. Amalu and B. Ogunsemi, Effects of Component Stand-off Height on Reliability of Solder Joints in Assembled Electronic Component, 20th European *Microelectronics and Packaging Conference Proceedings*, 14 Sep-16 Sep, EMPC 2015 Germany, IEEE, 2015 (published).

- Mallik, S., Njoku, J. and Takyi, G. (2015) Quantitative evaluation of voids in lead-free solder joints, *Applied Mechanics and Materials*, 772, pp. 284–289. (Published)

- Mallik, Sabuj, and Franziska Kaiser (Presented by Jude Njoku (2014),). "Reliability study of subsea electronic systems subjected to accelerated thermal cycle ageing." *Proceedings of the World Congress on Engineering*. Vol. 2. IEEE, 2014 (Published).

9.6 .1 Other Publications

- Jude E. Njoku, Sabuj Mallik, Raj Bhatti1, Emeka H. Amalu and N.N. Ekere, Effect of Reflow Profile on Thermomechanical Reliability of Surface Mounted Chip Resistor Solder Joints, *Soldering and Surface Mount Technology*, (Submitted Journal).

- Jude E. Njoku, Sabuj Mallik, Raj Bhatti, Emeka H. Amalu and N.N. Ekere, Effect of Component Stand-Off Height on Thermomechanical Reliability of Ball Grid Array (BGA) Solder Joints in Electronic Assembly, *Soldering and Surface Mount Technology* (Submitted Journal)

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