A computational investigation of the effect of three-dimensional void morphology on the thermal resistance of solder thermal interface materials.

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Abstract

Process-induced solder voids have three-dimensional shapes and show spatially random distribution with polydisperse geometric dimensions. There exists no analytical formulation of thermal resistances which incorporates void shapes, distribution and polydispersity variables. This paper uses finite element methods to investigate the effect of realistic void morphology on the thermal resistance of solder thermal interface materials (STIMs). The study has developed two computationally efficient methods for generating voids that show the features of real voids. Cylindrical and spherical void morphologies have been studied. The study is the first attempt, in literature, of characterizing the holistic effects of such realistic three-dimensional void morphologies on the thermal resistance of STIM layers. We have shown a qualitative agreement between our results and simplistic analytical predictions. However, the influence of void shapes, distribution and polydispersity have been shown to contribute to increased thermal resistances. The findings should provide significant insight to electrical/electronics engineers, micro-electronics chips manufacturers and academic research groups working on thermodynamics design of chip scale package (CSP) devices. It is also a framework for investigating objectively, the consequence of voids on the thermo-mechanical response of solder joints.

Keywords: void morphology, solder thermal interface materials, thermal resistance, microelectronics, three-dimensional, virtual testing

1. Introduction

There are two main drivers that influence the current development of power devices: miniaturization and improved cooling. First, there is an increasing trend for electronic components and power devices to be miniaturized such that multiple electronic circuitry/components can be housed within a compact landscape. As well as the miniaturization trend, there exist also legislations requiring that the power devices must demonstrate improved cooling. To

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address these two drivers, engineers are working on innovative package designs for power devices with contemporary designs mainly based on the integrated circuits (ICs) with chip scale packaging (CSP): a very promising implementation, amongst many others [1, 2].

Some of the common implementations of the CSP technology in power electronics designs include: the metal-oxide-semiconductor field-effect transistor (MOSFET)[3], ball-grid array (BGA) packages, flip-chip packages, flip-chip on flex (FCoF), integrated power electronics modules (IPEMs) [4], high-power light emitting diodes (LED) [5], etc. This paper is focussed on the flip-chip packages technology. Figure 1 shows a schematic representation of the flip-chip CSP arrangement. The chip (silicon die) is attached to a substrate with the latter bonded onto a PCB board using the ball grid arrays interconnections. Due to the flip-chip arrangement, heat dissipation is via the backside of the chip through the heat spreader, and a possible heat sink (not shown in Figure 1).

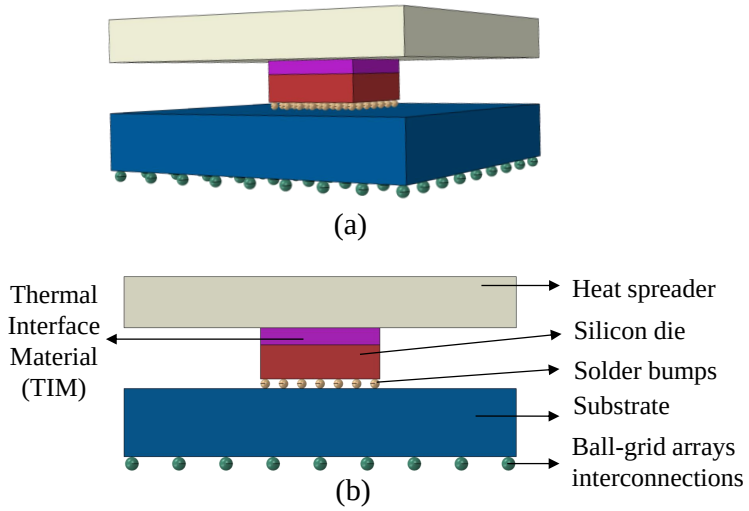


Figure 1: A schematic representation of a typical flip-chip CSP arrangement showing (a) isometric and (b) planar views, with the different components identified on the planar view.

Effective heat management in such high power-density chip packages is a priority. Heat conduction between the chip (silicon die) and the heat spreader is enhanced by the introduction of a thin layer of *thermal interface material* (TIM), also called the *die-attach* [6]. The TIM suppresses interstitial air gaps [7, 8] (see Figure 2) between the mating silicon die and heat spreader components, thereby ensuring the efficient transfer of heat from the silicon die to the heat spreader.

TIMs can be either polymer-based or solder-based with the later preferred due to their better thermal performance [9]. TIMs are very important in the CSP technology and deserves careful consideration, if the desired improved cooling of the CSP package must be achieved consistently. It is important that engineers objectively quantify the thermal resistance associated with the TIM layer as this will help design reliable packages that will perform adequately over the life of the product.

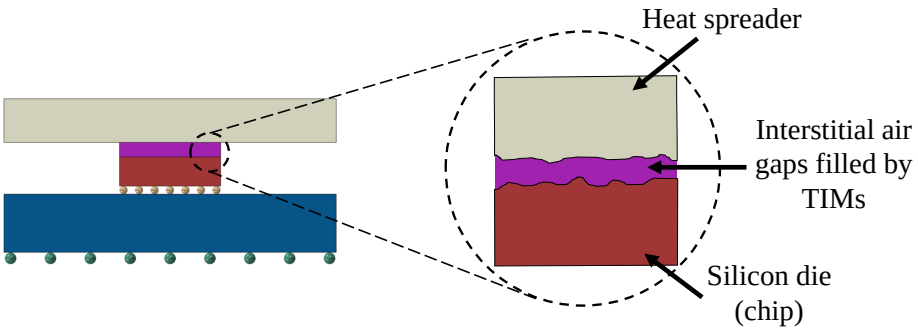


Figure 2: Illustration of how the thermal interface materials (TIMs) are used to suppress/fill interstitial air gaps between the mating surfaces of the silicon die and the heat spreader.

Although solder-based TIMs (STIMs) are preferred to other types, a major limitation of their use in practice is their propensity for forming voids during the manufacture/reflow process of the flip-chip packages [10]. When voids form, they lead to increased thermal resistances of the TIM layer and as a result reduce the effective thermal transfer between the silicon die and the heat spreader. This raises a reliability concern for their use in design of high power-density flip-chip packages. In the last seven years, there has been sustained publications in this field and some of the commonly cited authors are given in the following references [11–16].

Unfortunately, the prevalence of voids in STIMs is unavoidable due to the complex manufacturing process that solders are subjected to as well as other combination of factors, described in detail by Bušek *et al.* [17]. The formation of voids in solders result from outgassing during the solder reflow process, defective metallisation and poor wettability of solder [15]. The adoption of lead(Pb)-free solders have exacerbated the problem since the lead-free solders show poor solderability. Some studies have even reported more than 50% void volume fraction in some lead-free solder joints [18, 19].

Some recent attempts have been made to optimize the processing history solders are subjected to, in order to limit void formation. One of the recent methods is the *vapour phase soldering* (VPS) system, also described as, *condensation soldering*. This method is a reflow soldering method considered a viable alternative to conventional and infrared soldering methods [20]. The distinctive thing about the VPS approach is that the soldering of the printed circuit board (PCB) is done within an envelop of a vapour phase of a special heat transfer fluid, such that the heat generation and transfer that completes the reflow process is through the latent heat of the condensing mass of such fluid. The main benefit for this method lie in elimination of overheat, prevention of shadowing effect (especially in large components), as well as limiting the prevalence of voiding in the solder joint [21, 22]. In spite of its clear advantages, the VPS method is still fraught with such limitations as voiding (albeit limited), paste sputtering and tombstone failures [21]. Such approach and other emerging solder processing methods should serve to limit voiding in solder joints but not eliminate it completely, hence the investigation proposed here will always remain relevant to the soldering industry.

There are different classifications of voids that can be found within a solder joint for example: micro-, macro-, shrinkage, micro-via, kirkendall and pinhole voids [23]. The most common void type is the macrovoids and their diameters range from $100\mu m$ to 300 μm, while microvoids have diameters of less than 50 μm [17]. The macrovoids are usually process-dependent voids since they are caused by the manufacturing process. The flux type and amount on void formation during the manufacturing process of solder joints was studied by Bušek *et al.* [17].

The impact of voids in thermo-mechanical reliability of solder joints has been studied and reported extensively. Yu *et al.* [24] observed that voids influence the thermal fatigue resistance of CSP solder joints. The authors observed that small voids (i.e microvoids) have no apparent effect on fatigue life but when the voids are big, usually about 30% of the solder size, and located along the crack path, they adversely affect the fatigue resistance.

Le *et al.* [25] used finite element modelling approaches to investigate the effect of process-induced voids on the fatigue lifetime of lead-free solder joints subjected to thermal cycling. The authors observed that fatigue lifetime is inversely proportional to void volume fraction. Also, the location of voids affects the initiation and propagation of voids. Voids away from certain damage-prone locations did not adversely affect the integrity of the solder joints. Ladani and Dasgupta [26] used finite element modelling to investigate the effect of two-dimensional void shapes, their position, size and spacing on the durability of lead-free solder joints used in BGA packages. They concluded that voids contribute to damage initiation and evolution.

Yanus *et al.* [27] studied the effect of spatial representation of voids on the thermo-mechanical reliability of solder joints. The study observed that spatial positioning of the voids and their spatial distribution are significant indices for the reliability of the solder joint. Zhou and Qiu [28] used sub-modelling technique to investigate the spatial representation effects of voids on thermal fatigue reliability of BGA package and arrived at similar conclusions as Yanus *et al.* . The above studies show that the void morphology is a crucial design index in consideration of TIMs. In particular, the location of the void is critical as these lead to initiation and evolution of cracks within the material.

Published works on the influence of voids on solder joints tend to be focused on assessment of aspects of thermomechanical-related fatigue studies. Consequently, the test specimen is subjected to thermal cycling profiles that represent the sort of load histories that the electronic components are subjected to in practice. This area of research is now quite well understood. However, there is need to explore the influence of void morphology on the thermal resistance (exclusive of fatigue loading) of the solder joints. It has been reported that thickness of the solder [29] can significantly influence the fatigue life and as a consequence the thermal resistance. This work intends to explore the effect of changing solder thickness on thermal resistance.

In considering the void morphology, the void shape, size, spatial distribution are vital

features that must be incorporated within a numerical scheme investigating the influence of voids on thermal performance of flip-chip packages. The use of numerical modelling methods has grown significantly, especially as computing powers available to engineers continue to increase [30]. The development of virtual testing techniques [31] in investigating the thermo-mechanical behaviour of diverse materials has helped advance the numerical studies of void effects on flip-chip packages.

Before deploying a numerical solution to the void effects study, experimental characterizations of the void morphology need to be undertaken so that model validation data for the numerical scheme can be generated. The traditional approach used in void characterization is by use of microscopy studies but this is known to destroy the voids when the surfaces are prepared for the microscopy. Recently, computed micro-tomography techniques are proving very beneficial in realistic capture of the void morphology. This is because such technique is capable of non-destructive imaging of the solder joint volume, thus revealing in three-dimensions, the exact shape, size and location of the voids.

Also, 3D tomography data can be used as the virtual domain input to a finite element modelling scheme. This methodology is quite new in study of voiding of solder joints and often require specialist software skills to analyze and convert the 3D tomography data into a format acceptable to FEM solvers. Also, the acquisition of tomography data can be quite expensive as the X-ray tomography machines are usually very expensive. Figure 3 shows typical microstructural representation of voids as 2D (micrographs) and 3D (tomography) data.

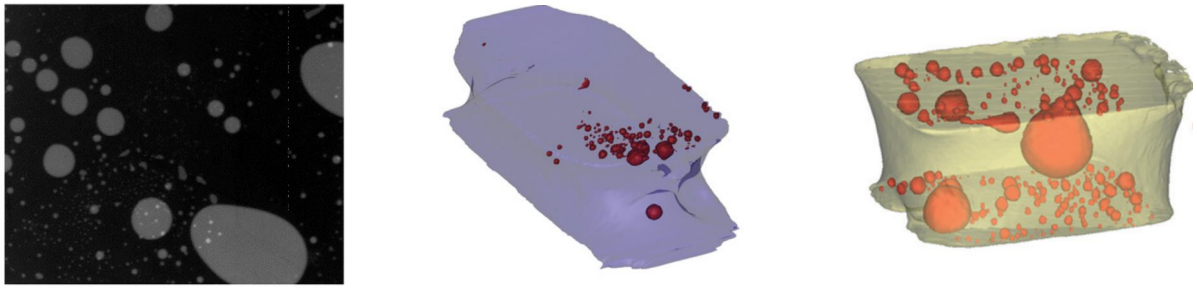


Figure 3: Microstructural representation of voids showing: (a) 2D micrographs (voids are gray shapes) [25] (b) 3D tomography of voided Pb-free solder joint [32], and, (c) 3D tomography of porosities/voids of a Sn-based solder joint [33]. Note that on the 3D tomography data, the voids are shown as reddish shapes of random spatial distribution, sizes and shapes. *Images reproduced with kind permission of Le* et al. *[25], Dudek* et al. *[32] and Padilla* et al. *[33]* .

Any method for artificially generating voids in solder joints must capture the spatial realizations, polydispersities and heterogeneities of the voids seen in Figure 3. Analytical methods exist for generating void morphologies but such methods often over-simplify the void morphology by enforcing a regular pattern of void distribution based on simple void shapes e.g. squares [34]. Apart from analytical methods, numerical approaches are becoming useful in describing void morphology that show the features of real void distributions

without resorting to expensive tomography techniques. Otiaba *et al.* [15] generated spatially random void patterns by a MATLAB-based algorithm called *MCRVEGen*, developed by Okereke and Akpoyomare *et al.* [35]. The authors used this approach to study the influence of void morphology on the thermomechanical behaviour of STIMs. The methodology was also adopted by Le *et al.* [25] to generate process-induced 'macrovoids' for investigation of the fatigue lifetime of solder joints subjected to thermal cycling.

The above void generation techniques are quite promising showing spatial randomness, however the voids are two-dimensional entities. Actual voids, shown in Figure 3, are three-dimensional entities which are not simply spatially random but also polydisperse (with varying diameters). The motivation of this study is to extend the existing understanding of void morphology by numerically generating voids that are three-dimensional and polydisperse: essential features for realistic voids.

This paper therefore presents two approaches of numerically generating process-induced solder voids with spatially random, three-dimensional shapes. Findings will provide a comprehensive evidence of the holistic effect of three-dimensional void morphologies on the thermal performance of solder thermal interface materials. Moreso, the proposed void-generation methodologies is fast and cheap, in comparison with voids generation based on X-ray tomography techniques. It is the objective here to investigate the influence of three-dimensional shaped voids (shape, size, spatial representation, void volume fraction and STIM layer thickness) on the thermal resistance of STIMs. The outline of paper includes: description of the numerical generation of three-dimensional voids; then, a brief presentation of the finite element analysis of the thermal response of the voids before concluding with parametric studies of aspects of the finite element solution.

2. Methodology

This study used a numerical modelling philosophy based on the finite element method to investigate the influence of void morphology on the thermal resistance of solder thermal interface material within a flip-chip CSP arrangement. Here, we present the methodology for numerically generating realistic voids before describing the theory of thermal resistance for such joints. Finally, the components of the finite element model are described.

2.1. Numerical generation of realistic voids

Previous numerical generation of voids were based on 2D representation of voids, according to the *MCRVEGen* implementation of Okereke and Akpoyomare [35]. In the following, we will described two methods for creating three-dimensional voids.

2.1.1. The MCRVEGen2D Method

The first method is based on the Monte Carlo Representative Volume Element (RVE) generator method, developed by Okereke and Akpoyomare [35] and used for investigating fatigue behaviour of 2D voids by Otiaba *et al.* [15]. In their work, as well as this, the voids have been represented as penny-shaped cylinders. This approach involves first using the *MCRVEGen* code to create a planar distribution of voids (red circles) as shown in

Figure 4(a), before subsequently extruding the circles to create the *cylindrical* voids (see Figure 4(b)). The void morphology shows random distribution on the XY-plane according to Figure 4. This method is called hereafter the *MCRVEGen2D* since the void morphology is based on an extruded 2D planar distribution of circular voids.

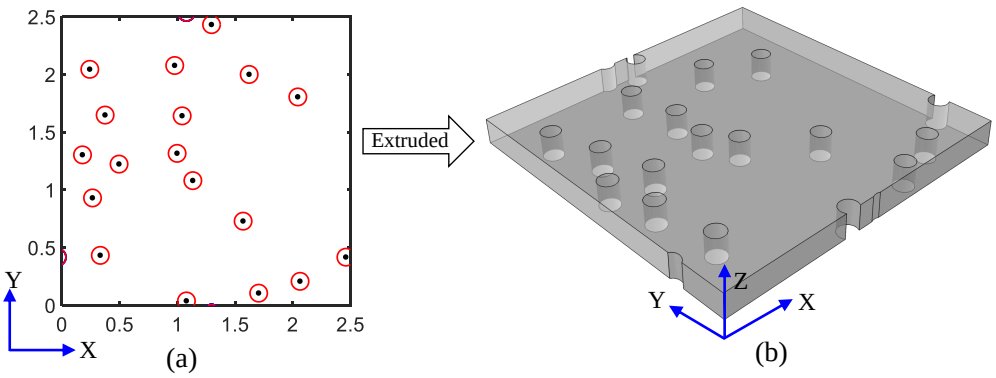


Figure 4: A two-step process for creating voided STIM with cylindrical void morphology, showing (a) planar view (created in MATLAB) and (b) isometric view (created in ABAQUS) of the STIM layer. The STIM layer is of dimension $2.5 \times 2.5 \times 0.20$ mm^3 and each void is of diameter, $D_f = 150\mu$m.

To determine the number of voids within a 2D planar RVE, let us consider a typical STIM layer of length, L, width, W, and height, H. If the number of voids in the STIM layer is N_f, then the void volume fraction for a void diameter, D_f, becomes:

$$V_f = \frac{N_f V_{voids}}{LWH} \quad \longrightarrow \quad V_f = \frac{N_f \pi D_f^2 H}{4LWH} \quad \text{or} \quad N_f = \frac{4V_f LW}{\pi D_f^2} \tag{1}$$

In the proposed numerical scheme, the void diameter, D_f and void volume fraction, V_f are given as input parameters. These can be obtained from micrographs of the voided STIM layer. The algorithm will determine the number of cylindrical voids, N_f which will populate the given RVE window of dimensions $L \times W$, thus resulting in Figure 4(b).

2.1.2. The Voxel Method

The second method of generating 3D voids is based on a *Voxel*-style *randomized* combination of geometric unit cells of voids. Each unit cell consists of an individual void created according to specified void dimensions, void volume fraction and unit-cell level spatial positioning. If the void is very close to the edge, such that it is shared between two or more adjacent unit cells, the implementation enforces the periodicity of the void, resulting in two or more surface voids appearing on opposite faces of the RVE.

Figure 5 shows eight examples of *Voxel* unit cells with inside and surface voids at different spatial positions. Since each unit cell was created according to a specified void fraction, therefore at the STIM structural level, the generated model will also inherit the unit cell void volume fraction. Polydispersity is achieved by creating unit cells that have various void diameters while ensuring the desired void volume fraction is kept constant for all the unit

cells.

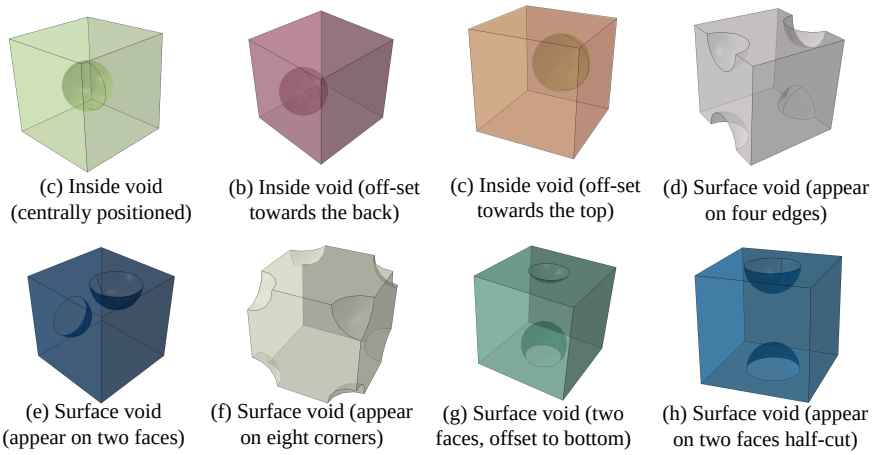


Figure 5: Illustration of eight types of *Voxel* unit cells showing different void positions.

The *Voxel* unit cells can be combined in a randomized manner into *Voxel* elements, as shown in Figure 6. This is followed by a randomized assembly of the *Voxel* elements which results in the voided solder model, of thickness, H. The order of combinations of unit cells into *Voxel* elements is random and the user defines a random operator that drives this. The only constraint exists for unit cells with surface voids that must be enforced with periodicity arguments. Similarly, the order of combinations of *Voxel*-elements into the solder model is also driven by another pre-defined random operator. Through this double-fold random operation, the desired random distribution of the voids is achieved.

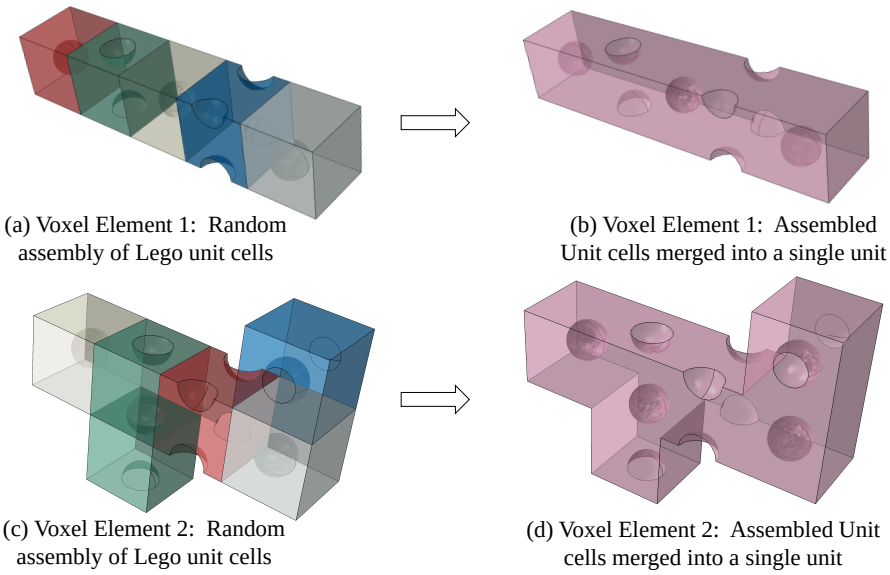


Figure 6: Illustration of two typical *Voxel* elements formed by randomized assembly of individual *Voxel* unit cell (shown in Figure 5).

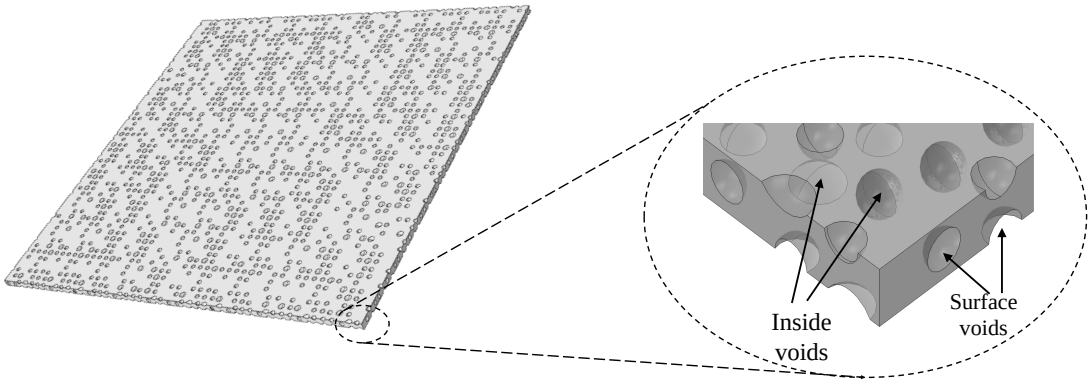


Figure 7: A typical RVE of a voided solder thermal interface material (STIM) created based on the *Voxel method*. Insert image shows a close-up view revealing spatially random surface and inside void patterns.

Figure 7 shows a typical voided STIM with a close-up image showing the random distribution of the voids, as expected for a realistic void morphology. Also, notice on the insert image the surface and inside voids. It is important to represent these type of surface voids as part of a realistic void morphology because literature shows that surface voids influence the thermo-mechanical response of the solder joint [15]. Finally, Figure 8 shows the algorithmic steps required in creating the 3D voids for the two approaches discussed in this work.

2.2. Theoretical calculations of thermal resistances

The study focused solely on the thermal conductivity through the three-components of the CSP package. The applicable governing equation for heat conduction, in all three dimensions is:

$$\boldsymbol{q}''(x,y,z,t) = -k\left[\frac{\partial T}{\partial x}\boldsymbol{i} + \frac{\partial T}{\partial y}\boldsymbol{j} + \frac{\partial T}{\partial z}\boldsymbol{k}\right] \tag{2}$$

where k = thermal conductivity $(W/K\cdot)$, T = temperature (K), t = time (seconds) and $\boldsymbol{q}''$ = is heat flux per unit area (W/m^2).

Using the schematic diagram of the CSP package shown in Figure 9, the dominant heat flux is along the $z-$axis. Therefore, the heat conduction equation along this axis, in view of Equation 2, can be simply written as:

$$q_z'' = -k\frac{\partial T}{\partial z} \quad \longrightarrow \quad q_z'' = \frac{q_z}{A_{chip}} = -k\frac{T_a - T_s}{L} \tag{3}$$

where T_s and T_a are temperatures at the source (chip) and ambient isothermal surfaces of the CSP model while k = effective thermal conductivity of the CSP model. A_{chip} is the area of the chip (silicon die) which for this study is $A_{chip} = 2.5^2$ mm^2. Also, L = total length of the CSP structure, along the $z-$axis and consists of lengths of the chip, L_{chip}, the voided STIM layer, L_{vSTIM} and the copper heat spreader, $L_{spreader}$. Re-arranging Equation 3, we can define the thermal resistance from the source/chip to the ambient/air, R_{sa} as:

$$R_{sa} = \frac{T_s - T_a}{q'' A_{chip}} \quad \longrightarrow \quad R_{sa} = \frac{L}{kA_{chip}} \tag{4}$$

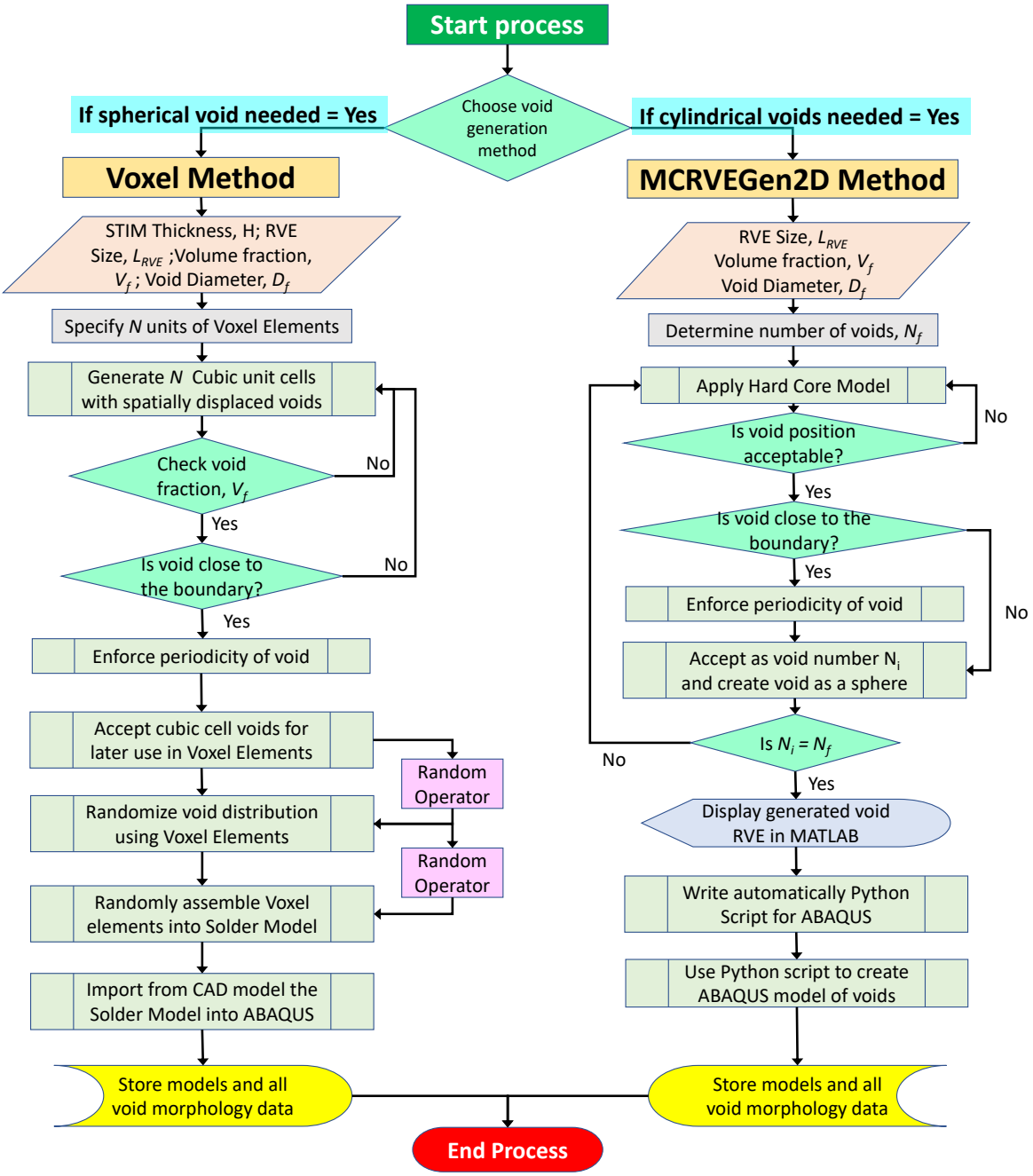


Figure 8: The algorithmic steps for generating cylindrical and spherical voids based on the *MCRVEGen2D* and the *Voxel* methods respectively.

The thermal resistance term R_{sa} can be determined from a numerical solution using finite element methods, as proposed in this work and the parameters, T_s, T_a, and q'' can easily be obtained from the numerical solution.

However, it is also feasible to determine the thermal resistance from source to ambient, R_{sa} based on analytical consideration of the thermal conductivities of the different compo-

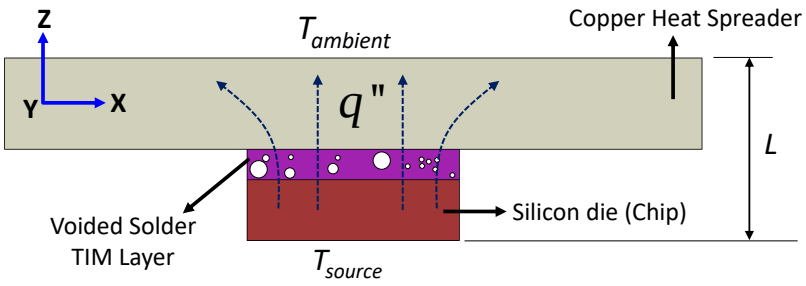


Figure 9: An illustration of the boundary conditions adopted for this study. The flow direction of the heat flux, q'', through the model is shown by the dashed lines.

nents that make up the CSP package. We have assumed a serial combination of thermal resistances for the three components that make up the CSP assembly under investigation i.e. the chip, the STIM and the heat spreader. Since the thermal resistance of a voided STIM should be higher than those of virgin STIM, we have therefore accounted for the effect of air (in the voids) by assuming a parallel combination of the thermal resistance of a voided STIM and the voids itself (containing air). The power network representation of the CSP package studied here is given in Figure 10.

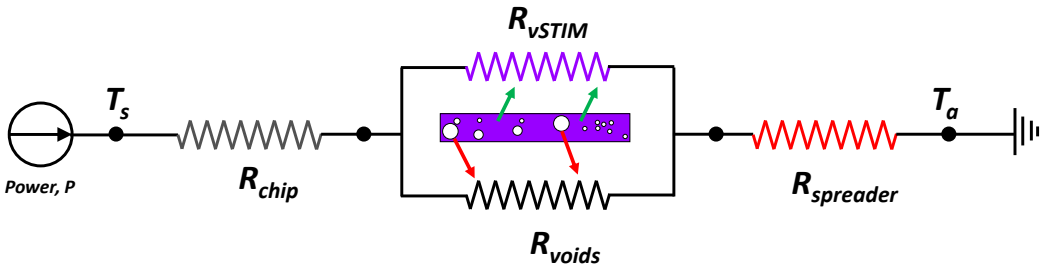


Figure 10: A resistance network diagram of the CSP model studied in this work, showing the thermal resistances of the chip, STIM, voids and the copper heat spreader.

Based on the resistance network diagram, the effective thermal resistance between the source and the ambient, R_{sa}^{eff}, can be defined by the sum of the thermal resistances of the chip, voided STIM and the copper heat spreader. The mathematical formulation of the sum of the serial thermal resistance network becomes:

$$R_{sa}^{eff} = \frac{L_{chip}}{k_{chip}A_{chip}} + \frac{L_{TIM}}{k_{vSTIM}A_{chip}} + \frac{L_{spreader}}{k_{spreader}A_{spreader}} \tag{5}$$

where k_{chip}, k_{vSTIM}, and $k_{spreader}$ are the thermal conductivities of the chip, voided STIM and the copper heat spreader. Also, $A_{spreader}$ = surface area of the copper heat spreader, and for this study $A_{spreader} = 5^2$ mm^2.

Ramos-Alvarado *et al.* [36] derived the expression of the voided STIM by considering the voids to be filled with air, and their resulting expression becomes:

$$k_{vSTIM} = k_{STIM}(1 - V_f) + k_{air}V_f \tag{6}$$

where k_{STIM} = thermal conductivity of the virgin STIM without any voids, and its value is given in Table 2 while V_f is void volume fraction. Also, k_{air} = thermal conductivity of air, and for this work, $k_{air} = 0.0262\ W/K \cdot m$. The R_{sa} parameter of Equation 4 is equivalent to an analytically determined effective thermal resistance, R_{sa}^{eff}, of Equation 5.

The R_{chip} and $R_{spreader}$ thermal resistances are constant and independent of voided STIM thickness and void volume fraction. However, R_{STIM} of the voided STIM is dependent on void volume fraction and STIM layer thickness. The numerical study reported in this work considers the dependence of thermal resistance on the STIM layer thickness and the void volume fraction: both parameters that are known to influence the thermal performance of the CSP assembly.

2.3. Numerical modelling

In this section, we present the features of the finite element numerical model used for the simulation. The features range from the virtual domain description, the material types, the mesh generation, applicable boundary conditions, and the analysis types. The finite element investigation was carried out using ABAQUS FEM solver [37] and all model inputs were created using ABAQUS/CAE and Python scripts (where necessary).

2.3.1. Virtual domain of FE domain

The virtual domain used for this study is an assembly consisting of the silicon die (chip), a copper heat spreader and the solder thermal interface material (STIM). Table 1 gives the dimensions of the three component parts of the flip-chip CSP package studied in this work. In order to assess the influence of the STIM thickness, H on the thermal resistance of the CSP package, five STIM thicknesses were studied namely: 40μm, 80μm, 120μm, 160μm, and 200μm. The diameter of the voids was from 50μm to 150μm and different STIM models with varying void volume fractions were created for the study.

Table 1: Dimensions of the component parts of the finite element model.

Component part	**Length, L (mm)**	**Width, W (mm)**	**Height, H (mm)**
Silicon die (chip)	2.5	2.5	0.30
Copper heat spreader	5.0	5.0	1.00
Solder TIM Layer	2.5	2.5	0.04 - 0.20[a]

[a] The STIM thickness was varied in increments of $40\mu m$.

2.3.2. Model materials

The study considers only the thermal response of the model assembly. The dominant mode of heat transfer here is conduction and characterized by the thermal conductivity, K, density, ρ and specific heat capacity, c. Heat transfer through radiation was neglected since the test temperatures were quite low to result in significant radiation. Convective heat transfer was also not included in this study, although including it might result to improved cooling of the CSP assembly. The conduction heat transfer considered here represents the

worst case scenario for the CSP package, thus adequate in highlighting the significant effect of void morphology. Table 2 shows the thermal properties of the different component parts of the flip chip assembly. These values were obtained from these references [15, 36, 38, 39].

Table 2: Thermal properties of the component parts of the finite element model.

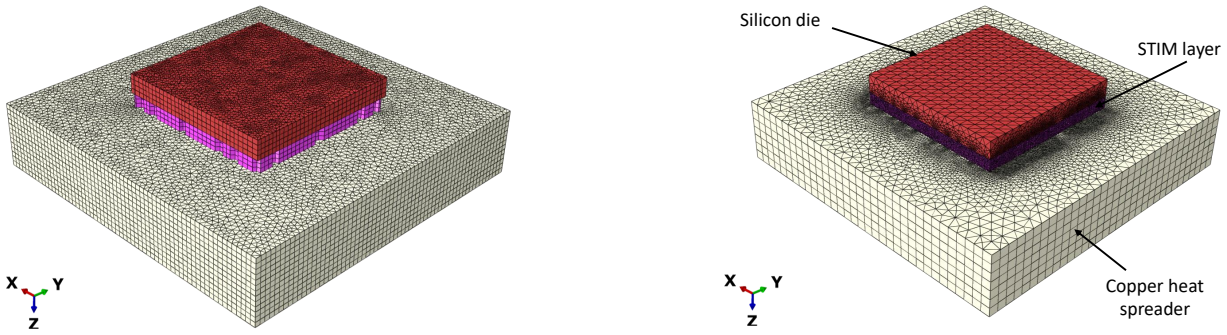
Component part	**Conductivity, k (W/K·mm)**	**Density, ρ (kg/mm^3)**	**Specific heat, c (J/kg·K)**
Silicon die (chip)	0.1100	2.32×10^{-6}	700
Copper heat spreader	0.4010	8.96×10^{-6}	380
SAC305 STIM layer	0.0578	8.41×10^{-6}	230

2.3.3. Model boundary conditions

The boundary condition chosen for this study is illustrated in Figure 9. This consists of a temperature at source, $T_{source} = 85^oC$, prescribed on the silicon chip, which represents the heat generated by the electronic circuitry. This heat needs to be conducted away to ensure improved cooling of the CSP package. On the other side of the flip-chip CSP package, an ambient temperature, $T_{ambient} = 20^oC$, has been prescribed on the copper heat spreader. As a result, the thermal gradient will be from the silicon chip to the copper heat spreader due to the temperature gradient between the two. The STIM layer is right in between these two components, hence we can quantify the effect of void morphology on the thermal resistance of the STIM layer appropriately.

2.3.4. Model meshing

The critical component under investigation here is the SAC305 STIM layer hence this was finely meshed. The discretizing element for the silicon chip and the copper heat spreader is a 3D solid elements with diffusive (heat transfer) element formulation. Figure 11 shows a meshed model of the CSP package for the cylindrical and spherical voided STIM layers.



(a) (b)

Figure 11: A meshed model of the CSP package showing the silicon chip, STIM layer and the copper heat spreader with the STIM layer containing: (a) cylindrical and, (b) spherical void morphologies.

The specific element type used for the spherical voided STIM is a four-node linear tetrahedral element identified as DC3D4 within ABAQUS FE solver. The copper heat spreader was discretized using a six-node triangular prism element, identified within ABAQUS FE solver by DC3D6. The STIM layer with cylindrical voids was discretized using the DC3D6 element type. Also, the heat spreader and silicon die (for the cylindrical voids study) was discretized using same DC3D6 element. The meshes shown in Figure 11(a) and 11(b) consists of a sum total 168,892 and 3,009,485 elements respectively.

2.4. Mesh-sensitivity studies

Mesh-sensitivity studies were carried out on two 0.20 mm thick STIM layers containing cylindrical and spherical shaped voids. The mesh density of each representative volume element (RVE) of the voided STIM was characterized by the total number of elements, N^e in the model. The higher the N^e, the finer the model and therefore the higher the mesh density. Six mesh densities of both the spherical and cylindrical shaped voids were created and analyzed. The thermal resistance from the source to the ambient, R_{sa}, was determined for all mesh densities.

Figure 12 shows the plot of thermal resistance obtained from the six mesh densities against the total number of element, N^e, in the model. It was observed that at $N^e = 31,000$ elements, the cylindrical-shaped voided STIM layer attained a mesh-indepdendent thermal resistance, while the spherical-shaped voided STIM layer converged to a mesh-independent thermal resistance at a much larger total number of elements, $N^e = 130,000$ elements. In subsequent studies, we have used a mesh density with total number of elements, $N^e \gg 150,000$ elements, to ensure that the density of the mesh does not influence our findings.

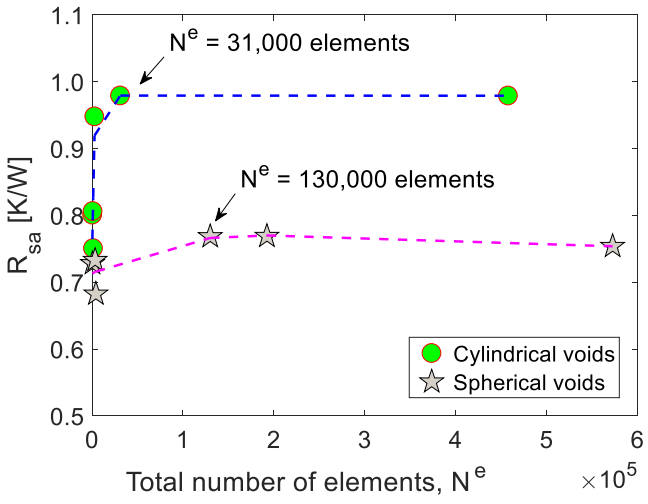


Figure 12: Mesh sensitivity studies for the cylindrical and spherical shaped voided STIM layer.

2.5. Transient analysis studies

The study adopted a transient analysis methodology for this study. Typical plots of the $Z-$axis heat flux, q_Z and temperature, T within the STIM layer during the test are shown

in Figure 13. For each simulation, the maximum, average and minimum heat fluxes were determined for the voided STIM layer only, as shown in Figures 13(a) and 13(a) for the cylindrical and spherical voids, respectively.

Similarly, the temperature profile for all elements in the voided STIM layer were determined. The maximum, T_{max}, and minimum, T_{min}, temperatures were determined, and the distribution of the temperature for all elements in the model are given in Figures 13(b) and 13(b) for the cylindrical and spherical voids, respectively. The number of elements in the spherical-void RVE is much higher than the cylindrical void morphology, as shown in Figure 13. The T_{max}, was on the side of the STIM layer nearest to the silicon chip and the T_{min} was obtained closest to the copper heat spreader. The average heat flux, $q_{z(average)}$, T_{max} and T_{min}, were used subsequently to calculate the numerically-determined thermal resistances, R_{sa}, according to Equation 4.

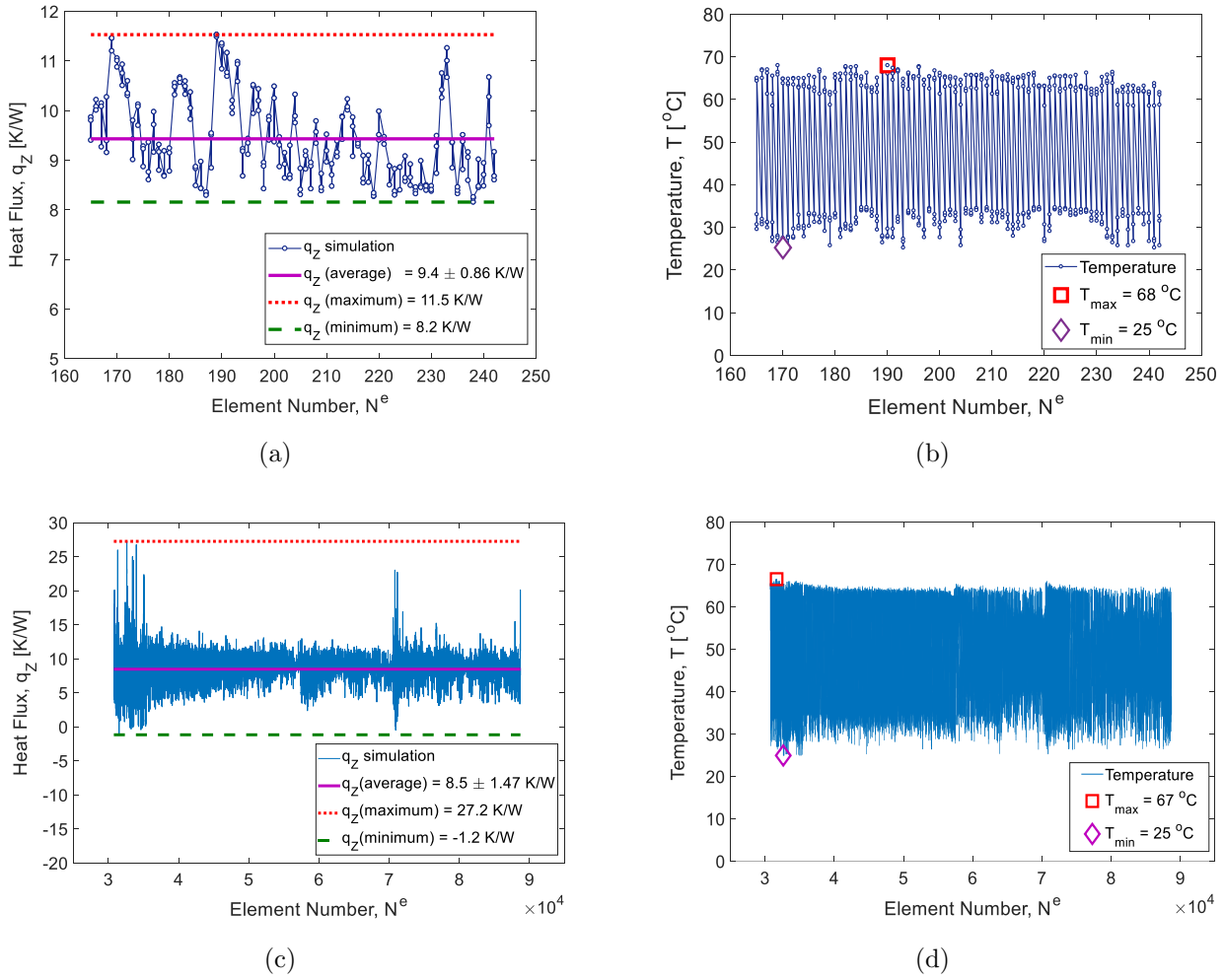
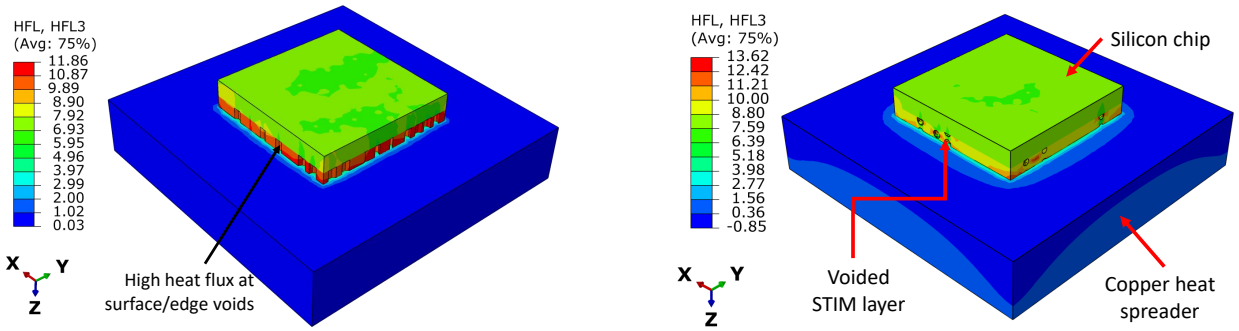


Figure 13: Typical distribution of STIM-layer only element-level model parameters, namely : (a) Z-axis heat flux per unit area, q_Z, and, (b) temperature, T (both for cylindrical void morphology). (c) Z-axis heat flux per unit area, q_Z, and, (d) temperature, T, (both for spherical void morphologies).

3. Results and discussions

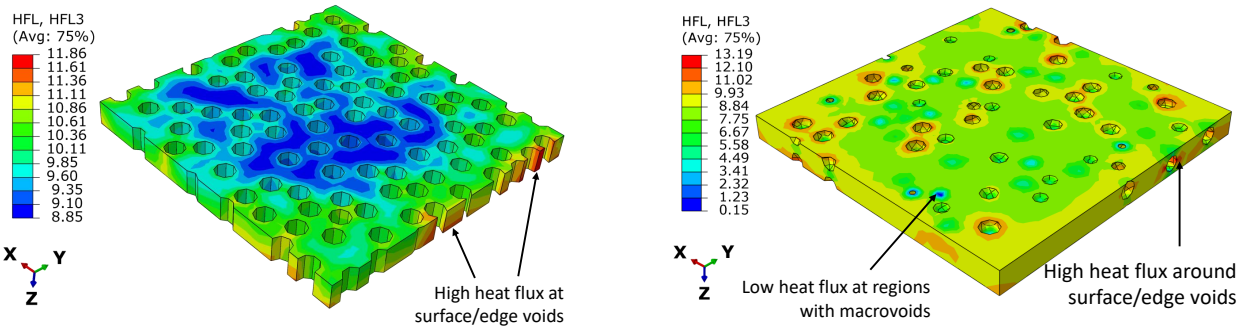
3.1. Full-scale model outputs

The full scale model simulations/outputs obtained from the two void morphology studies are shown in Figure 14. The STIM layer for both cases are 0.20 mm thick, but the void volume fractions for the cylindrical and spherical voids are 30% and 10% respectively. In order to understand the effect of the voids on the distribution of heat flux through the STIM layer, typical contour plots of $Z-$axes heat fluxes per unit area, through the voided STIM layer, for the two void shapes, are shown in Figure 15.



(a) (b)

Figure 14: Typical full CSP model simulation results showing the copper heat spreader, the STIM layer and the silicon chip where the STIM layer contains voids with (a) cylindrical, and, (b) spherical shapes.



(a) (b)

Figure 15: Typical contour plots of the heat flux on the STIM layer with: (a) cylindrical, and, (b) spherical void morphologies. Images show the heat flux (`HFL`) magnitude in the STIM layer.

The model outputs of Figure 14 show, as expected, that the voids in STIM influence the heat flux and consequently the thermal resistance of the CSP package. Quantitative data relating to this is discussed subsequently in Sections 3.2 and 3.3. The cylindrical voided STIM layer, for the thickness and void volume fraction considered in Figure 14(a), shows a higher heat flux (circa $q_Z = 11.86 W/mm^2$) than the heat fluxes in the silicon chip (circa

$q_Z = 5.95W/mm^2$) or the copper heat spreader (circa $q_Z = 0.03W/mm^2$). Similar observations apply for the voided STIM layer with spherical voids.

3.2. Comparison of analytical and numerical results

In order to validate model predictions, there is need for experimental data relating to this study. However, there is no experimental data in literature that assess the morphological features of the two types of voids studied in this work. The only comparison will depend on the analytical predictions using Equation 5 where the thermal conductivity of the voided STIM layer is determined based on Equation 6, such that the R_{sa}^{eff} parameter is equivalent to the numerically-determined R_{sa} of Equation 4. The comparison of analytical and numerical thermal resistances results are shown in Figure 16. The *Analytical CSP* profile is different from the *Analytical STIM* profile due to the thermal resistance contributions from the copper heat spreader and the silicon die.

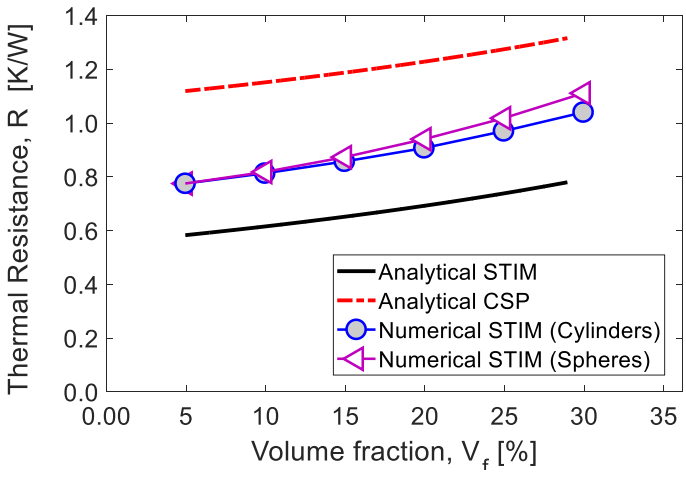


Figure 16: Comparison of thermal resistances determined by analytical and numerical methods for the STIM layer and the CSP package.

Figure 16 also shows the numerically-determined thermal resistances of the voided STIM layer only, with cylindrical and spherical void shapes. Qualitatively, the STIM-layer only analytical and numerical thermal resistances agree, having the same shape and dependence of thermal resistances on the STIM layer thickness and volume fractions. However, quantitatively, we notice a higher thermal resistance from the numerical study in comparison with the analytical predictions. This difference is in order of circa $0.20K/W$. We should note that the analytical derivations were obtained by assuming a linear heat conduction profile, with a single planar void, positioned directly along the heat conduction path. This is an idealistic case and does not account for features of the void morphology studied here. The contour plots of Figures 14 and 15 show a nonlinear distribution of heat flux, distorted significantly by the effects of the void morphology.

The above pieces of evidence help us conclude that the quantitative difference between the analytical and numerical thermal resistances of the STIM layer arise from the void mor-

phology variables of: three-dimensional void shapes, polydisperse void diameters, spatially random positioning of the voids and even surface/edge voids effects. Therefore, any realistic assessment of void effects in STIM layers must account for the influence of these variables in order to obtain a representative thermal resistance for the CSP package under investigation. This conclusion need to be confirmed by experimental data, based on consistently generated voids with dominant spherical or cylindrical morphology. At the time of writing, the authors did not find in literature any experimental data that is suitable for the type of study carried out here. An inspiration for future work in this area will be to generate such experimental data.

3.3. Effect of voided STIM layer thickness and void volume fraction

Simulations were carried out for various STIM layer thicknesses ranging from 0.04 mm to 0.20 mm for different volume fractions, from 5% to 30%. Figure 17 shows the comparison plots between the cylindrical and spherical shaped (randomly placed) voids within the STIM layer of dimensions given in Table 1.

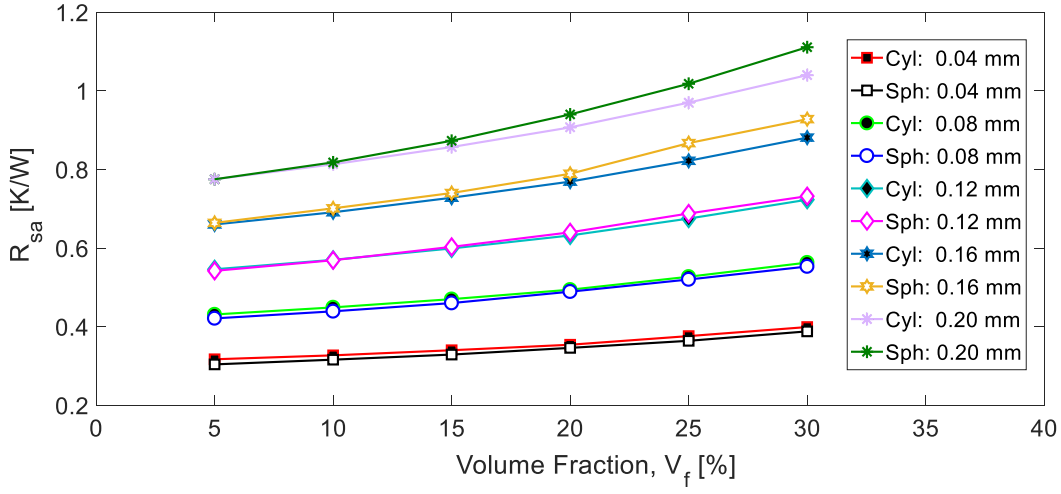


Figure 17: Comparison of effects of cylindrical and spherical voids on thermal resistance of the STIM layer for different thicknesses and volume fractions.

The results show the same dependence on thickness and volume fractions for both void shapes. As thickness of the STIM layer increases, so does the thermal resistance. Also, with increasing volume fractions, the thermal resistance of the STIM layer also increases. However, when considered more closely, there are slight quantitative differences between the thermal resistances for the cylindrical and spherical shapes.

For STIM layers with low void volume fraction, $V_f \leq 15\%$, both void shapes do not show significant difference in the numerically-determined thermal resistances. However, at large volume fractions, $V_f > 15\%$, the spherical voids gave the highest thermal resistances. The histogram of Figure 18 shows the comparative effect of STIM layer thicknesses and void volume fraction on the numerically-determined thermal resistances. For low void volume fractions and STIM layer thicknesses, $L_{STIM} \leq 80\mu m$, either the cylindrical or spherical

voids can be reliably used for investigating effect of void morphology on R_{sa}. However, at void volume fractions, $V_f > 15\%$ and STIM-layer thicknesses, $L_{STIM} > 80\mu m$, a spherical void type is recommended.

It should be noted here that this study is limited solely to a thermal analysis. The objective here was to highlight the influence of three-dimensional representation of void morphologies on thermal resistance of CSP packages. The findings here have shown there is an effect albeit it marginal for the sort of study carried out. It is our view that a more holistic study should be a thermo-mechanical study, with thermo-mechanical fatigue of STIM layer and industry-standard thermal cycling load histories included. Also, one will model the STIM using a viscoplastic model like the Anand model [40, 41] which will allow for mechanical failure of the STIM layer and thermal residual stresses accumulation: both factors seen in real components. For such a study, we will expect an appreciable difference between the spherical and cylindrical morphologies. This will be the inspiration for a future study.

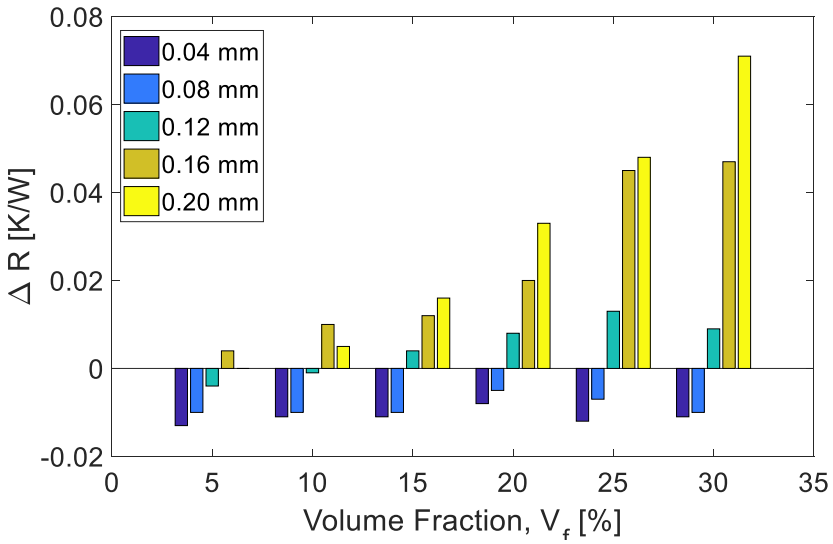


Figure 18: Difference in thermal resistance between cylindrical and spherical voids for different STIM layer thicknesses.

3.4. Effect of surface/edge voids

A consideration of the heat fluxes, shown in Figure 15, shows that for both the cylindrical and spherical voids, the spatial location of the voids influences the distribution of the heat flux and as a consequence the thermal resistance of the STIM layer. In particular, the cylindrical voids located near the surface or edges of the RVE of the STIM layer show a higher heat fluxes than those within the RVE. This is consistent with findings already by Otiaba *et al.* [15] and Le *et al.* [25] who both reported that edge/surface voids lead to higher thermal resistances. As a result, such edge/surface voids facilitate damage initiation of the solder and hence decrease the fatigue life of the solder joint. This implies that the sites with edge/surface voids are critical damage sites and so are susceptible to fatigue failure.

For the spherical voids, the distribution of the heat fluxes is nearly even although there exists regions where the heat fluxes are quite low. These tend to be in region around the large (macrovoids) as shown in Figure 19. As a result, the macrovoids block the linear path of the heat flux thus leading to reduction in the thermal conductivity of that area of the STIM layer. This is the evidence that supports findings by Yu *et al.* [24] which suggests that macrovoids reduce significantly the fatigue resistance of the voids. The microvoids of Figure 19 did not seem to cause an appreciable change in the heat flux hence the thermal resistance will be quite low in such regions. This observation is a critical influence arising from the void polydispersity of the STIM layer.

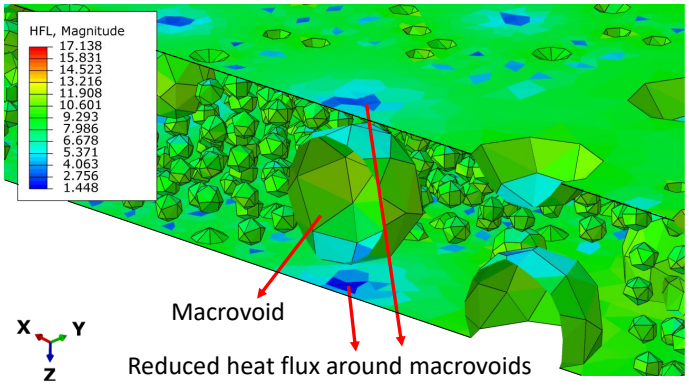


Figure 19: A sectioned view of STIM layer, showing a spherical macrovoid bounded by low heat fluxes (i.e. $q'' = 1.448W/mm^2$). The macrovoid causes a reduction in the thermal conduction through the STIM layer.

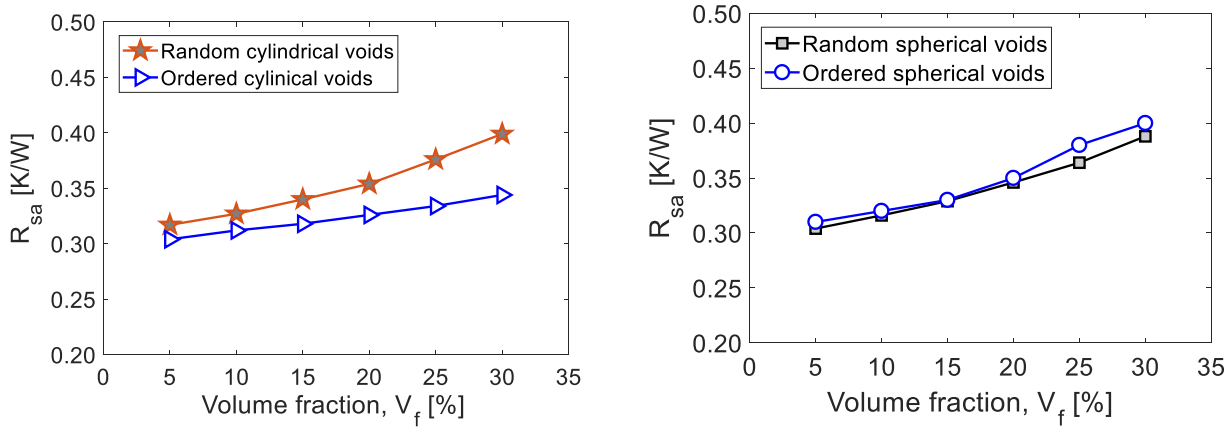
3.4.1. Effect of random versus ordered void arrangement

Some authors have considered the effect of void arrangements in thermo-mechanical response of the STIM layer [27, 28]. This study also investigated the effect of void arrangement for the two realistic void morphologies numerically generated in this work. The study was based on a 0.20 mm thick STIM layer and simulations were carried out for void fractions ranging from 5% to 30%. Figures 20(a) and 20(b) show the thermal resistance versus void volume fraction plots for the cylindrical and spherical void shapes respectively.

It can be seen that there is a clear difference between random and ordered arrangement for the cylindrical void shapes while there is no difference for the spherical void shapes. If one is to undertake a study of void morphology effects on thermal resistances using cylindrical void shapes, then the random void arrangement is recommended as this gave a higher thermal resistance. Consequently, care should be taken when electing for ordered arrangements as they generally gave lower thermal resistance predictions and they do not reflect the realistic void morphology of voided STIM layers. Contour plots for both void shapes are given in Figure 21.

3.5. Effect of void spatial realization

The influence of random spatial realizations of the voids (circular and spherical) were also considered in this study. Spatial realization refers to the random positioning of the voids



(a) (b)

Figure 20: Comparison of random versus ordered arrangement of voids in the STIM layer for : (a) cylindrical; and, (b) spherical void shapes.

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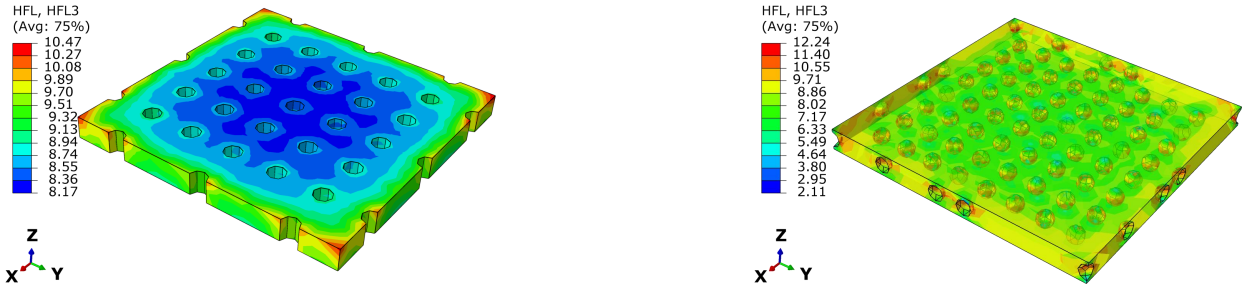

(a) (b)

Figure 21: The contour plot of the $z-$axis heat flux (HFL3) of voided STIM containing ordered arrangement of: (a) cylindrical; and, (b) spherical void shapes.

within the given RVE domain. Due to the random nature of the void generating algorithm, no two STIM layers are ever the same. It is therefore important to quantify if there is an effect on the thermal resistance by the random spatial realizations.

In this study, eight different spatial realizations of the STIM layer were generated for the same void volume fraction, RVE size, and same void generating method, as well as the same model boundary conditions. This ensured that the only variable in the model is the spatial positioning of the voids. The STIM is of size $2.5 \times 2.5 \times 0.20$ mm^3, with a void volume fraction, $V_f = 10\%$, and void diameter, $D_f = 150$ μm. The quantitative results from this study are reported in Figure 22 in the form of a histogram with each spatial realization identified by a numerical spatial realization index. The results show that the cylindrical shaped voids were least susceptible to spatial realization effects even though they gave a higher thermal resistance. However, the STIM layer with spherical voids were affected significantly by the spatial realization.

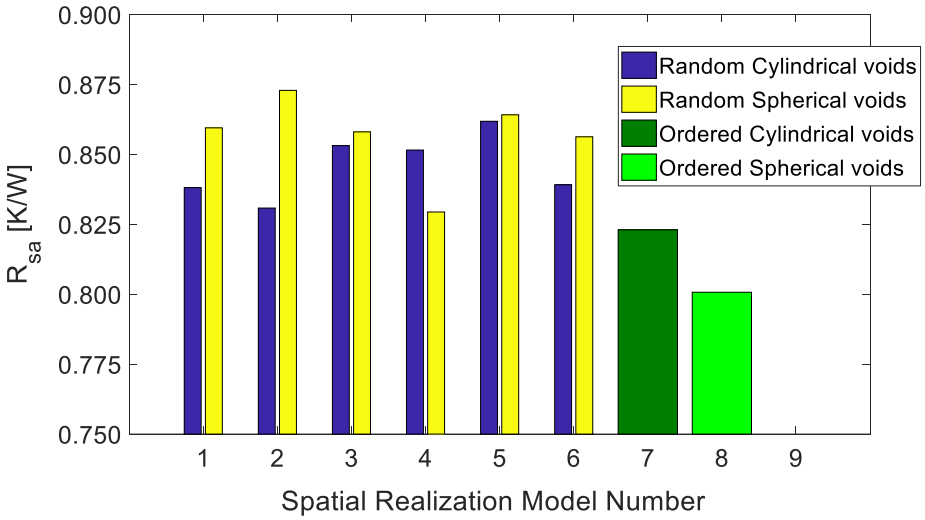

Figure 22: Comparison of influence of spatial realization on the thermal resistance of the STIM layer with cylindrical and spherical void morphologies.

These results can be explained since in the STIM layer with cylindrical voids, random positioning of the voids was only in the $XZ-$plane (see Figure 4). As a result, the flow of the heat flux along the $Y-$axis is not altered by the planar void positions. On the other hand, the STIM layer with spherical voids has a spatial positioning in all planes of the STIM layer. Consequently, the flow of the heat flux will be altered by the voids which will influence the thermal resistance. Evidence for the heat flux for only the STIM layer containing cylindrical and spherical voids, are shown in Figures 23 and 24 respectively. These contour plots show the heat flux variations within the voided STIM layer. The differences in heat flux map are solely due to the effect of spatial positioning/realization of the voids within the given STIM RVE. In order to ensure that an appropriate RVE for this type of study (with spherical voids) is isolated, larger RVE sizes would have to be chosen, which will not be susceptible to significant variations in thermal resistances due to the spatial realizations of the voids.

4. Conclusions

This paper has assessed the impact of three-dimensional void morphologies on the thermal resistance of Chip-scale packaged electronic devices. The void morphologies studies here consist of cylindrical and spherical shaped voids within a solder thermal interface material (STIM) layer. The voids are randomly distributed within the bulk of the STIM: a characteristic that is evident in real voided STIM. Since real voids show polydisperse void sizes, this study has considered polydisperse void shapes. Again, it is known in literature that macrovoids have detrimental effects on the thermal performance of electronic devices, therefore this study has focussed on void diameters in the range of $150\mu m$ and above.

The paper has shown two innovative numerical approaches for generating three-dimensional and realistic void morphologies. The has developed first approach (`MCRVEGEN2D`) is based on the Monte Carlo Hard core model, common in composite mechanics literature. Firstly, a planar spatial distribution of circles within a defined RVE is generated, and this is sub-

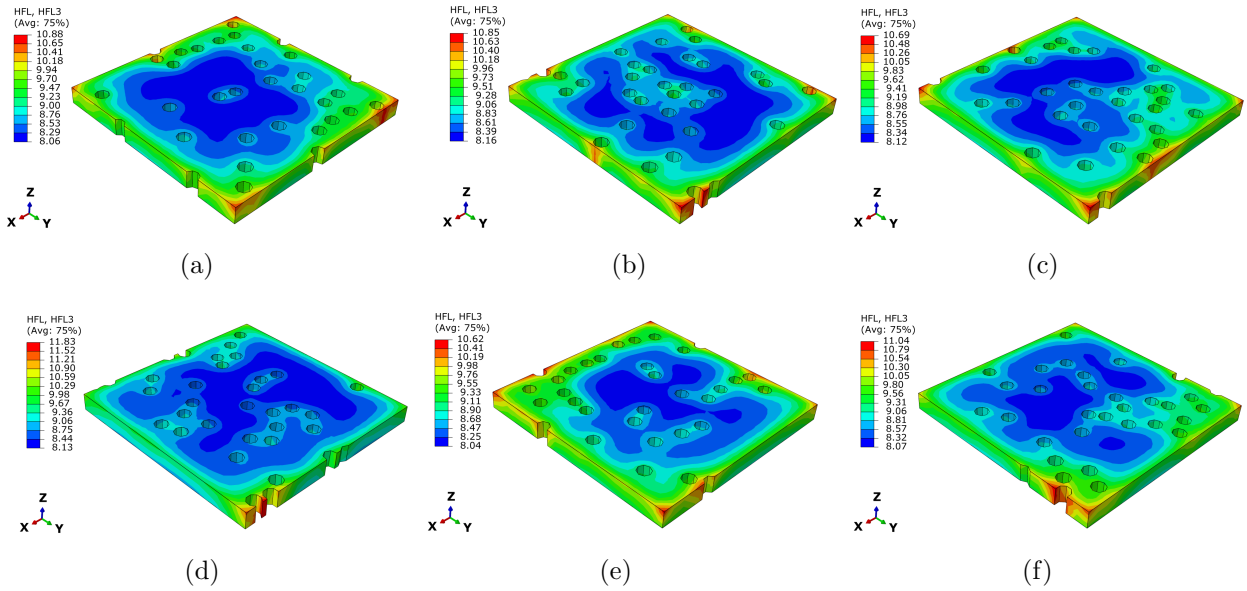

Figure 23: The effect of spatial realization on the distribution of $z-$axis heat flux (`HFL3`) of voided STIM containing cylindrical voids.

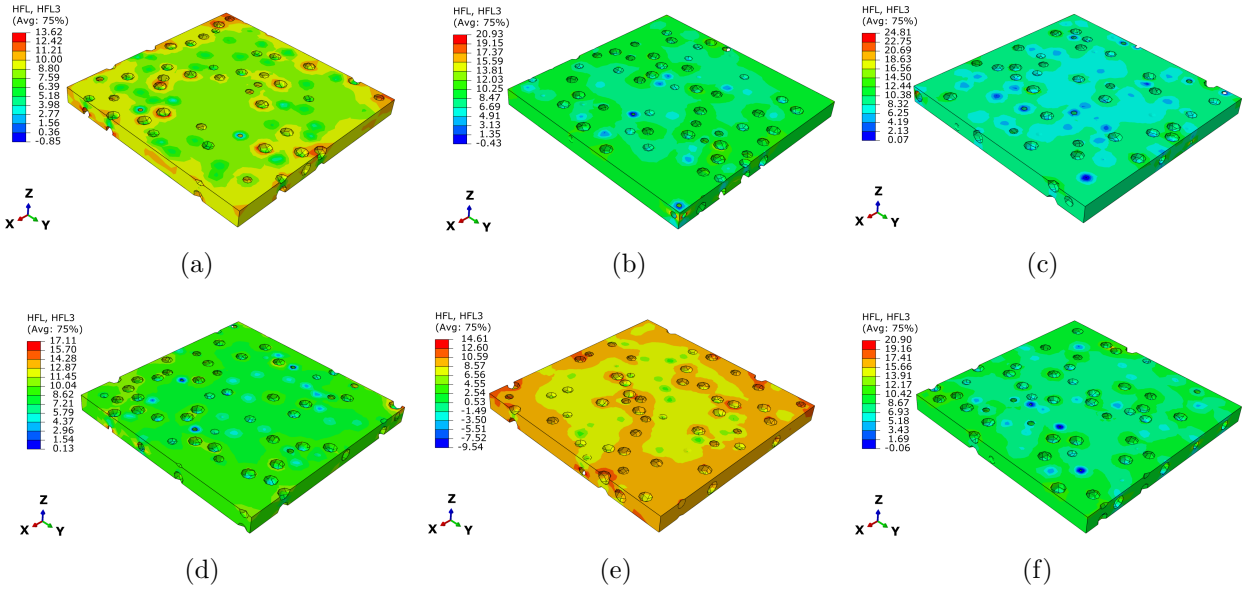

Figure 24: The effect of spatial realization on the distribution of $z-$axis heat flux (`HFL3`) of voided STIM containing spherical voids.

sequently extruded to create cylindrical shaped voids. The second method (*Voxel-method*) is based on a assembly of Voxel-type unit cells of voids of differing spatial positioning and diameters. The unit cells are assembled randomly to form Voxel elements which are subsequently combined, randomly to form the voided STIM. These numerically-generated voids can be created quite rapidly, making it computationally cheap for investigation of influence of void morphologies of STIM layers.

The study undertook a computational investigation of void morphologies of the STIM layer as regards the thermal performance of the complete CSP setup. The study found that both spherical and cylindrical shaped voids influence significantly the thermal resistance of the CSP assembly. At low void volume fraction or STIM layer thicknesses, there is minimal difference between describing the voids as either cylindrical or spherical shapes. However, at void volume fractions in order of 20% and above, or for thick STIM layers ($\backsim 160\mu m$), the void morphologies are best described using spherical voids.

The study compared analytical description of the dependence of thermal resistance on void volume fraction and STIM layer thickness. The study showed that analytical formulations (based on one-dimensional heat conduction theories) tend to under-estimate the effect of the void morphologies on the thermal performance of CSP packages. This was attributed to the fact that the one-dimensional considerations does not account for the multi-dimensional distortion of the heat flux map during the heat conduction from the chip heat source to the ambient. This distortion leads to reduction in the heat flow and hence a higher thermal resistance. Therefore, such investigations as this has paved a way for a realistic study of the holistic effect of void morphologies on the thermal resistance of the STIM layer and as a consequence the thermal performance of the CSP assembly.

The paper also investigated numerically the effect of random and ordered spatial positioning of the voids within the RVE window. This is because recent studies have assumed an ordered representation of voids when investigating void effects on thermal performance of STIM. The study showed that for a cylindrical representation of voids, there is a significant divergence between the ordered and random representation with the ordered representation giving a lower thermal resistance than the random representation. In principle, for the cylindrical void shapes, choosing an ordered spatial positioning of the voids will under-predict the thermal resistance hence susceptible to pre-mature failure for the components developed based on this information. However, for the spherical void shapes, we have shown that there is little difference between random and ordered representation. It is recommended that a spherical void pattern of random spatial positioning should be used for numerical studies as this.

Also, the study showed that the spatial distribution of voids within a defined RVE window is a significant consideration in assessing the effect of voids on thermal performance of CSP packages. This was the case for both the cylindrical or spherical shaped voids. It is essential that a representative volume element of the STIM layer, for the study should be generated which is not susceptible to signficant effects arising from spatial positioning of the voids within the RVE window.

The findings from this work will be significant for engineers working with micro-chip devices where government policies surrounding miniaturization of micro-chip packages have led to the need to improve the thermal performance of these devices. The approach presented here, in the view of the authors, is the first attempt at three-dimensional representation of voids within a computational scheme here, rather than relying on expensive, technically demanding computed tomography techniques of creating voided STIMs. Insights gained

from this work should drive further improvements in the electronics industry, with sustained improvement in the thermal performance of electronic devices.

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