Sintered Silver Finite Element Modelling and Reliability Based Design Optimisation in Power Electronic Module

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Abstract

This paper discusses the design for reliability of a sintered silver structure in a power electronic module based on the computational approach that composed of high fidelity analysis, reduced order modelling, numerical risk analysis, and optimisation. The methodology was demonstrated on sintered silver interconnect sandwiched between silicon carbide chip and copper substrate in a power electronic module. In particular, sintered silver reliability due to thermal fatigue material degradation is one of the main concerns. Thermo-mechanical behaviour of the power module sintered silver joint structure is simulated by finite element analysis for cyclic temperature loading profile in order to capture the strain distribution. The discussion was on methods for approximate reduced order modelling based on interpolation techniques using Kriging and radial basis functions. The reduced order modelling approach uses prediction data for the thermo-mechanical behaviour. The fatigue lifetime of the sintered silver interconnect and the warpage of the interconnect layer was particular interest in this study. The reduced order models were used for the analysis of the effect of design uncertainties on the reliability of the sintered silver layer. To assess the effect of uncertain design data, a method for estimating the variation of reliability related metrics namely Latin Hypercube sampling was utilised. The product capability indices are evaluated from the distributions fitted to the histogram resulting from Latin Hypercube sampling technique. A reliability based design optimisation was demonstrated using Particle Swarm Optimisation algorithm for constraint optimisation task consists of optimising two different characteristic performance metrics such as the thermo-mechanical plastic strain accumulation per cycle on the sintered layer and the thermally induced warpage.

Keywords: Reduced Order Models, Power electronic module, Risk Analysis, Particle swarm optimisation, Kriging, Radial basis.

1. Introduction

In a power electronic module, the silicon chip is attached by die attach materials usually solder materials to package substrate material. The package substrate is typically composed of ceramic isolated by copper layers. Nowadays silicon chips are replaced by silicon carbide chips which is able to withstand a temperature up to $500°$ C [1]. However die attach materials such as solders can't endure a temperature of above $200°$ C. Lead free solders such as SnAgCu has the melting temperature of $220°$ C. These lead free solders can be used as die attach material for up to 80% of the melting temperature before creep strain effects cause failure [1]. To enhance the thermo mechanical behaviour of die attach material, one of the approach is to use the sintered silver joint as die attach. Sintered silver joint has a high melting temperature, together with silicon carbide die is more suitable combination for high temperature application of power electronic module. The limitation of successful application of sintered silver interconnect is its long term reliability depends on the density of the sintered layer, types of substrates, substrate roughness, joint configuration (die sizes and interconnect thickness) formulation of sintered silver paste and other factors [2].

Experimental observations of power module with thin sintered silver layer (20 μm) as die attach material subject to thermal cyclic loading are listed below from the study by Herboth et al [3]

- Cracks initiated and propagated into interconnected network cracks
- Cracks penetrated through the sintered Ag layer nearly vertically

The observation concluded that primary failure mechanism of sintered layer was due to deformation by plasticity and the fracture mechanism in the sintered layer was intergranular fracture caused by the grain boundary porosity [3]. This observation motivated us to conduct a finite element analysis on sintered silver structural model in the hope of replicating these observations. Additionally this study is concluded with a reliability based design optimisation on sintered silver structure. Herboth's experimental observation in [3] was in contrast to the experimental observation discussed by DeVoto et al [4]. In DeVoto's article, it was reported that experimental observation of perimeter delamination of sintered silver layer as function of number of thermal cycles.

A review of the finite element modelling of sintered silver joint in power module applications are discussed in this paragraph. A 2D finite element modelling of sintered silver structure using Anand visco-plastic constitutive model to simulate the inelastic strain deformation is discussed by Chen et al [5]. Chen's article concluded that under thermal cycling conditions a ratcheting effect [6] of shear stress and strain in the sintered silver joint attached to chip. Another 2D FEA study on sintered silver structure for residual bending was simulated by Mei et al [7]. A simplified relationship for residual curvature versus joint size was also proposed with number of assumptions and FEA result was compared with experimental results [7]. In Herboth's article [3] a 3D FEA was conducted using a linear elastic fracture mechanics based crack initiation and propagation model and concluded that maximum stress intensity is related to diameter of the sintered silver joint for same substrate size. Another Herboth article [8] discusses a FEA on sintered layer structure and concluded that the cracks initiate at the edges of the die/sintered layer interface. Bai et al [9] simulated 3D FEA on sintered silver attached to silicon carbide chip and observed that thermo mechanical stresses are high on the perimeter of the interface.

2. Finite Element Analysis of Sintered silver in Power Module

In this section, the method and results of using finite element analysis computer modelling to investigate the effect of varying thermal load on the residual stress in the sintered silver layer are presented. To simulate the thermo mechanical loading condition on a sintered silver structure in Ansys FEA software [10] we generated the three dimensional finite element models as shown in Fig 1, Dimensions of the structure are indicated in Fig 1.
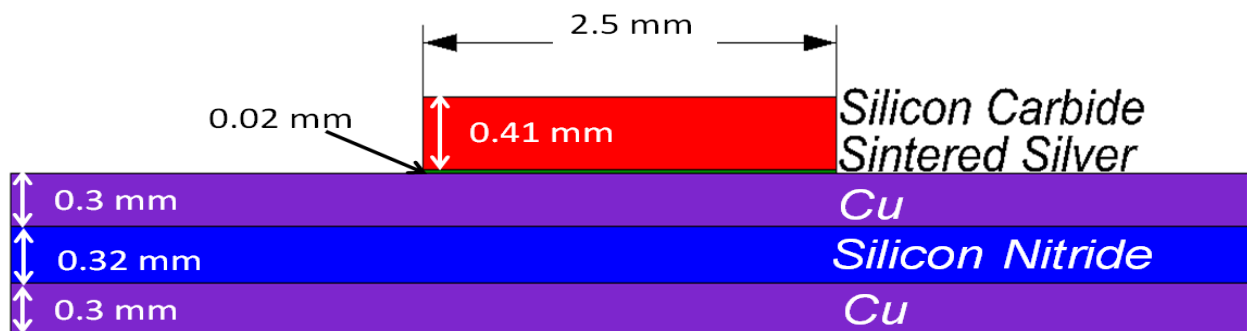

**Fig 1: The dimensions of the sintered silver finite element model**

The length and width of the silicon carbide chip is 2.5 mm × 2.5 mm and the silicon nitride length and width are chosen as 7.5 mm × 7.5 mm. The elastic and thermal material properties of all the materials used in this model are listed in Table 1 and plastic material properties are listed in Table 2. The material properties of sintered silver interconnect were obtained from the thesis by Bai [11]. Additional sintered silver material properties are extracted from the technical report by Wereszczak et al [12]. Fig 1 shows geometry and materials of the different layers. According to Dudek et al [13] the sintered silver shows elastic-plastic behaviour without the strong creep of soft solder up to the high temperature range (150° C). Additionally Chen et al [6] concluded from their experiment that the process of damage evolution of sintered silver interconnects was temperature independent. Hence we utilised elastic-plastic behaviour of the sinter layer instead of creep characteristic. Beside, creep data for the sintered layer was unavailable at the time of the study. In this study, FEA simulations in Ansys were a passive thermo mechanical analysis using the element SOLID185. The parts in the model associated with critical regions of interest have finer mesh in order to ensure accurate FEA results.

Table 1: Elastic and thermal material properties used in the FEA

Properties	Silicon Carbide (SiC)	Silicon Nitrate (Si₃N₄)	Copper (Cu)	Sintered Silver (80% dense)	Pure Silver
Thermal Conductivity (W/(K·m))	370	70	401	240	430
Specific Heat (J/(kg·°C))	750	691	390	234	234
Density (kg/cm^3)	3.21	2.40	8.96	8.4	10.492
Coefficient of Thermal Expansion (10^{-6}/K)	4.0	3.0	16.5	19	18.9
Young's Modulus (GPa)	410	314	128	10	83.5
Poisson Ratio	0.14	0.3	0.34	0.37	0.37

Table 2: Plastic material property used in the FEA

	Sintered Silver (80% dense)	Pure Silver
Yield Strength (Mpa)	43	55
Tangent Modulus (Mpa)	0	133
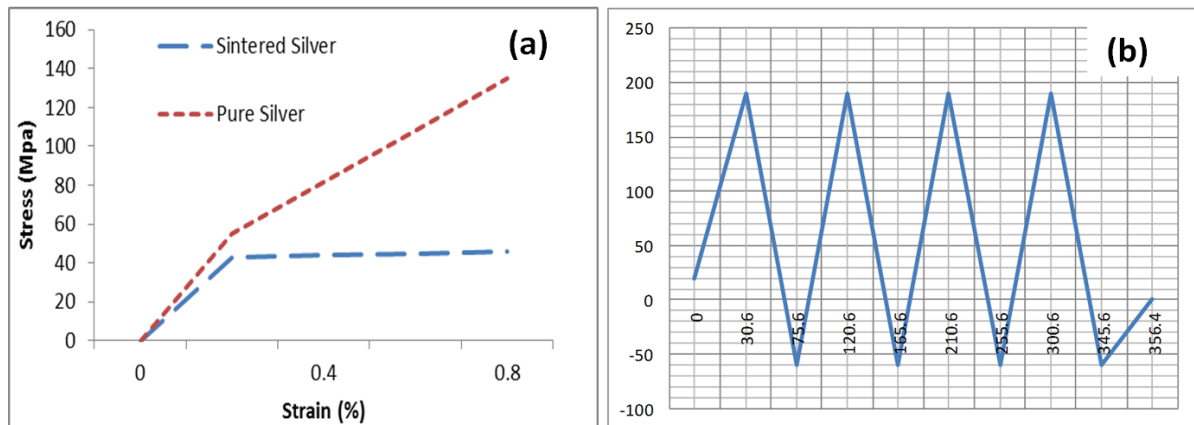
Fig 2. (a) Tensile stress versus strain plot of sintered silver and pure silver and (b) temperature cycling profile imposed on the finite element model.

The three point movement restraining boundary condition were imposed on the model. All three degrees of freedom at a lower point are fixed and then two degrees of freedom of the next lower point is fixed and one degree of freedom of the third lower point is fixed. Temperature cyclic loading as in Fig 2(b) is imposed on a passive thermo-mechanical analysis. Due to convergence issue with iterative solver in Ansys mechanical software, we utilised discreet static analysis using LOAD STEP option in all finite element simulations. The output extracted from the finite element simulation are accumulated plastic strain as in Fig 3 and relative displacement as in Fig 4. In Fig 4, the point A is the upper middle point of the sintered silver layer and point B is the lower middle point of the sintered layer. Relative displacement between point A and B is defined as

$$D_R = \sqrt{\left(u_A - u_B\right)^2 + \left(v_A - v_B\right)^2 + \left(w_A - w_B\right)^2}$$
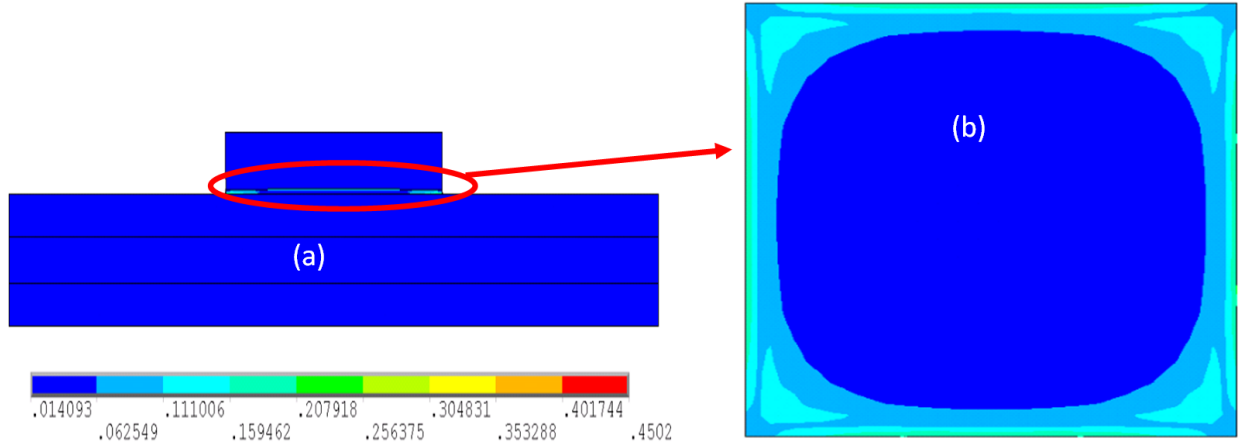
Fig 3. (a) Accumulated plastic strain distribution on the complete model and (b) Accumulated plastic strain of the sintered silver layer

The evaluation of predictive fatigue lifetime of solder joint can be categorised based on stress, plastic strain, plastic and creep strain, energy, and damage accumulation during a test [14]. For sintered silver interconnect with elasto plastic material properties we used a plastic strain based life prediction model which only considers plastic phenomena caused by coefficient of thermal expansion mismatch between various metals in the model. The Coffin-Manson fatigue life model one of the widely used model with the following equation were used in this study

$$N_f = C\left(\Delta\varepsilon_{pl}\right)^{-k}$$ (1)

where $\Delta\varepsilon_{pl}$ is the accumulated equivalent plastic strain during a stabilised cycle. This damage metrics were used for sintered silver layer fatigue life prediction. For the calculation of number of cycles before failure we used a sub volume (20 microns thickness) of the sintered silver layer which has the interface with silicon carbide. To calculate the accumulated plastic strain we used the volume weighted average (VWA) method which is widely reported in the literature. Maximum strain value at the corner was not chosen as damage metric to avoid the stress singularity issue of finite element modelling.

$$\Delta\varepsilon_{pl} = \frac{\sum_j \Delta\varepsilon_{pl}^j V_j}{V_{total}}$$ (2)

where V_{tot} is the summation of volumes of all the elements in the volume, V_j is the volume of the jth element and $\Delta\varepsilon_{pl}^j$ is the associated accumulated plastic strain. A study by Knoerr et al [1] for reliability assessment of sintered Nano silver die attachments for power semiconductors estimated the values of C and k in equation (1) as 0.16 and 2.96 respectively. This data set was used in the Coffin-Manson based relation of equation (1) to predict the cycles to failure for a specific cyclic loading profile.
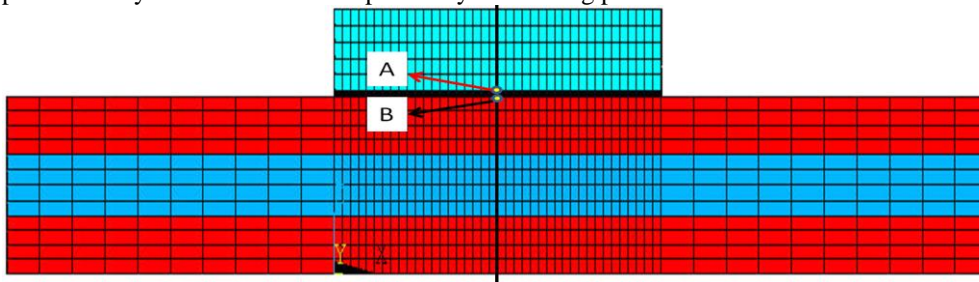

Fig 4: Relative displacement between the point A and B

One of the results from FEA simulation in ANSYS was the accumulated plastic strain (ANSYS command script output parameters for accumulated plastic strain is NL, EPEQ). A volume averaging technique described in equation (2) is then employed to calculate the accumulated plastic strain for 20 micron thick layer of sintered silver layer. In this study we used accumulated plastic strain as our response variable rather than number of cycles to failure

The influence of the sintered silver layer thicknesses on strain and stresses within the layer was analysed by changing the thickness of the sintered layer. Three thicknesses were chosen such as 20, 40, 60 microns and associated finite element models were simulated for the cyclic temperature loading profile of Fig 2(b). The accumulated plastic strain for third cycle (between 255 seconds and 345 seconds) was extracted and the strain distribution for these three simulations are as in Fig 5.
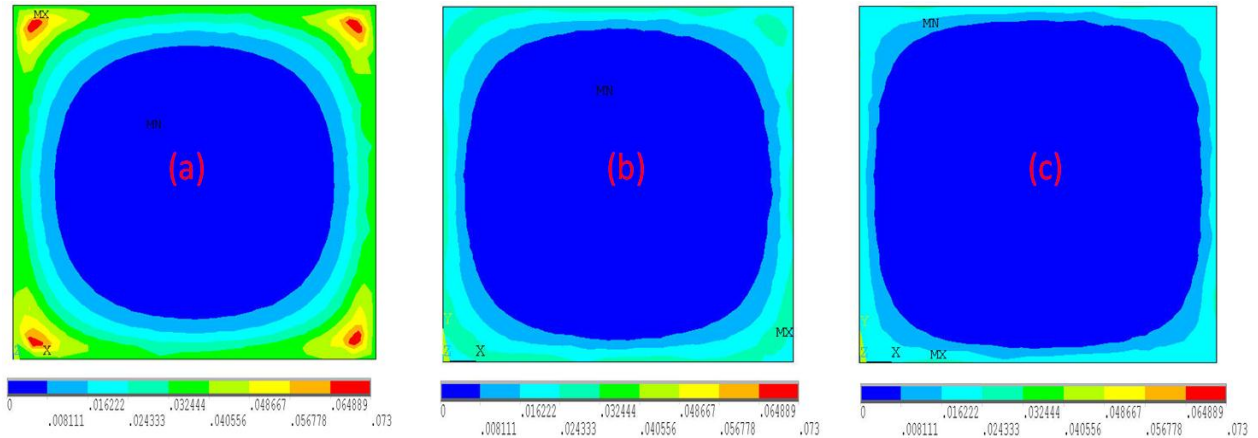

Fig 5: (a) accumulated plastic strain on 20 microns thickness layer, (b) accumulated plastic strain on 40 microns thickness layer, and (c) accumulated plastic strain on 60 microns thickness layer.

Accumulated average plastic strain at the third cycle for 20, 40, and 60 microns thickness sintered layer models are 0.0103, 0.0048, 0.0028 respectively, which implies that an increase in sintered silver layer thickness decreases the average plastic strain in the layer. Additionally accumulated plastic strain of the original 20 microns thickness layer was compared with the accumulated plastic strain of the same thickness layer with width and length are doubled and the resulting accumulative plastic strain values didn't have significant differences, hence the length and width of the model didn't influence the accumulated strain in the layer. Accumulated plastic strain distribution along the path from centre to the corner of the layer was exponential increment behaviour as in the Fig 6(b). This trend was also observed along the other paths (Fig 6(a)) as well. Increasing the thickness by 20 microns reduced the maximum stain distribution by 60 % in all paths on the sintered layer/copper interface at the last time step. In the sintered silver layer/ silicon carbide die interface increasing the sintered silver layer thickness from 20 microns to 40 reduced the maximum strain distribution of extreme points by roughly 60% and increasing the thickness of the sinter layer from 40 to 60 micron reduced the maximum strain distribution of extreme points by roughly 30%. This trend was also observed in other paths on this interface.
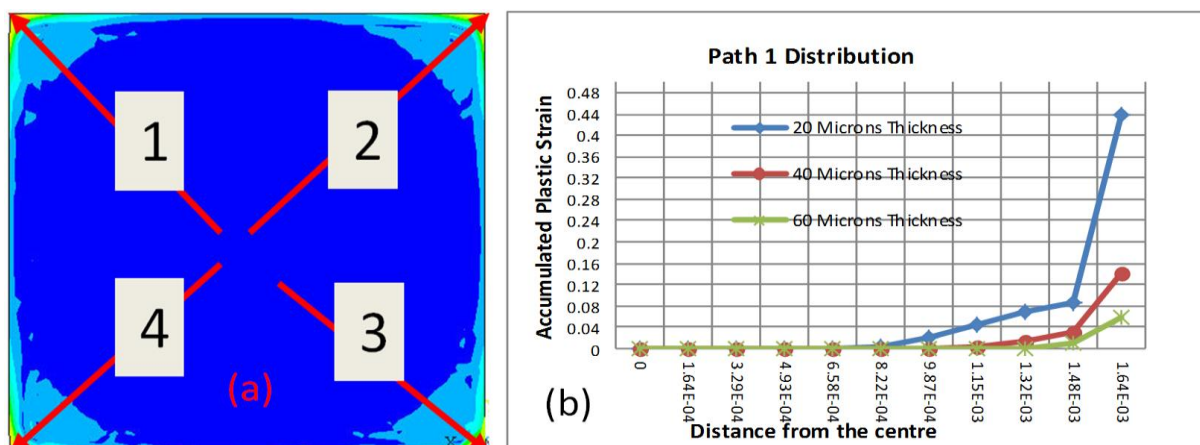

Fig 6: (a) The path numbering in the sintered silver layer, and (b) accumulated plastic strain distribution along the path 1 (from the centre to top left corner)
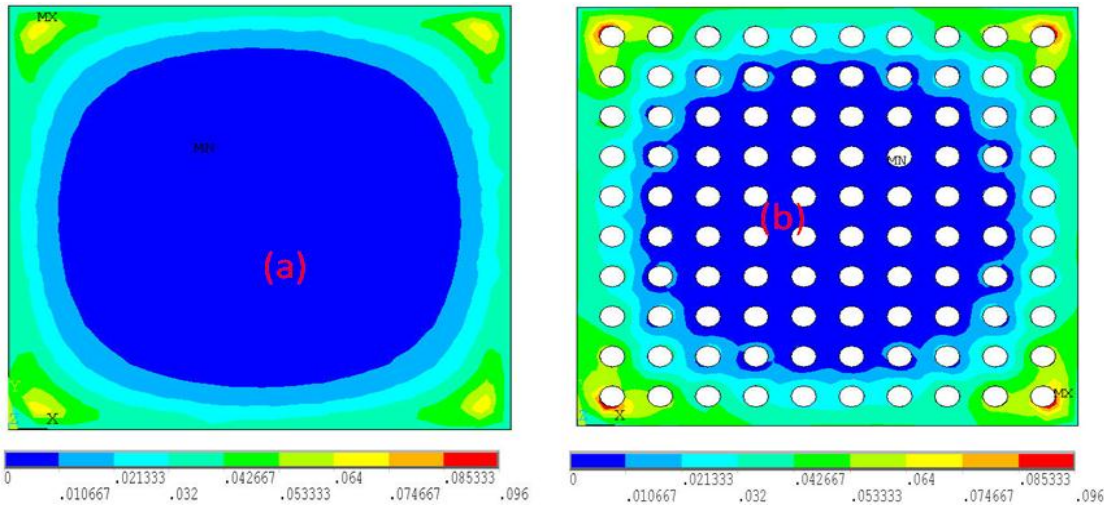
Fig 7: (a) Accumulated plastic strain on 20 micron thickness layer, and (b) Accumulated plastic strain on layer with cylindrical voids

In sintered silver layer with higher porosity, 80% dense sintered silver layer consists of 20 % void. One of the question arises is can these porosity cause any abnormally in the plastic strain distribution in the layer. A micromechanical finite element model was simulated by Dudek et al [13] to extract stress strain curve for various porosity rate. Replicating the voids in the full finite element model is computationally expensive, we employed a crude approximation in the finite element model by introducing 100 cylindrical shaped voids in the layer in order to observe change in strain distribution. These cylindrincal voids are equally distributed cylinders as in Fig 7(b). The remaining materials are assigned sintered silver materials property for consistency. Average plastic strain in both simulation (as in Fig 7(a) and Fig 7(b)) were closer values. The model with voids have increased maximum accumulated plastic strain on the path in comparison with the model without void. The increment percentage of maximum accumulated plastic strain were between 9% to 14%. Introduction of voids slightly altered the plastic strain distribution on the sinter layer along the path, but not very significantly as in the Fig 7(b). Hence the introduction of voids did not capture the porosity of the sintered silver layer in finite element model.

The plastic strain concentration and cracks are related [4]. Hence the concentration of plastic strain observed in the finite element model was on the perimeters of the interfaces as opposed to the observation of delamination appear everywhere in experiment caused by the porosity in the sintered silver layer. In the next section we proceed to conduct a reliability based design optimisation of sintered silver model subject to certain pre requirement.

3. Reduced order modelling by Data Interpolation Approach

The complexity of a system resulting from FEA simulation is generally influenced by two aspects: the complexity of the physics involved and the complexity of the model structural composition. An approach to reduce the computational complexity in number of FEA simulations is to replace it by a reduced order models. The reduced order modelling strategy presented here is based on interpolation and uses data obtained through Design of Experiment (DoE) based statistical methods. The DoE is a specific way of obtaining the design points within the design space. Various DoE strategies exist in the literatures. The reduced order models are developed as functions of the selected design parameters under consideration for investigation. In this study the discussions were on two interpolation-based models, Kriging and radial basis models. Kriging models incorporate the correlation between the design variables and both Kriging and RBF are popular models widely used in various disciplines. In microelectronics, Kim et al [15] has utilised these models for shape optimisation on heat sinks for micro-electronic cooling. The main objective of applying these reduced order models in this paper was to enhance a reliability based design optimisation. The ROM models were demonstrated for the sintered silver structure in power electronic module.

3.1. Design of Experiments

Table 3 lists the key assembly parameters of interest to be optimised for specific characteristic performances. The second column specifies the value of the nominal (or initial) design of the sintered silver model while third column of the table provides details on some possible design variations of the model assembly parameters that are selected for this study. The fourth column of the table is the normalised design parameter variations.

Table 3: Design parameters of the model

Sintered silver Model Design Variables	Nominal Values	Un-scaled limits	Scaled Limits/dimensionless
Silicon carbide chip Thickness(mm)	0.41	0.395 to 0.425	-1 to 1
Sintered silver Thickness(mm)	0.0275	0.02 to 0.035	-1 to 1

By altering the value of these design variables within the selected range, various design modification of the sintered silver model can be generated. A set of values for the specified design variables that specify a particular design is referred as a design point.

Table 4: DoE points and predicted sintered silver joint model responses from FEA

DoE Points No	Silicon Carbide Thickness (mm)		Sintered Layer Thickness (mm)		Accumulated Plastic Strain ($\times 10^{-3}$)	Relative Displacement D_w ($\times 10^{-7}$)
	Actual	Scaled	Actual	Scaled		
1	0.395	-1	0.02	-1	10.2938	1.0463
2	0.425	1	0.02	-1	11.0419	1.3718
3	0.395	-1	0.035	1	5.7191	1.8296
4	0.425	1	0.035	1	5.7763	1.8356
5	0.41	0	0.0275	0	7.4815	1.4401
6	0.41	0	0.02	-1	10.3231	1.0482
7	0.41	0	0.035	1	5.7461	1.8321
8	0.395	-1	0.0275	0	7.4535	1.4378
9	0.425	1	0.0275	0	7.5133	1.4431

The first step in the ROM approach is to obtain performance characteristic data through DoE by evaluation of a limited number of design FEA simulations. From a design point of view, any design modification of the sintered silver model was restricted to changing the Silicon carbide chip thickness (h_{CHIP}) and the sintered silver thickness (h_{SiAg}).

DoE methods were applied in the two-dimensional design space of the sintered silver model defined by the respective limits for the Silicon carbide chip thickness (0.395 mm to 0.425 mm) and the sintered silver layer thickness(0.02 mm to 0.035 mm). A two level full factorial design method was utilised to this design space to provide four design points. Additionally five points were derived through Box Behnhan DoE technique. From the nine design variables set nine FEA models were simulated. Increasing more DoE points increases the accuracy but it also increases the effort and computational cost in FEA model simulation. The DoE points are listed in Table 4. The table also shows the dimensionless scaled values of design variables over the range -1 to 1 used in the following generation of the reduced order models. The last two columns list the finite element analysis predictions for accumulated plastic strain on the sintered silver layer and relative displacement between point A and B in the model for each of the DoE points in the table. The value of accumulated plastic strain was then used in equation (2) to predict the mean life time to failure of the sintered silver structure. The ROMs were generated for the characteristic performances for the accumulated plastic strain and relative displacement in 10^{-7} meter, the last two columns of the Table 4.

3.2. Kriging Reduced order models

Kriging is a method of interpolation which predicts unknown performance data value or a particular point based on performance data already observed at known points. It minimises the error of predicted values which are estimated by distribution of observed data. Kriging response surface shows great promise for building accurate global approximation of design space. A Kriging model is defined as in equation (3)

$$\hat{y}(X) = \sum_{j=0}^{m} \beta_j P_j(X) + \sum_{i=1}^{n} \alpha_i r_i \qquad (3)$$

where X is the vector of the m design variables, $X= (x_1,..., x_m)$ and β_j $(j=0,...,m)$ are the coefficients of the polynomials $P_j(X)$ $(j=0,...,m)$. In equation 1, α_i $(i=1,...,n)$ are the coefficients of the basis functions r_i $(i=1,...,n)$ where n is the number of the DoE points. The polynomials $P_j(X)$ in this study are linear (i.e. $P_j(X)=x_j$, $j =1,...,m$ and $P_0(X)=1$).

The basis function $r_i = \varphi(\|X-X_i\|)$ is called a variogram and has as argument the absolute distance between points X and X_i. There are many variogram models available. In this work, the spherical model was utilised as it is suitable for cases with small number of design variables, typically when m≤3 [16]. If $h_i = \|X-X_i\|$ $(i=1,...,n)$, the spherical model is defined as:

$$\varphi(h_i)=\begin{cases} 0 & if \quad h_i = 0 \\ C_1\left(\dfrac{1.5h_i}{C_2}-0.5\dfrac{h_i^3}{C_2^3}\right) & if \quad 0 < h_i \le C_2 \\ C_1 & if \quad h_i > C_2 \end{cases} \tag{4}$$

where C_1 and C_2 are the variogram coefficients. The unknown coefficients in Kriging ROMs, β_j $(j=0,...,m)$, α_i $(i=1,...,n)$, C_1 and C_2 were computed so that the error of variation of the predicted and observed data is minimised [16].
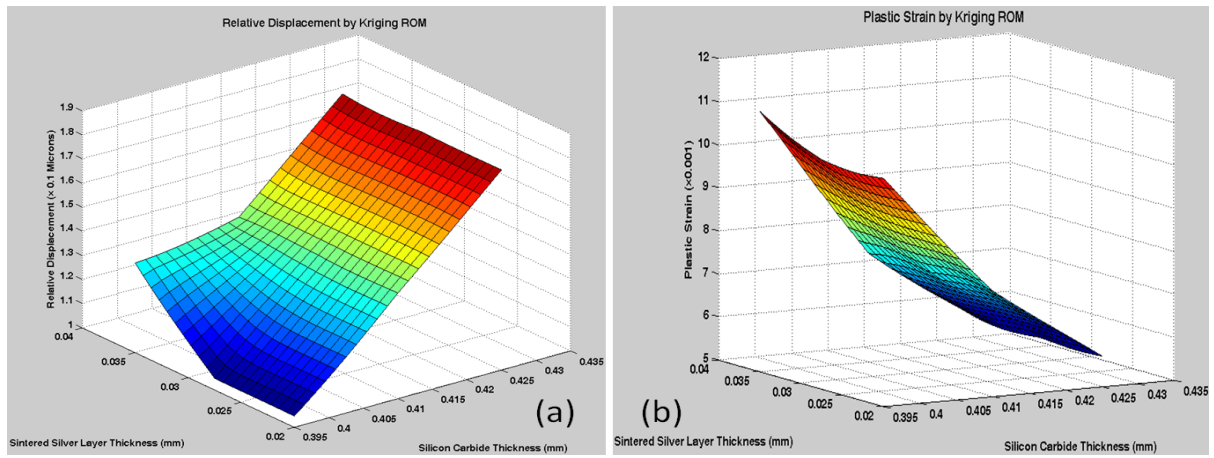

Fig 8: 3D plots of (a) relative displacement($\times 10^{-1}$μm) by Kriging ROM (equation (6)) and (b) plastic strain($\times 10^{-3}$) by Kriging ROM (equation (5))

The Kriging ROM, $K_{\varepsilon p}$, for the accumulated plastic strain ($\times 10^{-7}$) for two design variables silicon carbide chip thickness (h_{CHIP}), and sintered silver layer thickness (h_{SiAg}) on the subsection of sintered silver layer using the nine DoE points in Table 4 is defined as

$$K_{\varepsilon_p}\left(h_{CHIP},h_{SiAg}\right)=7.981+0.156*h_{CHIP}-2.415*h_{SiAg}+0.3523\sum_{i=1}^{9}a_i\left(\frac{1.5h_i}{1.708}-\frac{0.5h_i^3}{4.986}\right)$$

$$h_i=\sqrt{\left(h_{CHIP}-\left(h_{CHIP}\right)_i\right)^2+\left(h_{SiAg}-\left(h_{SiAg}\right)_i\right)^2} \tag{5}$$

The Kriging ROM for the maximum warpage ($\times 10^{-1}$μm) of the model using nine DoE points in Table 4 is defined as

$$K_{RD}\left(h_{CHIP},h_{SiAg}\right)=1.507+0.072*h_{CHIP}+0.032*h_{SiAg}+0.0211\sum_{i=1}^{9}a_i\left(\frac{1.5h_i}{2.828}-\frac{0.5h_i^3}{22.627}\right) \tag{6}$$

where h_i is as in (5). The 3D plots of two Kriging ROMs are in Fig 8(a) and 8(b).

3.3. Radial Basis Reduced order models

For a given data points and corresponding performance characteristic data a set of basis function is chosen in a way to form a linear combination of these set of basis to satisfy the interpolation condition. The interpolation condition generates a linear system of equation which determines the coefficients vector. If the data points are unique in the sense there are no duplication data point, many of the choices of basis functions produce non singular linear system matrix. For the higher dimensional data points above approach does not work. For higher

dimensional data points the approach is instead forming linear combination of set of basis functions that are independent of data points, ones forms a linear combinations of translates of single basis function that is symmetric about a centre. This approach is defined as radial basis method.

A response $y(x)$ in a domain that has a set of data points $\{x_i\}_{i=0,1,\cdots,n}$. The nodal response value is y_i at data points. Radial basis response surface constructs the reduced order model function to pass through all these training data points using radial basis function $\phi(\|x - x_j\|)$ and a polynomial $P(x)$

$$y(x) = \sum_{i=1}^{n} a_i \phi(\|x - x_i\|) + \sum_{j=1}^{m} b_j P_j(x) = B^T(x)a + P^T(x)b \tag{7}$$

Where a_i is the coefficient of $\phi(\|x - x_i\|)$ and b_j is the coefficient of the polynomial term P_j [17 and 18]. A radial basis function has the following general form

$\phi(\|x - x_j\|) = \phi(r_i)$ where r_i is the Euclidean distance between interpolation point x and x_i. Several types of radial basis function may be chosen for ϕ [17]. In this paper we used a Gaussian radial basis function $\phi(r) = e^{-\beta r^2}$ where Gaussian radial basis function is most commonly used with $\beta = 0.01$. Polynomial P is usually a lower order polynomial, in this paper we used a linear form. The reduced order models were implemented in our in-house software ROMARA [19] and utilised in this study. The radial basis reduced order model for the accumulated plastic strain ($\times 10^{-7}$) on sub section of volume of the sintered silver joint attached to the silicon carbide chip $R_{\varepsilon p}$ and warpage R_{Dw} ($\times 10^{-1}\mu m$) are in equation (8) and (9).

$$R_{\varepsilon_p}\left(h_{CHIP}, h_{SiAg}\right) = 220.983 + 5.811 * h_{CHIP} - 8.075 * h_{SiAg} + \sum_{i=1}^{9} a_i^{\varepsilon_p} e^{-0.01 h_i^2} \tag{8}$$

$$R_{RD}\left(h_{CHIP}, h_{SiAg}\right) = 92.805 + 2.708 * h_{CHIP} - 2.312 * h_{SiAg} + \sum_{i=1}^{9} a_i^{RD} e^{-0.01 h_i^2} \tag{9}$$

where i = 1,...,n (n = 13 DoE as in the Table 4), h_i is as in equation (5) and the values of the coefficients are listed in Table 5.

Table 5: Coefficients for Kriging and radial basis function models

Sintered Silver model DoE scaled value		Coefficients of Reduced order models			
		Kriging		Radial Basis	
$(h_{CHIP})_i$	$(h_{SiAg})_i$	$a_i^{\varepsilon p}$	a_i^{RD}	$a_i^{\varepsilon p}$	a_i^{RD}
-1	-1	-0.5615	-0.1029	1012396.76	463619.7
1	-1	-2.0032	-17.2539	1027438.87	470657.99
-1	1	-1.0807	-2.6978	997791.07	456793.54
1	1	-0.5611	-0.1075	1012383.8	463624.02
0	0	0.8488	-0.8926	3988255.15	1827058.46
0	-1	0.4469	12.554	-2023693.9	-927368.87
0	1	-0.4759	-1.9976	-1994033.14	-913508.74
-1	0	1.2323	-2.0312	-1995451.9	-913503.66
1	0	2.1544	12.5295	-2025086.72	-927372.43

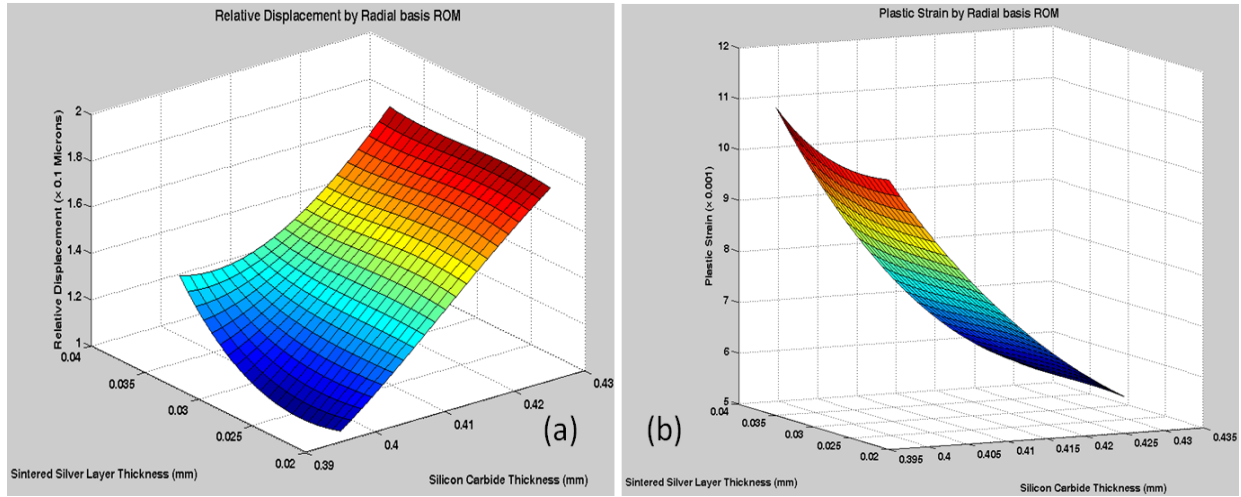The 3D plots of two radial basis ROMs are in Fig 9(a) and 9(b).

Fig 9: 3D plots of (a) relative displacement ($\times 10^{-1}$ µm) by Radial basis ROM (equation 9) and (b) plastic strain($\times 10^{-3}$) by Radial basis ROM (equation 8)

4. Sintered Silver model Uncertainty and Product Capability Analysis

In microelectronics products and systems, it is important to gain the information about the impact of design variables and manufacturing uncertainties on the performance characteristic and to assess if key product characteristics fall outside acceptable specification limits. This would typically require an evaluation of the actual variation distribution of the performance characteristic parameters of interest. These distributions of performance characteristic can then be utilised for the purpose of capability calculations and risk mitigation. The techniques for probabilistic distribution estimation discussed here involve of sampling based technique namely Latin Hypercube sampling (LHS)

LHS is a stratified sampling scheme developed by McKay et al [20]. It uses a technique known as 'stratified sampling without replacements', see as described in [21]. For a model Y that is a function of other variables $x_1, x_2, …, x_n$. This method selects M different values from each n random variable using the following method. The probability distribution of each n random variable $x_1, x_2, …, x_n$ is split into M non overlapping intervals based on an equal probability of occurrence. One value from each interval is selected at random with respect to the probability density in the interval. The M sample values obtained for x_1 are paired in a random manner with the M values of x_2. These M pairs are then paired in a random manner with the M values of x_3 to form M triplets, and so on, until M by n tuples are formed. The next step involves the generation of M samples from M by n tuples. The response function is computed from M randomly permuted samples in all samples provided no two samples have any input corresponding to the same interval. The advantage of this method is that random samples are generated from all the ranges of possible values; therefore it extracts information for the tails of the probability distribution.

LHS simulation based distribution estimation technique was utilised for the process or product variable distribution and a histogram was obtained. Fitting a distribution to this histogram is essential for product capability index calculation if the underlying distribution follow a non normal format. The Silicon carbide chip thickness and sintered silver layer thickness in the model were assumed to follow normal Gaussian distributions with standard deviations of 1.2 µm, and 0.6 µm respectively. Nominal Silicon carbide chip thickness was assumed as 0.41 mm and nominal sintered silver layer thickness was assumed as 0.0275 mm. The predictions for the plastic strain and relative displacement probability distribution from Latin Hypercube for the nominal design case of the Silicon carbide chip thickness (h_{CHIP} = 41 mm, and sintered silver layer thickness (h_{SiAg} = 0.0275 mm) are shown in Figure 10 to 13. The values for the sintered silver model responses of interest were obtained using the Kriging and radial basis reduced order models.

In practice microelectronic systems process or product variable distributions, in most situations follow a non normal distribution for which the product capability indices calculations need to be evaluated. There are several statistical measurements available to measure the capability of the process or product namely C_{np}, C_{npk}, C_{npm}, C_{npu}, and C_{npl}. The terminology used in product capability analysis such as LSL, USL, T means the lower specification limit, upper specification limit and target value respectively. The product capability indices of the product or process variable for a non normal distributions are defined as [22, 23]:

$$C_{np} = \frac{USL - LSL}{p(0.99865) - p(0.00135)}$$

$$C_{npk} = \min\left[\frac{USL - p(0.5)}{p(0.99865) - p(0.5)}, \frac{p(0.5) - LSL}{p(0.5) - p(0.00135)}\right]$$

$$C_{npm} = \frac{\min\left(USL - p(0.5),\ p(0.5) - LSL\right)}{\sqrt[3]{\left(\frac{p(0.99865) - p(0.00135)}{6}\right)^2 + \left(p(0.5) - T\right)^2}}$$

where p(0.99865), p(0.00135), and p(0.5) are the 99.865[th] percentile, 50th percentile and 0.135[th] percentile of the underlying distribution respectively. In this study, the values of LSL, USL for the plastic strain were assumed as 6.9×10^{-3} and 8.1×10^{-3} respectively. Similarly LSL and USL for relative displacement were assumed as 0.134 and 0.155 microns respectively. For product capability analysis, the histogram data was skewed (non-symmetric), we fitted some non-normal distributions to the histogram data. Weibull distribution was fitted to the histogram resulting from LHS. The probability density function and cumulative density function of two parameter Weibull distribution are defined as equation (10) and (11):

$$f(x) = \left(\frac{\beta x^{\beta - 1}}{\alpha^\beta}\right) e^{-\left(\frac{x}{\alpha}\right)^\beta} \tag{10}$$

$$F(x) = 1 - e^{-\left(\frac{x}{\alpha}\right)^\beta}, \quad x \geq 0 \tag{11}$$

where α is the scale parameter which is the characteristic value of the distribution, such as time to failure when considering this distribution to describe the life time of materials under fatigue and fracture loads. The shape parameter β of Weibull distribution controls the width of the frequency. Statistical software Minitab [24] was utilised in this study. The histogram and fitted Weibull distributions on cumulative distribution histogram generated in Minitab are on Fig 10 – 13.
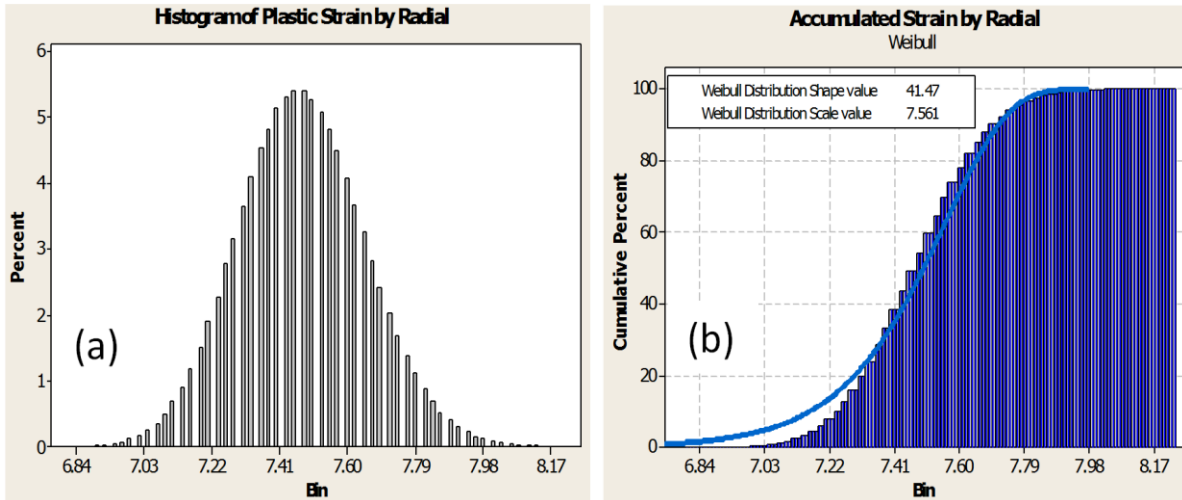

Fig 10: (a) Histogram of plastic strain (× 0.001) distribution by Radial basis model (b) Weibull distribution fitted to cumulative distribution of histogram by Radial basis model
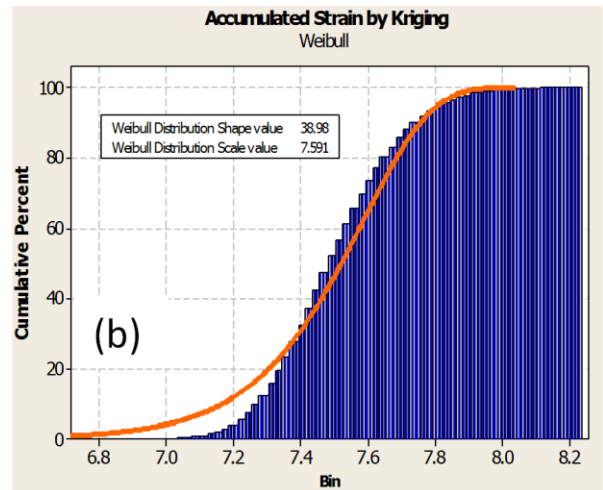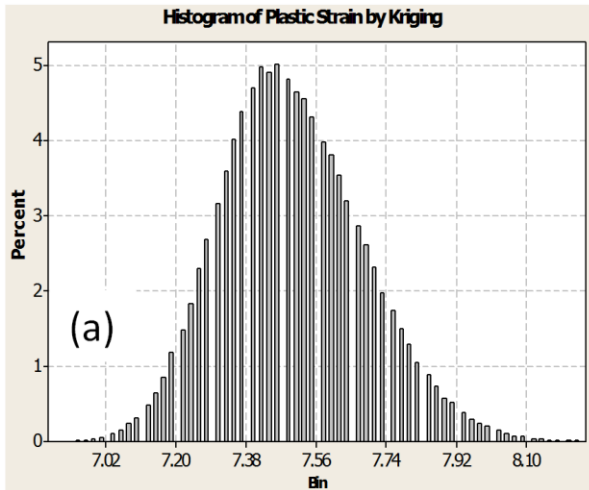
Fig 11: (a) Histogram of plastic strain (× 0.001) distribution by Kriging (b) Weibull distribution fitted to cumulative distribution of histogram by Kriging

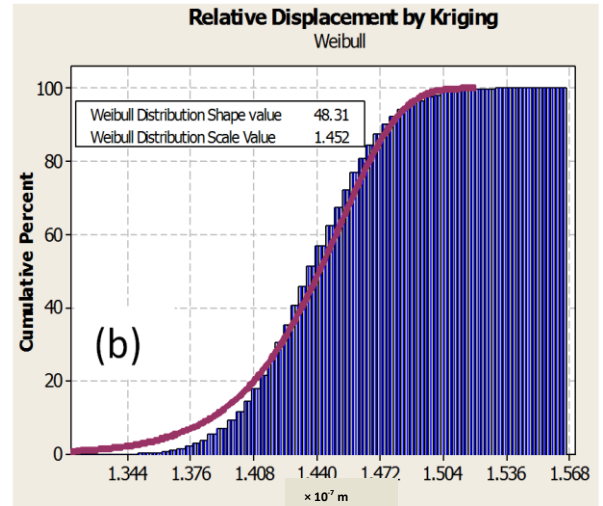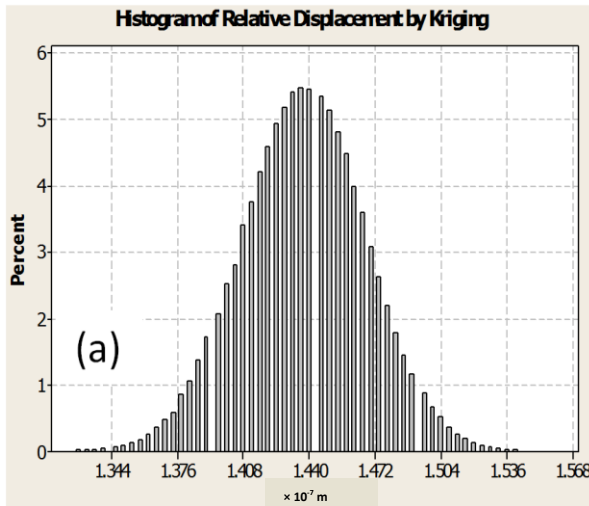**Fig 12: (a) Histogram of relative displacement (× 10^{-1} μm) distribution by Kriging (b) Weibull distribution fitted to cumulative distribution of histogram by Kriging**

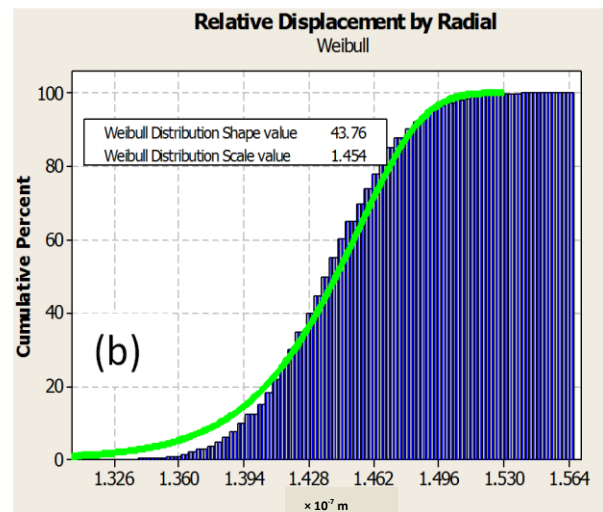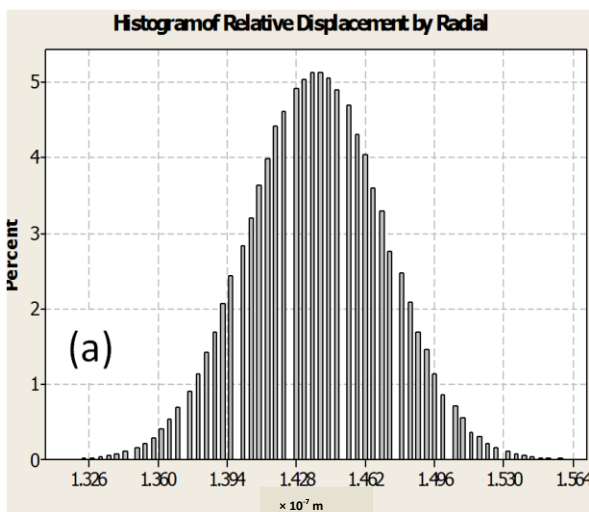**Fig 13: (a) Histogram of relative displacement(× 10^{-1} μm) distribution by radial basis model (b) Weibull distribution fitted to cumulative distribution of histogram by radial basis model**

Table 6: Mean and Standard deviation of various reduced order models, the data of various fitted distributions to histogram and product capability indices values

		Plastic Strain(×0.001)by Kriging	Plastic Strain(×0.001) by Radial basis	Relative Displacement (×10⁻¹ µm) by Kriging	Relative Displacement (×10⁻¹ µm) by Radial basis
LHS simulation	Mean	7.511	7.485	1.439	1.440
	Standard Deviation	0.1842	0.1787	0.0303	0.0335
Weibull Distribution Fitting to Histogram	Scale value	7.591	7.561	1.452	1.454
	Shape value	38.98	41.47	48.31	43.76
Lognormal Distribution fitting to histogram	Location value	2.015	2.011	0.3626	0.3629
	Scale value	0.0245	0.0239	0.0211	0.0233
Gamma Distribution fitting to histogram	Shape value	1670	1750	2248	1842
	Scale value	0.0045	0.0043	0.0006	0.0008
Logistic Distribution fitting to histogram	Location value	7.493	7.471	1.437	1.438
	Scale value	0.105	0.1022	0.0173	0.0192
Loglogistic Distribution fitting to histogram	Location value	2.014	2.011	0.363	0.363
	Scale value	0.014	0.0137	0.0121	0.0133
C_{np} (Weibull)		0.769	0.819	0.862	0.784
C_{np} (Lognormal)		1.087	1.119	1.153	1.044
C_{np} (Gamma)		1.09	1.12	1.155	1.045
C_{np} (Logistic)		0.865	0.889	0.917	0.83
C_{np} (Loglogistic)		0.866	0.888	0.916	0.828
C_{npk} (Weibull)		0.557	0.568	0.579	0.532
C_{npk} (Lognormal)		1.048	1.104	1.101	1.005
C_{npk} (Gamma)		1.066	1.092	1.089	0.991
C_{npk} (Logistic)		0.855	0.846	0.847	0.774
C_{npk} (Loglogistic)		0.837	0.885	0.884	0.806

From the product capability indices values of C_{np} and C_{npk} based on fitted distributions on Table 6, we can observe that the values of C_{np} and C_{npk} for most models based on lognormal and gamma distribution are greater than one. The numerical values of C_{np} and C_{npk} are greater than one means the product or process is capable, i.e. failure rate is below an acceptable tolerance value. To identify the best distribution that the data follows in all models, we applied Anderson Darling statistic test (AD). Lower AD values indicate a better distribution fit to the histogram. With a confidence interval of 95%, the best fitted distribution with lower AD value is Gamma distribution as in Fig 14. Hence the product capability indices C_{np}, C_{npk} were in acceptable range for the specified requirements since the the values of C_{np}, C_{npk} generated from the Gamma distribution are above one.
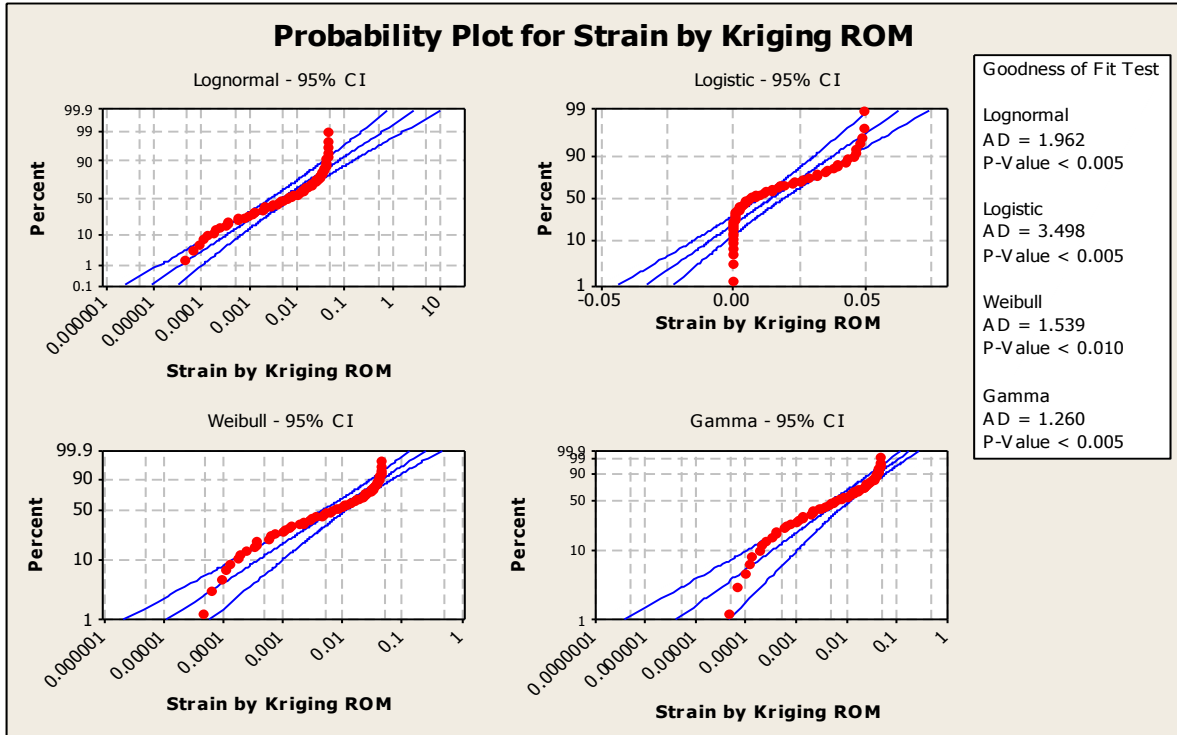
Fig 14: Anderson Darling (AD) values of lognormal, logistic, Weibull and gamma distributions for 95 % confidence interval

5. Sintered silver model Design Optimisation

The design optimisation task is to evaluate the optimal sintered silver structure for which the relative displacement of the model is minimised while satisfying a requirement that the maximum plastic strain in the sintered silver model does not exceed an upper limit (a value of 11.01×10^{-3}, I.e. no lower than 100000 mean fatigue life cycles by Coffin Manson fatigue parameters of [1]). The design modifications were restricted to changes of the two design variables within the limit values. In this study, a design for the height of the silicon carbide chip and the height of the sintered silver layer are defined as optimal if it satisfies all defined constraints. The variation of the design variables followed Gaussian distribution with mean values are the nominal values. The following standard deviations specify the uncertainty of the sintered silver model design variables. The silicon carbide thickness (h_{CHIP}) and sintered silver layer thickness ($h_{Sintered}$) as 1.2 μm, and 0.6 μm respectively.

The uncertainty properties of the characteristic performances are usually unknown. Therefore, when uncertainties are included in the design optimisation task, we need to estimate the random properties of the responses or performance characteristic. In the section (4) we introduced Latin Hypercube sampling for estimating the distribution of a response model. This sampling method was utilised to obtain the information for uncertainty properties of response model and by using this information, we predicted the probability of failure with respect to the performance characteristic. In the reliability based optimisation the main objective was to accommodate the variations of the performance characteristic (response) that define the reliable design domain and to enforce the deterministic optimal solution is moved from the boundary of the active constraints inside the feasible domain. Therefore, the objective was to minimise and satisfy constraints that includes the system responses and the related probability of failure. This reliable optimum design is called a probabilistic or reliable optimum. To define the probabilistic optimum one must specify what probability of failure will be acceptable. To further clarify the reliability based design optimisation strategy, the following formulation of the design problem below was given. In this strategy when minimising an objective function, reliability constraints condition also need to be satisfied in the optimisation task.

Find values of h_{CHIP} and h_{SiAg} that

<u>*Minimise*</u> R_{RD} (12)

<u>*Subject to*</u>

       (c1) Probability of failure (Upper Specification Limit of $R_{\varepsilon p} < 11.01 \times 10^{-3}) < 0.05$

       (c2) $0.395 \leq h_{CHIP} \leq 0.425$ mm

          Standard deviation (σ) h_{CHIP} = 1.2 μm

       (c3) 0.02 mm $\leq h_{SiAg} \leq 0.035$ mm

Standard deviation (σ) h_{SiAg} = 6 µm

The solution of this optimisation problem will account for the variation of the input design variables (the constraints (c1) –(c3)). The constraint (c1) states that the probability of the plastic strain being less than or equal to 11.01×10^{-3} must be no greater than 0.05 (i.e. 5% probability of failure limit with respect to the plastic strain requirement) as in the Fig 15.

Similarly the constraint (c2) and (c3) are the bounds of the design variables. In a similar way for the reliability based design optimisation strategy, Optimisation task (13) is same except the ROM used in this scenario is Kriging ROM rather than radial basis ROM as in previous optimisation task (12). The above optimisation problems are defined and solved using VisualDOC [25]. The optimisation task was solved using particle swarm algorithm (PSO). The PSO scheme is based on a simplified social model that is originated from the swarming theory [26]. The scheme for updating the position of each particle is shown as

$$x_{k+1}^i = x_k^i + v_{k+1}^i \Delta t$$

Where the x_{k+1}^i represents the position of the particle i at iteration $k+1$ and v_{k+1}^i represents the corresponding velocity vector defined as

$$v_{k+1}^i = w * v_k^i + c_1 r_1 \frac{\left(p^i - x_k^i\right)}{\Delta t} + c_2 r_2 \frac{\left(p_k^g - x_k^i\right)}{\Delta t}$$ where r_1 and r_2 are random numbers between 0 and 1, p_i

is the best position found by particle i so far and p_k^g is the best position in the swarm at time k. In this study, the constants w, c_1, and c_2 are defined as 1.4, 1.5, and 2.5 respectively. The 10,000 Latin Hyper cube sampling was generated at each iteration step for probability of failure distribution prediction. In both cases PSO technique converges to identify the global optimal solutions (within the algorithm tolerances) within few number of iteration as in Fig 16. The optimal results are listed in Table 7 [25].
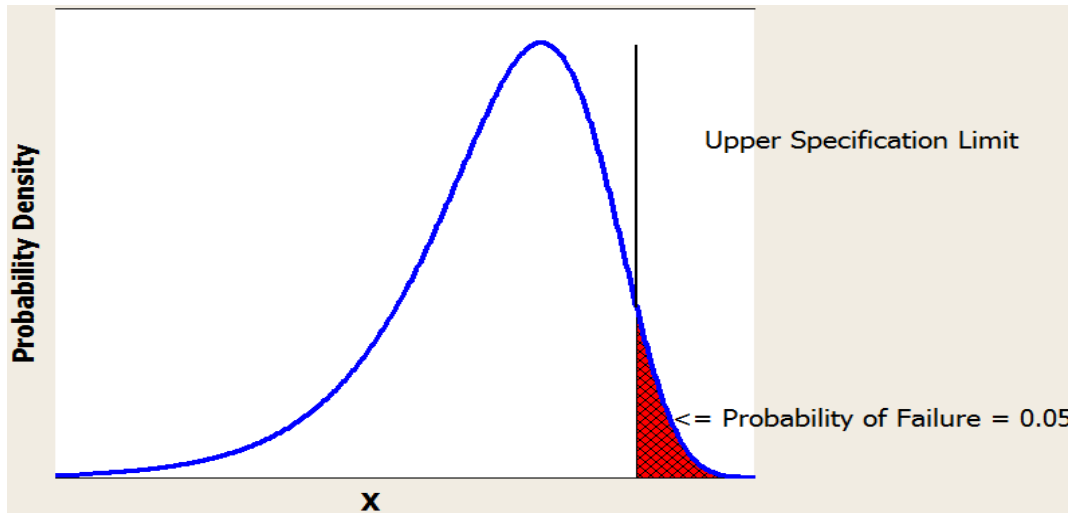

Fig 15: picture of probability of failure constraint (c1) in the optimisation task.

Table 7: PSO Optimisation results of the optimisation task (12) and (13)

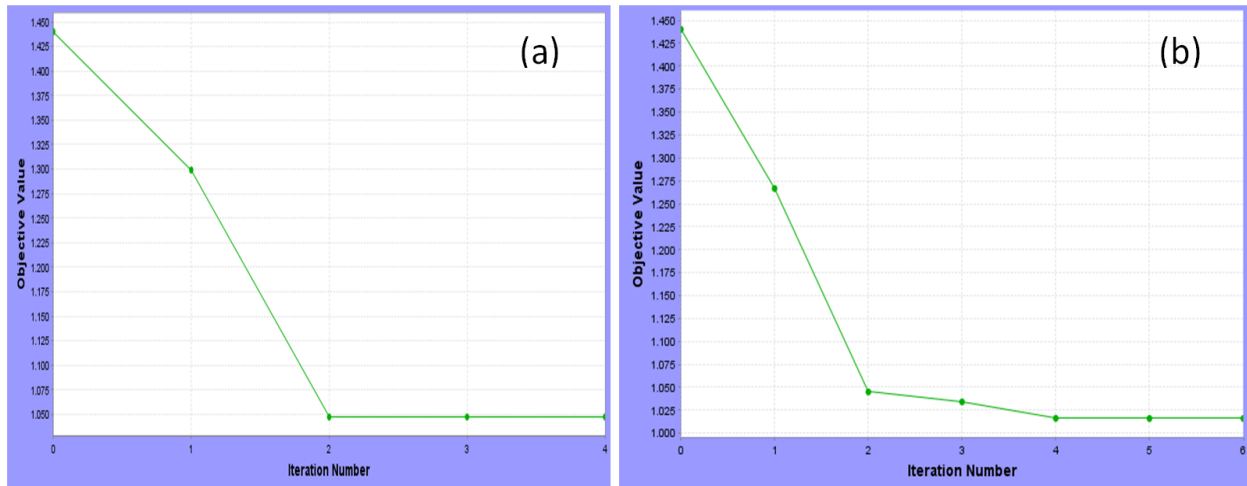|	Radial basis ROM	Kriging ROM
Best objective value of Relative Displacement	0.1016 µm	0.1047 µm
Best constraint value of accumulated plastic strain of the sintered silver layer	10.2416×10^{-3}	10.2823×10^{-3}
Standard deviation of plastic strain	0.2897×10^{-3}	0.2369×10^{-3}
Height of silicon carbide chip	0.4004 mm (scaled value is – 0.4875)	0.4077 mm (scaled value is – 0.1516)
Height of sintered silver Layer	0.02 mm (scaled value is -1)	0.02 mm (scaled value is -1)

Fig 16: (a) The value of objective function (Kriging ROM for warpage) versus iteration number and (b) The value of objective function (Radial basis ROM for warpage) versus iteration number

Best objective value of lower relative displacement from the PSO optimisation was 0.1016 μm and the ROM generated this value was Radial basis ROM. An improvement of 3% in comparison with Kriging ROM. When we consider the best constraints obtained from the optimisation for these two ROMs, mean (μ) and standard deviation (σ) of accumulated plastic strain by Kriging ROM are 10.282×10^{-3} and 0.2369×10^{-3} respectively. Assuming the accumulated plastic strain distribution follow a Gaussian distribution then, upper limit of the 95% confident interval ($\approx \{\mu -1.959\ \sigma, \mu +1.959\ \sigma\}$) for Kriging ROM 10.746×10^{-3}. Similarly upper limit of the 95% confident interval by Radial basis ROM distribution is 10.809×10^{-3}. In the optimisation task the constraint (c1) has the upper specification limit (USL) of 11.01×10^{-3}. Within these two ROM's distributions for accumulated plastic strain the higher difference between the upper limit from the upper specification limit belong to Kriging ROM accumulated plastic strain distribution. Overall, radial basis ROM slightly outperforms Kriging in this study.

6. Conclusions

This paper has discussed a computational analysis of sintered silver interconnect sandwiched between the silicon carbide chip and the copper substrate in power electronic module assembly using finite element modelling. The objective of the finite element modelling was to observe how the plastic strain were distributed on the silicon carbide chip/ sintered silver layer interface. In the FEA results, it was observed that the accumulated strain distribution was concentrated on the perimeter of the interface. Additionally this paper has discussed a computational analysis framework integrated with reliability based design optimisation methodology. This approach was applied to estimate the fatigue failure of sintered silver structure in power electronic module. Emphasis was on the numerical design methodology that builds up the modelling framework. Fast design evaluation reduced order model based on results from thermal-mechanical finite element analysis and Design of Experiments methods were developed using Kriging and Radial basis functions. The reduced order modelling approach used the prediction data for the thermo-mechanical behaviour. The fatigue lifetime of the sintered silver layer as die and the relative displacement of the sintered layer are particular interest in this study. The reduced order models were used for the analysis of the effect of design uncertainties on the reliability of the sintered silver layer. The models were be used to predict the fatigue damage in sintered silver layer.

A sample based distribution estimation technique namely Latin Hypercube sampling was utilised to predict the uncertainty effect on the characteristic performance metrics such as thermo-mechanical plastic strain accumulation per cycle of the sintered silver layer and the thermally induced warpage of the layer. Histograms generated from the Latin Hypercube sampling are fitted with various distributions for product capability indices evaluation for user specified limits. In the last section reliability based design optimisations were carried out. Latin Hypercube sampling method is combined for the purpose of carrying out reliability based design optimisation. The optimal design solution of the analysed sintered silver joint design in a power module with respect to reliability has been found in a very efficient way using stochastic global optimisation numerical technique such as particle swarm optimisation. The optimal solutions for Kriging and radial basis reduced order models with respect to reliability were compared.

Acknowledgements

References

[1] Knoerr M., Kraft S., and Schletz A., Reliability assessment sintered nano-silver die attachment for power semiconductors, 12th Electronic packaging technology conference, Singapore, Dec 2010

[2] Siow K. S., Are sintered silver joints ready for use as interconnect material in microelectronic packaging, Journal of electronic materials. 43(4), 2014

[3] Herboth T., Gunther M., Fix A., and Wilde J., Failure mechanisms of sintered silver interconnections for power electronic applications, 63rd IEEE conference on Electronic components and technology conference (ECTC), Las Vegas, NV, 2013

[4] DeVoto D J, Paret P P, and Wereszczak A A, Stress Intensity of Delamination in a Sintered-Silver Interconnection, International conference on high temperature electronics (IMAPS/HiTEC), International microelectronics assembly and packaging society, Albuquerque, New Mexico, May 2014

[5] Yu D, Chen X, Chen G, Lu G, and Wang Z, Applying Anand model to low-temperature sintered nanoscale silver paste chip attachment, Materials & Design, 30 (10), 2009, p. 4574-4579

[6] Chen G, Zhang Z, Mei Y, Li X, Lu G, and Chen X, Ratcheting behaviour of sandwiched joint by sintered nanosilver for power electronic packaging, Microelectronic Reliability, 53 (4), 2013, p. 645-651

[7] Mei Y, Chen G, Guo-Quan L, Chen X, Effect of joint sizes of low-temperature sintered nano-silver on thermal residual curvature of sandwiched assembly, International journal of adhesion and adhesives, 35, 2012, 88-93

[8] Herboth T, Früh C, Günther M, and Wilde J, Assessment of Thermo-Mechanical Stresses in Low Temperature Joining Technology, 13th International conference on thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems, EuroSimE, 2012, Lisbon, Portugal

[9] Bai J. G, Calata J. N, and Lu G, Processing and characterization of nanosilver pastes for die-attaching SiC devices, IEEE Transactions on Electronics Packaging Manufacturing, 30(4), 2007, p. 241–245

[10] ANSYS® Academic Research, Release 12.0, Ansys Inc (www.ansys.com/)

[11] Bai J. G, Low-Temperature Sintering of Nanoscale Silver Paste for Semiconductor Device Interconnection, PhD Thesis, Virginia Polytechnic Institute and State University, USA, 2005

[12] Wereszczak A. A, Vuono D. J, Wang H, Ferber M. K, and Liang Z, Properties of bulk sintered silver as function of porosity, Technical report, Oak Ridge national laboratory, USA, June 2012

[13] Dudek R, Doring R, Sommer P, and Seiler B, Combined experimental and FE-studies on sinter-Ag behaviour and effects on IGBT-module reliability, 15th International conference on Thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems (EuroSime), Ghent, Belgium, 2014

[14] Lee W. W, Nguyen L. T, and Selvaduray G. S, Solder joint fatigue models: review and applicability to chip scale packages, Microelectronics reliability, 40, 2000, p. 231-244

[15] Husain A, and Kim K. Y, Shape Optimisation of Micro- Chanel Heat Sink for Micro-Electronic Cooling, IEEE Transactions on Components and Packaging Technologies, 31(2), 2008

[16] Cressie N, Statistics for Spatial Data, John Wiley & Sons, New York, 1991

[17] Gumerov N and Duraiswami R, Fast Radial basis Function Interpolation via Preconditioned Krylov iteration, SIAM Journal of Scientific Computing, 29(5), 2007, p. 1876-1899.

[18] Wang J. G and Liu G. R, A Point Interpolation Meshless Method Based on Radial Basis Function, International Journal for Numerical Methods in Engineering, 54, 2002, p. 1623-1648.

[19] ROMARA, Reduced Order Modelling and Risk Analysis software, University of Greenwich, London, UK, http:// cmrg.gre.ac.uk/software/ROMARA

[20] McKay M. D, Conover W. J, and Beckman R. J. A, Comparison of Three Methods for Selecting Values of Input Variables in the Analysis of Output from a Computer Code, Technometrics 21, 1979, p. 239-245.

[21] Helton J. C, and Davis F. J, Latin Hypercube Sampling and the Propagation of Uncertainty in Analyses of Complex Systems, Reliability Engineering and System Safety, 81, 2003, p. 23-69

[22] Kotz S, and Johnson N. L, Process Capability Indices, Chapman & Hall, London, 1992

[23] Wu H, and Swain J. J, A Monte Carlo Comparison of Capability Indices When Process are non normally Distributed, Quality and Reliability Engineering International, 17, 2001, p. 219 – 231

[24] Minitab 16 Statistical Software (2010), State College, PA: Minitab, Inc. (www.minitab.com)

[25] VisualDOC is a product of Vanderplaats Research & Development Inc (www.vrand.com/)

[26] Venter G, and Sobieszczanski-Sbieski J, Particle Swarm Optimization, American institute of aeronautics and astronautics, 41(8), 2003, p. 1583-1589