Design of RF Amplifier with Enhanced Performance

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***Abstract* — In this paper, a RF CMOS amplifier is designed on the basis of a novel negative impedance linearization technique with negative differential resistance (NDR) element. The simulation results show that the designed amplifier can achieve high gain accuracy, good linearity with improved efficiency, revealing that the proposed technique could find wider application in RF/Microwave circuits and systems.**

Keywords - CMOS amplifier, linearization, RF feedback, negative impedance compensation, NDR

I. INTRODUCTION

Designing broadband amplifiers for digital signal transmission presents a trade-off between efficient amplifiers that create distortion or unnecessarily large and inefficient amplifiers without distortion. Therefore, in current CMOS technology, the design process is trapped in a trade-off cycle. One solution to break this cycle is to use a linearization technique to provide more flexibility for amplifier design.

In recent years, some new linearization methods such as using special predistortion [1, 2], compensating pre–post-distortion [3, 4], harmonic/intermodulation injection [5, 6] and active auxiliary compensation [7-10] have been reported. Among these new techniques, due to its significant advantages for fully monolithic design, the active auxiliary compensation has received a great deal of attention. The negative impedance linearization technique presented in [11, 12] uses a two-channel active compensation scheme, where the main amplifier provides the forward gain while the auxiliary amplifier functions as a negative impedance performing nonlinearity compensation. As discussed in [11, 12], the technique has many advantages over the existing linearization methods. However, the additional amplifier to implement the negative impedance causes more power dissipation; hence the power efficiency of the amplifier may be degraded.

In this paper, a novel RF CMOS amplifier design technique based on enhanced negative impedance compensation is presented. As can be seen, by using the negative differential resistance (NDR) [13] as a compensating device, the proposed method can improve not only the gain accuracy and the linearity but also the power efficiency greatly. The other useful features of the proposed technique are simpler structure, easy-to-implement and good for low power design.

II. NEGATIVE DIFFERENTIAL RESISTANCE (NDR)

The NDR element is commonly used in oscillator, flip-flop, adder, multifunctional logic gates etc. Because of its unique I-V transfer characteristics, it can be realized as negative impedance when biased properly. Thus the NDR element can be used to replace the auxiliary amplifier in [11, 12] to carry out the nonlinearity compensation in a RF feedback amplifier. In the novel linearization technique, using the NDR can cancel the additional power dissipated by the auxiliary amplifier, and due to improved gain accuracy, the power added efficiency (PAE) can be increased. Therefore the traditional linearity-efficiency trade-off will be overcome.

In the past most NDR devices were based on the resonant tunnelling diode (RTD). However these RTD devices are fabricated by the compound semiconductor and process [14], making it difficult to combine the RTD and NDR with other devices and circuits to achieve the system-on-chip (SoC). As shown in Figure 1, a new NDR fully composed of CMOS devices was first published in [15]. By means of the MOS-NDR element, the full linearized amplifier can be fabricated on a single chip without using any complicated and expensive process.

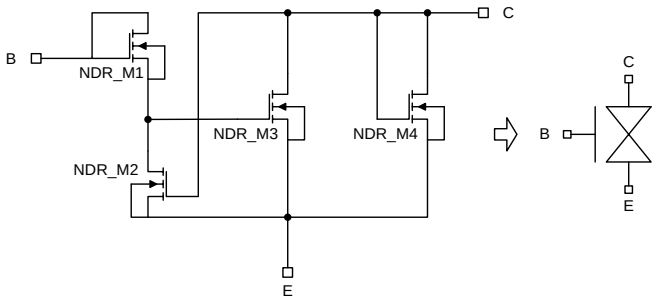


Figure 1. CMOS Negative Resistive Element and Its Symbol [15]

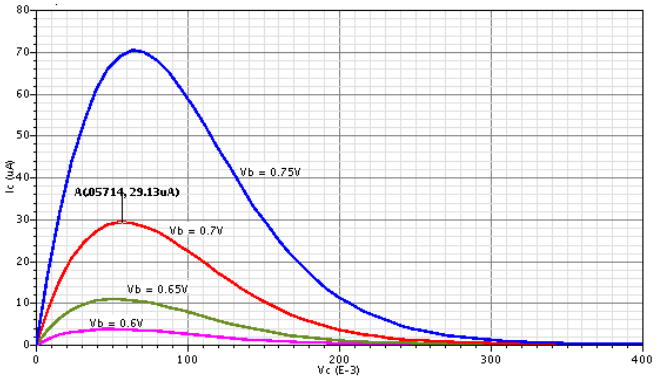


Figure 2. I_C – V_C Curve of the Negative Resistive Element in Figure 1

As shown in Figure 2, the simulated DC I_C-V_C characteristic of the element in Figure 1 demonstrates the NDR regions for different V_B values. For normal transistors, current rises with the increase in voltage, but for the NDR, the current I_C drops for the rise in voltage V_C within the given range. The inverse of slope of the curves represents the impedance; hence the negative slope demonstrates the negative impedance. This property of NDR can be utilised to realise the required negative impedance in the proposed linearization technique.

III. IMPLEMENTATION OF LINEARIZATION WITH NDR

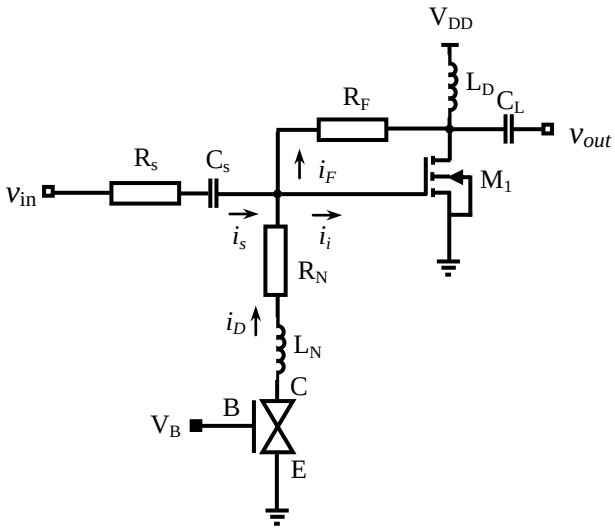


Figure 3. Linearized Amplifier with the NDR Element

As shown in Figure 3, in order to demonstrate the linearization technique an amplifier with NDR compensation has been designed, where the main amplifier is the drain–gate feedback configuration and the compensation circuit is a MOS-NDR connected to realize negative impedance. In order to obtain a closed loop gain of -5 (13.98dB), the input resistance R_S has been chosen as 400Ω and the feedback resistance R_F as 2kΩ. According to the theory presented in [11, 12] the required negative impedance for linearization can be calculated as

$$R_N = -R_S \,||\, R_F = -\frac{R_S R_F}{R_S + R_F} = -333.33\Omega \qquad (1)$$

As can be seen, in Figure 2, the I-V curve for V_b=0.7V has negative slope after peak point A ($V_c \approx 0.06$V) which represents the negative impedance of the NDR element. The value of the negative impedance realised by proper biasing (e.g. V_b = 0.7V and V_c > 0.06V) can be measured from inverse of the slope of curve. Under this condition, in Figure 3, the NDR element is biased with DC source (V_B) to remain under the downwards slope of the I-V characteristics, hence the impedance at the collector terminal of the MOS-NDR device is observed as (–1100–j12.72)Ω at 2.2GHz operating frequency. In order to realise the required negative impedance, a series structure, R_N = 766.67Ω and L_N = 0.92nH (which realised an impedance of 766.67+j12.72Ω at 2.2GHz) has been added so that the equivalent impedance seen from the base of M_1 is –333.33Ω. The implementation of the linearization has been realised in such a way that the current i_D from the NDR element neutralises the nonlinear current i_i.

Figure 4 shows the layout of the amplifier in Figure 3 by using the associated layer definitions and layout PCells of the FDK models based on 0.18µm CMOS technology. The developed layout has about 593 µm × 875 µm of chip area. In this context a simple L-section matching network has been utilized to transform input and output impedance of the developed amplifier.

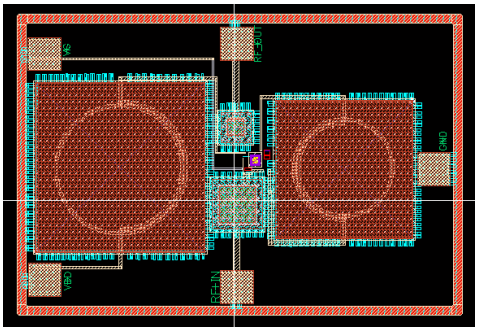


Figure 4. Layout of the Designed Amplifier

IV. SIMULATION RESULTS

In order to demonstrate the linearization method with the MOS-NDR element, both amplifier configurations with and without the linearization have been simulated using Cadence. The MOSFET transistors are simulated based on the BSIM3V3.3 models [16]. The final design parameters of the transistors are shown in Table I.

Table I: Transistor Parameters of the Designed Amplifier

Process	Transistor	Number of Finger	Finger Width(µm)	Total Width(µm)	Length(µm)
1.8V Model	M1	9	5	45	0.18
	NDR_M1	3	5	15	0.18
	NDR_M2	5	2	10	0.18
	NDR_M3	10	15	150	0.18
	NDR_M4	6	5	30	0.18

A. *Gain and Power Added Efficiency*

First, the gain of the designed amplifier, as presented in Figure 5, shows that the gain accuracy has been greatly improved with the proposed linearization technique. The gain of the amplifier without linearization is 9.8dB, a low value; but, the gain for with linearization has been improved to 13.2dB; which is much close to the ideal gain. In addition, the stable gain region of the linearized amplifier has been increased.

The simulation results in Figure 5 also show that, as a result of improved gain and increased output power without any additional auxiliary amplifier, the power added efficiency (PAE) of the linearized amplifier has been enhanced up to 30%. Hence the gain accuracy has been achieved without compromising the power efficiency.

B. *S-Parameter Simulation*

Figure 6 shows the simulation results for S_{21}, the transfer characteristics of the amplifier with and without the linearization. As can be seen, the implementation of the linearization can improve the transfer gain.

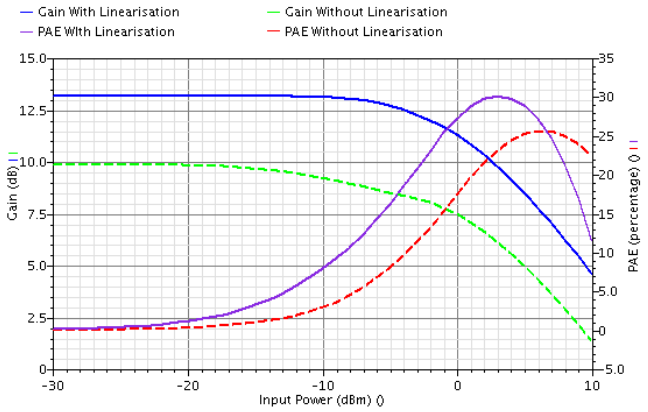


Figure 5. Gain and Power Added Efficiency

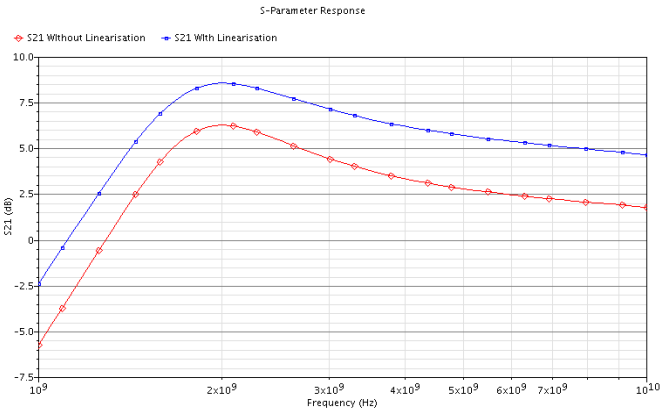


Figure 6. S_{21} for With and Without Linearization

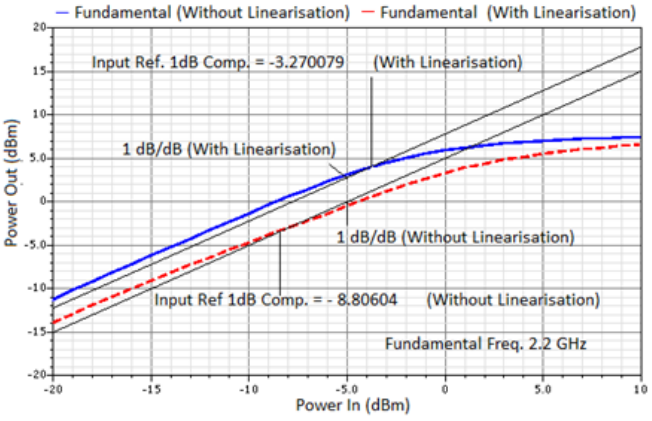


Figure 7. 1dB Compression Point

C. *Dynamic Range*

The dynamic range of the linearized amplifier can be measured by the 1dB compression point. The simulation results in Figure 7 show that the linearized amplifier has -3.27dBm input referred 1dB compression point, whereas the amplifier without linearization reaches to compression at -8.8dBm input power, revealing that the linear operating region of the amplifier has been increased with the proposed linearization technique.

D. *Intermodulation Distortion(IMD) Test*

In order to examine the nonlinearity of the designed amplifier, a two-tone test has been performed with 2.2GHz and 2.21GHz sinusoidal input signals having identical amplitude. When the input power is being increased from a given value, the IP_3 curve can be generated. As can be seen from Figure 8, the input referred IP_3 without linearization is found as 4.74dBm. However, with implementation of the linearization technique, the IP_3 can be increased to 12.925 dBm, more than 8dB of improvement has been achieved, which indicates that besides the improved gain accuracy, the third order intermodulation product with the linearization can also be suppressed.

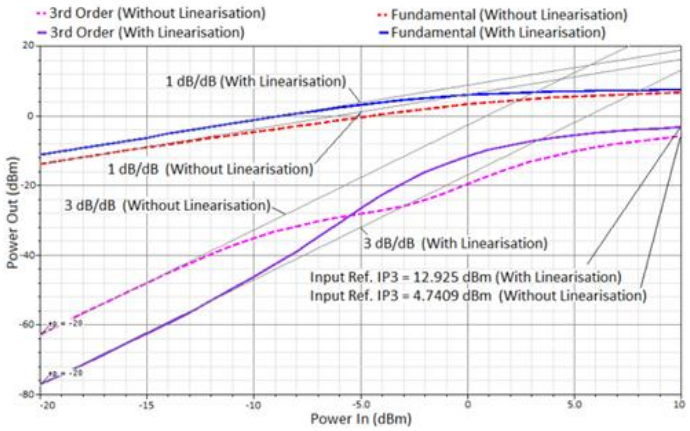
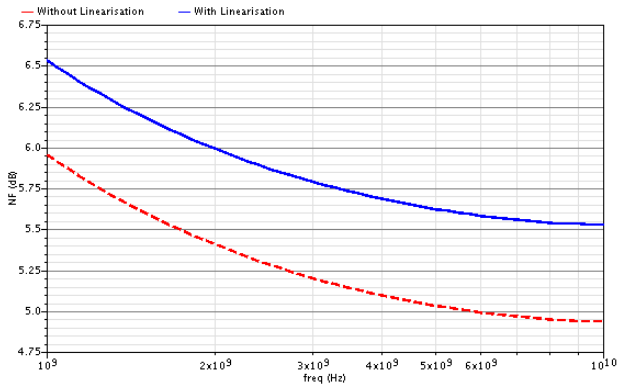


Figure 8. IP_3 Curves

E. *Noise Figure*

The noise analyses of the amplifier with and without the linearization technique have been performed with the S-parameter analysis. The simulation results shown in Figure 9 reveal that, with the implementation of the linearization, the noise figure has been improved by 0.5dB.



Figue 9. Comparison of Noise Figures

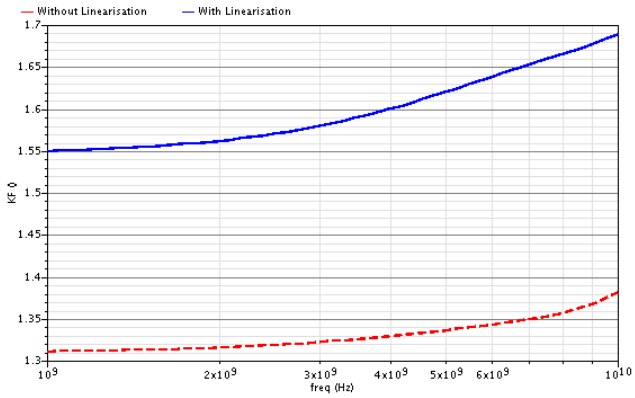


Figure 10. Stability Factor

F. Stability

Instabilities are encountered in all RF and microwave amplifiers, especially switching-mode amplifiers. In addition to the linear feedback mechanism that makes oscillation, the strong nonlinearity of power amplifiers may also lead to an unstable region [17]. According to Rollet's stability analysis [18], in order to be unconditionally stable, the developed amplifier has to satisfy $k > 1$ and $\Delta < 1$. Then, the circuit is stable no matter what passive terminations are presented in the input and output of the two-port network.

Analysis using the s-parameter demonstrated that the implementation of linearization technique improves the isolation of the two port network, i.e. increased difference between S_{11} and S_{22} at 2GHz operating frequency with lower S_{22} value. It can be assumed that the stability factor should also be increased by the linearization technique. Since the main amplifier without the linearization was unconditionally stable, the implementation of the linearized amplifier has to be stable. The simulation results shown in Figure 10 are also in agreement with the anticipated unconditional stability of the linearized amplifier.

V. CONCLUSION

The proposed linearization technique, similar to [11, 12], neutralises the distortion current caused by the feedback loop at the input of the amplifier, as a result the gain and PAE can be improved in addition to linearization.

As shown in Table II the proposed method has been compared with the previous work published in [4], [9] and [10]. As can be seen, the design results show that the new method can improve the gain accuracy and the linearity of RF feedback amplifier and enhance its power efficiency significantly. The results also confirmed that the method can achieve wider dynamic range, good noise figure and excellent stability. The proposed linearization technique has strong potential in RF/Microwave applications.

Table II: Performance Comparison

Ref.	[4]	[9]	[10]	This work
Operating frequency	2GHz	2.5GHz	2.45GHz	2.2GHz
Number of transistors	6	5	5	5
Impact on gain	Increased by 2.2%	Reduced	Reduced	Increased by 35%
IMD_3	N/A	N/A	Improved by 5 dB	Improved by 8 dB
IIP_3	Improved by 6.6 dBm	Improved by 6.8 dBm	N/A	Improved by 8.2 dB
PAE	Reduced	Reduced	Reduced	Improved by 30%

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