# Thermal and Thermo-mechanical Performance of Voided Lead-free Solder Thermal Interface Materials for Chip-scale Packaged Power Device

**KENNY C. OTIABA**

A thesis submitted in partial fulfilment of the requirements of the University of Greenwich for the Degree of Doctor of Philosophy

July 2013

## DECLARATION

I certify that this work has not been accepted in substance for any degree, and is not concurrently being submitted for any degree other than that of Doctor of Philosophy being studied at the University of Greenwich. I also declare that this work is the result of my own investigations except where otherwise identified by references and that I have not plagiarized the work of others.

Signed by Student: _____

Date: _____

Signed by Supervisor: _____

Date: _____

**DEDICATION**

*This work is specially dedicated to my dearly beloved late Mum - Mrs Caroline Ifeyinwa Otiaba (Arunne). I love you Mum but God loves you more. May your kind and gentle soul continue to rest in the bosom of the Lord. Amen*

## ACKNOWLEDGEMENTS

Firstly, I thank God who has been the source of my strength and courage during the course of this PhD study. It has been a gruelling campaign but at last; it is all over! Special acknowledgements to Dr Raj Bhatti, Dr Sabuj Mallik and Prof N.N. Ekere for their assistance, supervision and motivation during my PhD study. I am very thankful to the University of Greenwich, School of Engineering for the finance allocated to this research work.

I also very much appreciate the support from all other members of the Manufacturing Engineering Research Group (MERG) and School of Engineering staff. Of particular note is Dr Michael Okereke who assisted in the development of the MATLAB algorithm used in the generation of random solder voids. I shall not forget to thank Dr Ohid Alam for his support during the course of this thesis and for providing the solder perform samples used in the experimental study. It has been academically rewarding to have worked with you all.

Also, I want to thank Micross Components, UK for their generous support during the PhD particularly for providing the metallised die used in the experimental work. Kevin Armstrong, who sent the samples, is acknowledged too.

I would like to thank all my friends for their support and friendship over the years. It would be impossible to remember all your names, but some of those that come to mind include Nnaemeka, Obioma, Eleazar, Benjamin, Uche and Owen. A special acknowledgement goes to my sweetheart - Ngozi who kept on loving and supporting me over these years. Though we were thousands of miles apart most times, you never made me feel the distance. Your support has kept me going at critical moments and you will always be my best friend.

To my beloved family, I owe the greatest debt of all. I am not sure I would have been able to start and complete this research if not your support. Of particular mention are Daddy (Amandianeze!), Mummy, Dede, Chika, Uchenna, Onyechi, Chuks, Ify and Nneka. Thank you for your motivation and may God bless you all. Indeed, I am very grateful.

## ABSTRACT

The need to maximise thermal performance of electronic devices coupled with the continuing trends on miniaturization of electronic packages require innovative package designs for power devices and modules such as Electronic Control Unit (ECU). Chip scale packaging (CSP) technology offer promising solution for packaging power electronics. This is as a result of the technology's relatively improved thermal performance and inherent size advantage. In CSP technology, heat removal from the device could be enhanced through the backside of the chip. Heat dissipating units such as heat spreader and/or heat sink can be attached to the backside (reverse side) of the heat generating silicon die (via TIM) in an effort to improve the surface area available for heat dissipation. TIMs are used to mechanically couple the heat generating chip to a heat sinking device and more crucially to enhance thermal transfer across the interface.

Extensive review shows that solder thermal interface materials (STIMs) apparently offer better thermal performance than comparable state-of-the-art commercial polymer-based TIMs and thus a preferable choice in packaging power devices. Nonetheless, voiding remains a major reliability concern of STIMs. This is coupled with the fact that solder joints are generally prone to fatigue failures under thermal cyclic loading. Unfortunately, the occurrence of solder voids is almost unavoidable during manufacturing process and is even predominant in lead (Pb)-free solder joints. The impacts of these voids on the thermal and mechanical performance of solder joints are not clearly understood and scarcely available in literature especially with regards to STIMs (large area solder joints).

Hence, this work aims to investigate STIM and the influence of voids on the thermo-mechanical and thermal performance of STIM. As previous results suggest that factors such as the location, configuration (spatial arrangement) and size of voids play vital roles on the exact effect of voids, extensive three dimensional (3D) finite element modelling is employed to elucidate the precise effect of these void features on a Pb-free STIM selected after thermo-mechanical fatigue test of standard Pb-free solder alloys. Finite element analysis (FEA) results show that solder voids configuration, size and location are all vital parameters in evaluating the mechanical and thermal impacts of voids. Depending on the location, configuration and size of voids; solder voids can either influence the initiation or propagation of damage in the STIM layer or the location of hot spot on the heat generating chip. Experimental techniques are further employed to compare and correlate levels of voiding and

shear strength for representative Pb-free solders. Experimental results also suggest that void size, location and configuration may have an influence on the mechanical durability of solder joints.

The findings of this research work would be of interest to electronic packaging engineers especially in the automotive sector and have been disseminated through publications in peer reviewed journals and presentations in international conferences.

**Keywords:** Solder die attach, void, chip scale package, finite element analysis, thermal resistance, thermal fatigue, Lead-free solder

# CONTENTS

## Contents

## TABLES

## FIGURES

# NOMENCLATURE

## Abbreviations

| | |
|---|---|
| 2D | Two dimensional |
| 3D | Three dimensional |
| BCCs | bump chip carriers |
| BGA | Ball grid array |
| BLT | Bond-line thickness |
| CNFs | Carbon nanofibres |
| CNTs | Carbon nanotubes |
| CPES | Centre for power electronics systems |
| CSAM | Confocal Scanning Acoustic Microscopy |
| CSP | Chip scale Package |
| ECU | Electronic control unit |
| FEA | Finite element analysis |
| FEM | Finite element modelling |
| FiPoP | Fan-in Package on Package |
| ICs | Integrated circuits |
| IHS | Integrated heat spreader |
| IMC | Inter-metallic |
| IPC | Institute of Interconnecting and Packaging Electronic Circuits |
| IPEMs | Integrated power electronics modules |
| JEDEC | Joint Electron Devices Engineering Council |
| JEIDA | Japan electronic industry development association |
| MCRVEGen | Monte Carlo RVE Generator |
| MOSFET | Metal oxide semiconductor field effect transistor |
| NEMI | National Electronics Manufacturing Initiative |
| OSP | Organic solderability preservative |
| Phase | Change Materials |
| PECVD | Plasma enhanced chemical vapour deposition |
| PQFN | Power quad flat no leads |
| RoHS | Restriction of Hazardous Substances |
| ROI | Region of interest |

| | |
|---|---|
| RVE | Representative volume element |
| SAC | Sn-Ag-Cu (Tin-Silver-Copper) |
| SAC105 | Sn-1Ag-0.5Cu |
| SAC205 | Sn-2Ag-0.5Cu |
| SAC305 | Sn-3Ag-0.5Cu |
| SAC405 | Sn-4Ag-0.5Cu |
| SEM | Scanning electron microscope |
| SIA | Semiconductor Industry Association |
| SO | Small outline |
| ThCVD | Thermal chemical vapour deposition |
| UD | Uni-directional |

**Notations**

| | |
|---|---|
| $\dot{\varepsilon}_s$ | Steady state shear strain rate |
| A | Pre-exponential factor |
| a | Strain rate sensitivity of the hardening/softening |
| $a_{max}$ | Maximum number of attempts |
| $A_{STIM}$ | Area of the STIM joint |
| $A_v$ | Cross-sectional area of void |
| $A_{wj}$ | Wetting area of the solder joint |
| $C_1$ | Steady state shear strain rate |
| $c_a$ | Volume fraction of void |
| $c_s$ | Volume fraction of solder |
| $d_{ove}$ | Defined minimum accepted distance between the centres of any two voids |
| dT/dx | Temperature gradient |
| E | Young's modulus |
| E* | Calculated Young's modulus |
| $E_0$ | Young's modulus at $0^oC$ |
| $E_a$ | Young's modulus of void |
| $\varepsilon_{cr}$ | Time independent creep strain |
| $\varepsilon_e$ | Elastic strain |
| $\varepsilon_{in}$ | Inelastic strain |
| $\varepsilon_{pl}$ | Inelastic strain component |

| | |
|---|---|
| $E_s$ | Young's modulus of solder |
| $E_T$ | Temperature dependent value of Young's modulus |
| $\varepsilon_T$ | Total strain |
| $\varepsilon_{vp}$ | Time dependent visco-plastic strain |
| F | Shear force applied to the joint |
| $F_{max}$ | Thermal load |
| G | Temperature dependent shear modulus |
| $G_s$ | Shear modulus of solder |
| $h_o$ | Hardening/softening constant |
| $i_{route}$ | Iteration routes |
| K | Pre-exponential factor |
| k | Thermal conductivity |
| $k_a$ | Bulk modulus of void |
| $k_s$ | Bulk modulus of solder |
| L | Thickness of the solder |
| $L_{RVE}$ | Length of the RVE window |
| $W_{RVE}$ | Width of the RVE window |
| m | Strain rate sensitivity of stress |
| n | Plastic strain hardening component |
| $N_v$ | Number of voids |
| P | Power dissipation of the silicon chip |
| Pb | Lead |
| Q | Activation energy for creep |
| R | Universal gas constant |
| $\hat{s}$ | Coefficient for saturation value of deformation resistance |
| $s_o$ | Initial value of deformation resistance |
| STIM | Solder thermal interface material |
| T | Temperature |
| $T_1$-$T_2$ | Temperature difference |
| $T_{max}$ | Maximum temperature at the chip junction |
| $T_{min}$ | Minimum temperature at the top surface of the heat spreader |
| $v_a$ | Poison ratio of void |
| $V_i$ | Volume fraction of the inhomogeneities/voids |

| | |
|---|---|
| $v_i$ | Volume of the ith element |
| $v_s$ | Poison ratio of solder |
| $W_1$ - | Plastic work during the first load of the cycle |
| $W_n$ - | Plastic work during the lastload step of the cycle |
| α | Stress level at which the power law stress dependence breaks down |
| Wpl | Plastic work |
| $\Delta W_{pl,avg}$ | Volume averaged plastic work in the solder volume made up of n elements (i=1- n) |
| $Wpl,i$ | Plastic work in the ith element |
| θ-JC | Thermal resistance |
| ξ | Stress multiplier |
| σ | Stress |
| $\tau_{sj}$ | Shear strength of solder joint |
| $\phi_i$ | Diameter of the circular inhomogeneities/voids |

# Chapter 1: Introduction

### 1.1 Background

Thermal Management of electronic packages are poised to become one of the strategic technologies for the next generation of electronic systems. Hence, this has been identified by the National Electronics Manufacturing Initiative (NEMI) and the Semiconductor Industry Association (SIA), as one of the core research and development areas for electronic manufacturers globally[1]. The operation of power semiconductor devices at elevated temperature is a major cause of failures in electronic systems and a critical problem in developing more advanced electronic packages [2]. One such example of an electronic device is the electronic control unit (ECU) whose function in automotives has increased and is expected to further rise in the foreseeable future. As the functions of ECU in systems have increased in recent times, the number of components per unit area on its board has also risen. High board density boosts internal heat generated per unit time in ECU ambient. The generated heat induces stress and strain at the chip interconnects due to variation in the Coefficient of Thermal Expansion (CTE) of different bonded materials in the assembly. Thermal degradation could become critical and impacts device's efficiency. The life expectancy of electronic components reduces exponentially as the operating temperature rises [3] thus making thermal management pivotal in electronic system reliability.

The introduction of the recent European Union legislations (Euro 5 and 6 standards) [4] to put more stringent limits on pollutant emissions from road vehicles are amongst the major contributing factors of further ECU performance improvement.

#### 1.1.1 Motivation for electronic control unit (ECU) in automotive

The escalation of greenhouse effect as a result of increased levels of greenhouse gases in the atmosphere is considered to be the main contributing factor to global warming, which has been a universal concern [4]. With the automotive industry being responsible for a percentage of greenhouse gas emission worldwide, concerted effort is on-going by different bodies to cut down on such emission. In order to reduce the level of pollution caused by road vehicles, the European Union has introduced legislation to put more stringent limits on pollutant emissions from road vehicles, particularly for emissions of nitrogen oxides and particulates (Euro 5 and Euro 6 standards).

The latest legislation, Euro 6 standard (which will come into force on 1 September 2014) will require a substantial reduction of emission of hydrocarbon (HC), nitrogen oxides ($NO_x$) from all vehicles equipped with a diesel engine. Nitrogen oxides emission from diesel engine vehicles will be limited to 80mg/km (a 50% reduction when compared to the Euro 5

standard) [5]. It is also the goal of Euro 6 to limit carbon mono-oxide (CO) emission at 500mg/km, combined HC and $NO_x$ emissions at 170mg/km and particulates emission at 5mg/km [4-5]. Euro 6 aim to reduce fuel consumption in order to meet the growing demand for economical cars and also decrease environmental pollution caused by $CO_2$ emissions.

As a result of these increasing levels of restriction from European Union on gas emission [6], fuel injection has since replaced the carburettor (Figure 1.1-1). A carburettor in automotive engines regulates the amount of fuel that goes into the engine cylinder, thus, performs the function of fuel metering. A carburettor utilises mechanical approach in metering fuel, while fuel injection employ electronic methods, hence, the name Electronic Fuel Injection (EFI). The ECU drives the EFI and thus plays the primary role of efficiently controlling and integrating mixture formation, combustion and exhaust gas treatment. Thus, the ECU helps to achieve the lowest possible output of harmful gases and air pollution emissions. Power electronics is an enabling technology for the development of environmentally friendly and fuel efficient automotives [7] as more mechanical functions are converted to electrical and electronic functions. It is good to know that ECU may have other secondary functions in automotives such as the control of ancillary equipment including the ignition system, air compression, air bag, engine brake and alternator [6].

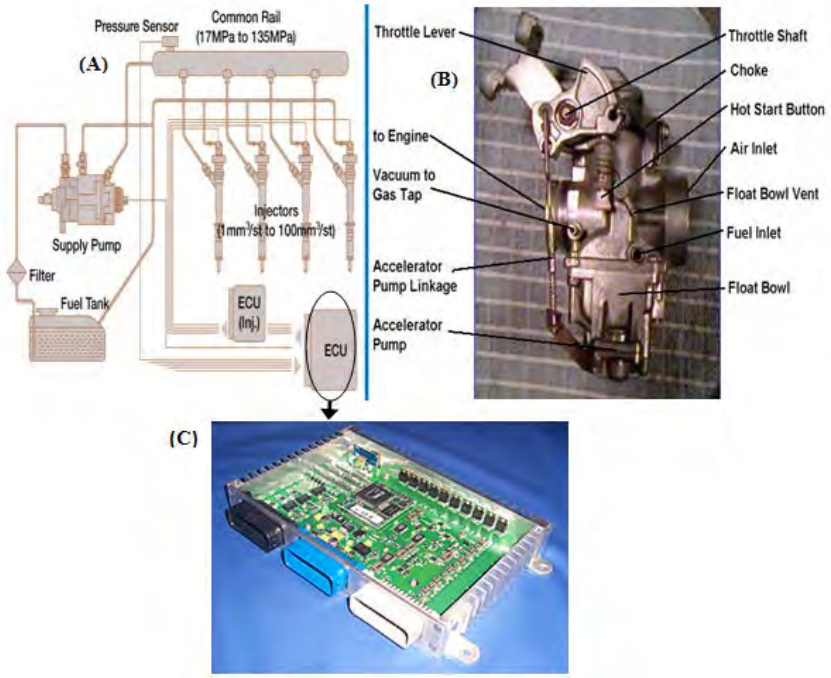



Figure 1.1-1: (A) shows schematic of ECU driving fuel injectors[8](B) shows a carburettor image [9] (C) shows custom designed ECU[10]

### *1.1.1.1 Thermal concerns in automotive ECU*

Intuitively, the next generation automotive ECU will have increased power density due to the incorporation of high-power motor controls and drive electronics that dissipate significant amount of thermal energy. For instance, if a power Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) [11] with a dimension of 10.4mm x 6.73mm x 2.36mm and a power dissipation rating of 83 W at 25$^{o}$C is used in an automotive ECU, the expected power dissipation density (of that particular area in the ECU) can be calculated as 118.58W/cm$^2$. This complements suggestions from References [12-14], that the die-level power dissipation density will exceed 100W/cm$^2$ in the next 10 years. With this power density being transformed to heat in the package, there is urgent need to efficiently dissipate the heat. This is because the life expectancy of electronic components reduces exponentially as the operating temperature rises [3]. Hence, improved heat dissipation is pivotal in electronic system design and reliability. Myers [15] and Myers et al. [16], in separate studies reported on the challenges and trends in automotive electronics thermal management. It was established that the required functionality and operating temperatures of automotives ECUs have significantly increased regardless of the decrease in size and cost of ECUs (Figure 1.1-2).

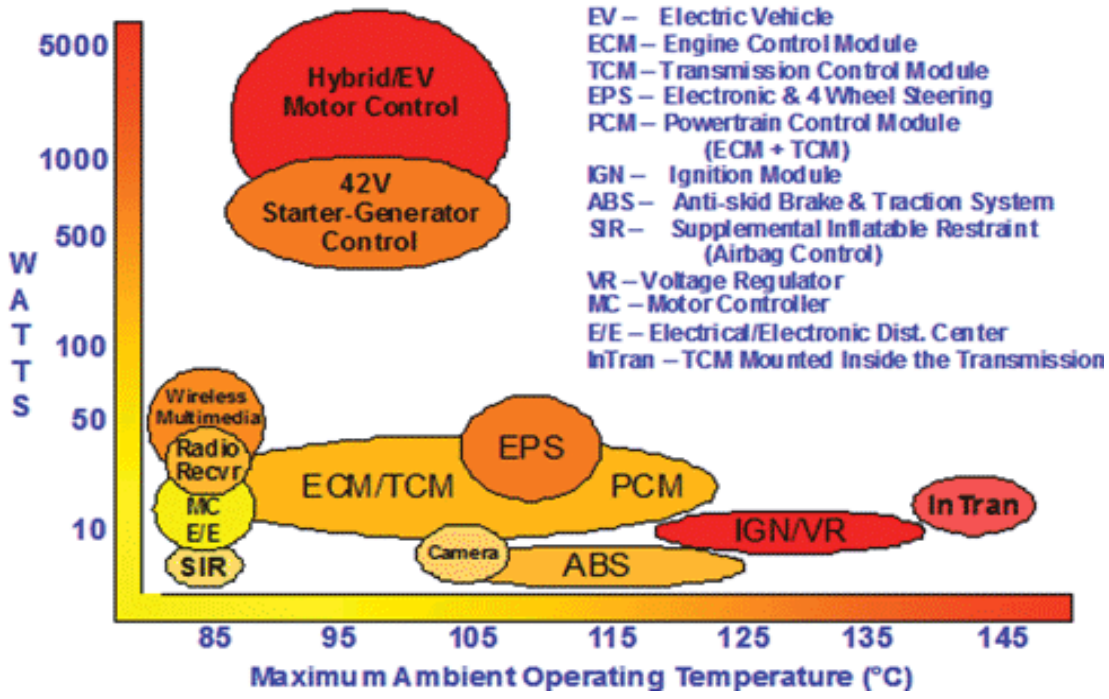



Figure 1.1-2: Thermal power dissipation and operating ambient temperature[16]

### 1.1.2 Electronics packaging - flip chip technology

Besides providing support and mechanical protection for electronic components and interconnects, packaging plays a crucial role in the overall thermal management of power device because it provides the first 'gate' for thermal dissipation from the electronic device [17]. The need to maximise thermal performance of electronic devices coupled with the continuing trends on miniaturization of electronic packages require innovative package designs for power devices and modules.

State-of-the-art packaging techniques for integrated circuits (ICs) such as chip scale packaging (CSP) technology [17-20] offer promising solution for packaging power electronics. This is as a result of the technology's relatively improved thermal performance and inherent size advantage [18]. Indeed, there has been continuous progress in applying CSP to power electronics packaging in recent years. Among such applications are the MOSFET (metal oxide semiconductor field effect transistor) BGA packages from Fairchild Semiconductor[20], FlipFET package from International Rectifier[21] and flip chip packages for power chips used in the integrated power electronics modules (IPEMs) from centre for power electronics systems (CPES)[18] (Table 1.1-1). These packages adopted the flip chip concept originally developed for IC packages and thus eliminated the leadframes and wirebonds by coupling a heat spreader directly to the backside of the die. This approach dramatically improves heat dissipation from the chip and maximises the overall thermal performance of the electronic package. In fact, Fairchild Semiconductor revealed that BGA MOSFET has a better heat dissipation ability of about 175% and 250% when compared to modified SO-8 and traditional wirebonded SO-8 packages (Figure 1.1-3), respectively [20]. When compared to wire-bonding, flip chip technology is a lower cost packaging technology which could be beneficial to the extreme cost constraints being undergone by the automotive industry; the bonding of all connections in flip chip are made concurrently unlike in wire bonding technology where one bond is made at a time. In recent years, more circuits using solder bumps are being placed in the engine compartment in order to reduce the quantity of cables and therefore, reduce costs. A depiction of the advancement in power device packaging from leadframe based to CSP technologies and emerging 3D packaging is presented in Figure 1.1-4.

Table 1.1-1: Flip chip packaging in power electronics applications[22]

| Developer | Image | Die size (mm x mm) | Rating |
|---|---|---|---|
| Fairchild Semiconductor |  | 5x5.5 | 22A, 30V Power Trench MOSFET |
| International Rectifier |  | 1.5 x 1.5 | 20V, p-channel MOSFET |
| CPES |  | 7.2 x 9 | 1200V 70A, IGBT |

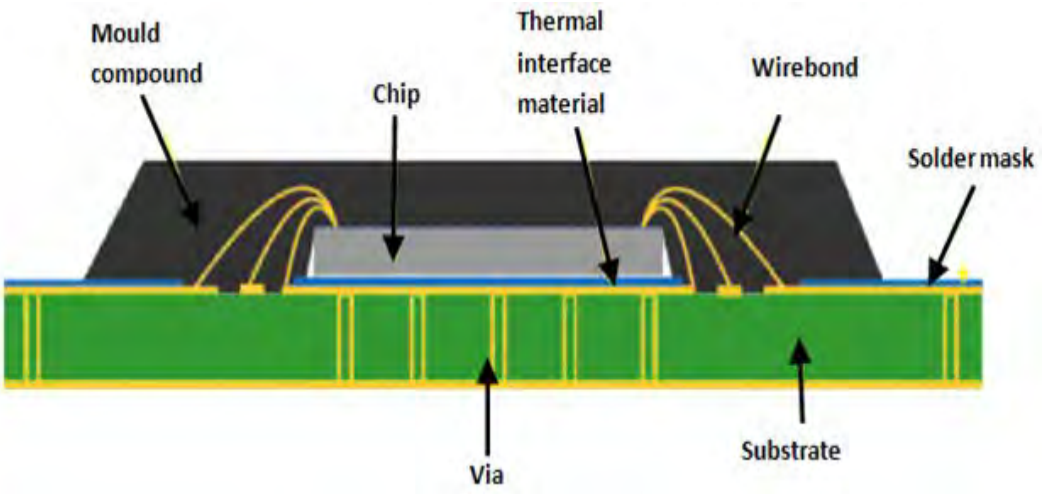



Figure 1.1-3: Schematic of wirebonded face-up silicon chip[23]

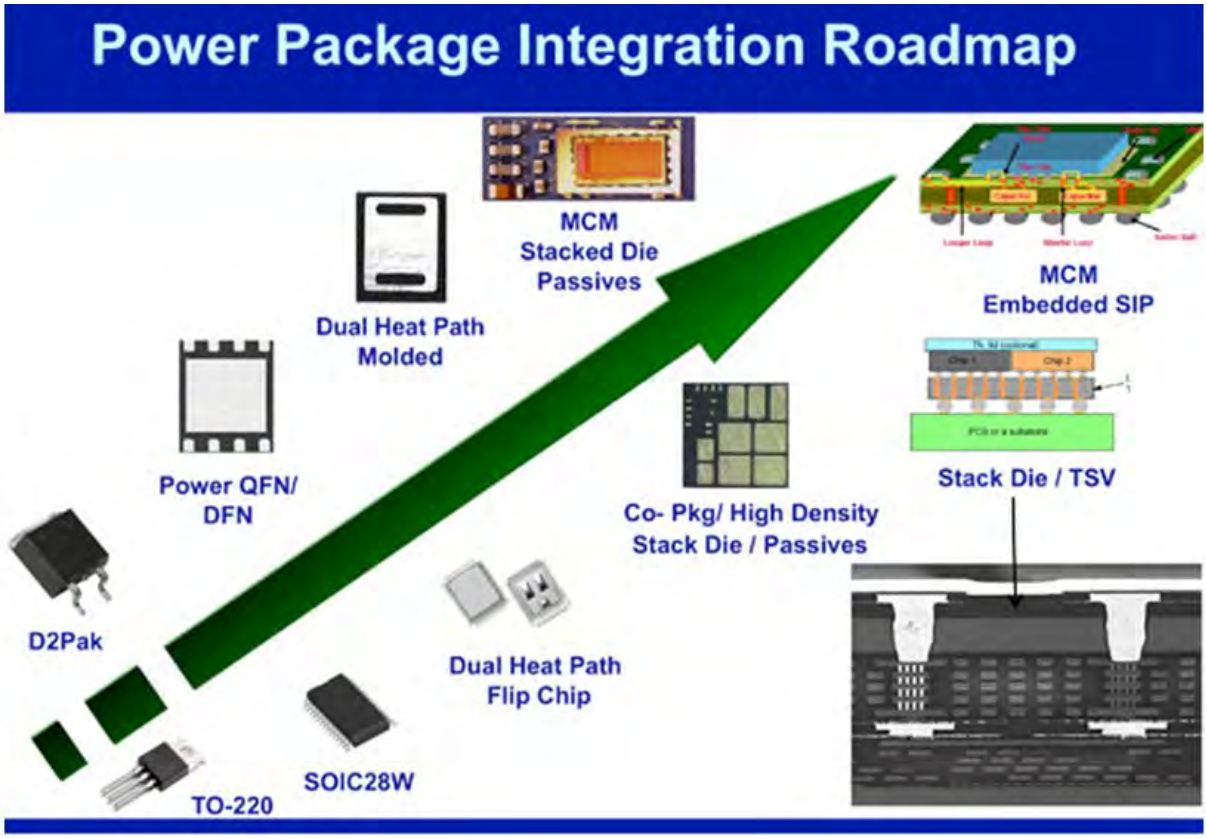



Figure 1.1-4: Power package integration roadmap [24]

Flip-chip concept is applicable to either multiple-chip module assembly (Figure 1.1-5a) or single-chip (Figure 1.1-5b). In flip-chip CSP, whilst the active side of the silicon device is mounted onto a substrate, which can be attached to a printed circuit board (PCB) via ball grid array (BGA) solder interconnections, heat removal from the device could be enhanced through the backside of the silicon die (chip). Heat dissipating units such as heat spreader and/or heat sink can be attached to the backside (reverse side) of the heat generating silicon die in an effort to improve the surface area available for heat dissipation.

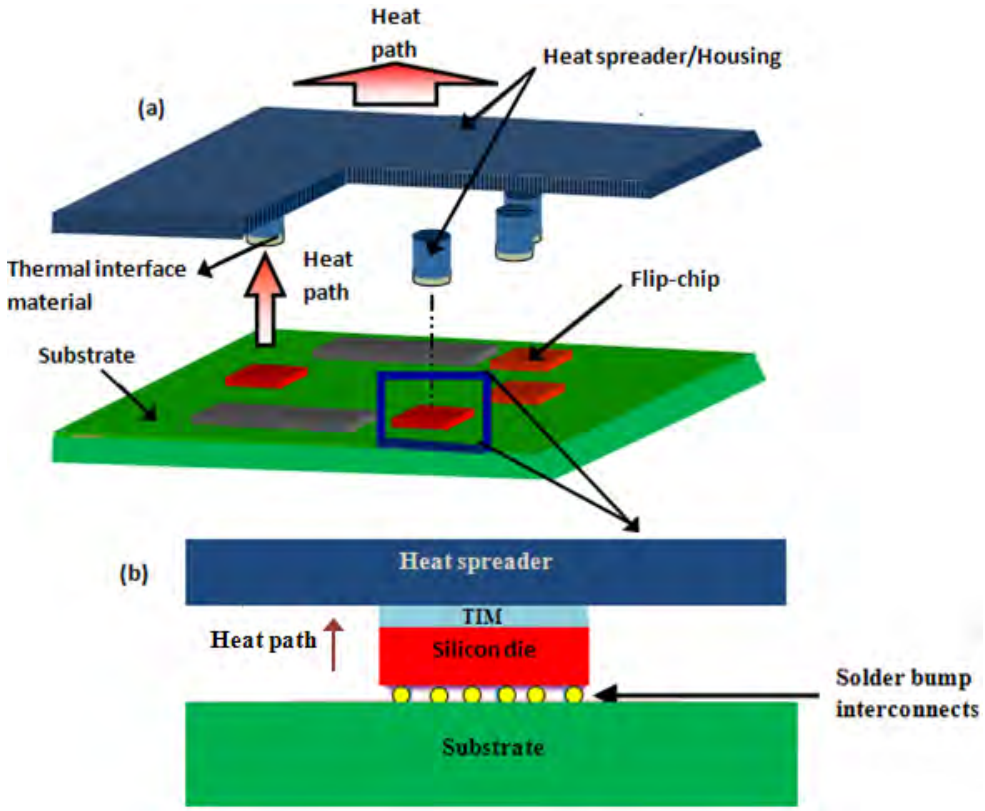



Figure 1.1-5: Schematic of flip-chip on board backside cooling, red arrows shows the heat path (a) multi-chip module; each flip-chip is coupled to the heat spreader/housing via a thermal interface material [25] (b) single chip configuration

#### *1.1.2.1 Cooling options in flip-chip package*

In addition to the enhanced cooling option provided by the backside heat sinking in flip-chip CSP, there are other feasible means of cooling. The representative heat paths for these cooling methods are shown by the arrows labelled a-c in Figure 1.1-6 and their corresponding thermal performances listed in Table 1.1-2 [25].

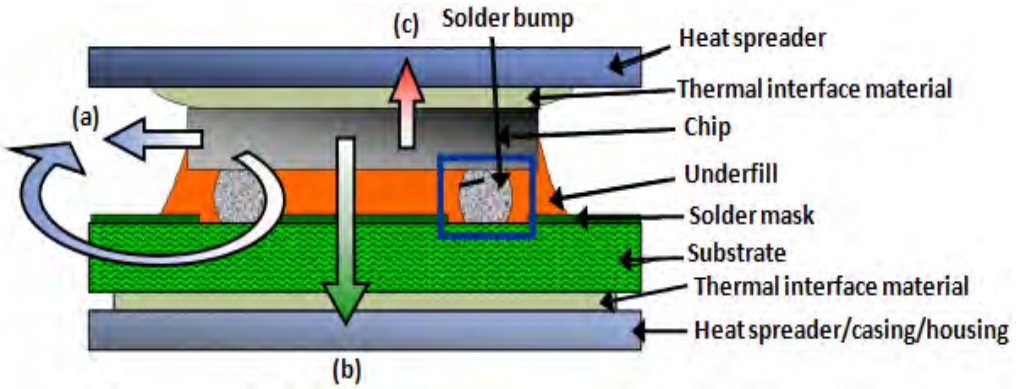



Figure 1.1-6: Three different means of cooling in flip-chip assembly (a) natural convection cooling (b) cooling through the substrate (c) cooling via the backside [25]

***(a) Convection cooling***

In this circumstance, there is no heat-spreader attached to the chip. Heat is dissipated by convection and radiation. This method offers a very poor thermal performance which is not favourable for high power dissipation. The reason for the poor thermal performance is as a result of the relative low thermal conductivity of the organic substrate and underfill (often lower by at least one order of magnitude in comparison to thermal interface material).

***(b) Cooling through the substrate***

In this cooling technique, the heat generated by the chip is dissipated by the solder bumps to the heat-spreader through the substrate. It should be noted that the heat spreader can equally act as the housing/casing. The substrate is coupled to a higher thermal conductivity heat-spreader/casing/housing using a thermal interface material in order to facilitate thermal contact. Though the thermal performance of this cooling technique is not good enough, it is better than that of cooling method (a). The poor performance can be attributed to the low thermal conductivity of the intermediate layers (particularly the organic substrate) and possibly limited number of solder bumps especially for smaller chips.

***(c) Cooling via the backside***

In this cooling situation, heat spreader which can also be part of the housing of the device is coupled to the electrically inactive side (backside) of the chip using a thermal interface material in an effort to improve heat transfer. This offers a unique thermal management basis for flip chip assemblies and represents the most effective heat dissipation path considering the less thermal resistance (shown in Table 1.1-2) provided by the direct coupling of the heat generating chip to the heat spreader using a thermal interface material. A significant improvement in thermal performance is obtained through this cooling means in comparison to other cooling means (a and b). Hence, the work reported in this thesis focuses on this backside configuration of a flip-chip package as the level of interest.

Table 1.1-2: Thermal performances of the three presented options for cooling in flip-chip assembly, these values are obtained by experimental test using a chip of area $A_{chip}$ = 20 $mm^2$ [25]

| Type | Method and heat path | Thermal resistance (K/W) |
|---|---|---|
| A | Chip – convection to housing | > 7 0 |
| B | Active (front) side of chip – board + thermal vias - housing | > 10 |
| C | Backside of chip – thermal interface - housing | < 4 |

## 1.2 Problem statement

The key concern associated with the advance thermal management "*option (c)"* as shown in Figure 1.1-6 for flip chip assembly remains the chip-to-IHS (integrated heat spreader) interface thermal resistance [26].The extreme cost constraints being undergone by the automotive industry may limit the feasibility of enhanced "surface finishing" resulting in interstitial air gaps (Figure 1.2-1)between the heat sink/spreader surface and heat source surface. The thermal resistance associated with this interfacial air gap has a detrimental impact on the overall heat dissipation from electronic devices. This interfacial thermal resistance is in series with the resistance of any heat sink and cannot be removed or reduced even by employing advanced cooling techniques on the side of the heat sink [2].

Therefore, thermal interface materials (TIMs) are employed to mechanically couple the heat generating chip to a heat sinking device and more crucially to enhance thermal transfer across the interface. TIMs need to be applied between contact surfaces to enhance heat conduction to the heat sink as air is not a good thermal conductor (0.026 W/mK at room temperature). Teertstra et al. [27] reported that by using TIM (grease), thermal resistance can be reduced by approximately a factor of five. Though TIMs are often employed to enhance heat transfer across chip-to-IHS interface [28], reports [26, 29-30] suggest that conventional polymer-based TIMs account for the largest thermal resistance in an electronic package. In fact, researchers suggest that current polymer-based TIMs contribute about 60% [1, 28, 31] interfacial thermal resistance in many electronic assemblies that employ a TIM to mount a heat sink/spreader like in automotive ECU. No wonder solder-based TIMs are preferred to

the commercially available polymer-based TIMs due to their relatively higher thermal conductivities and low thermal resistance (as will be demonstrated in the review in the next chapter); nonetheless, voiding (discussed in chapter 3) remains a major reliability concern of solder thermal interface materials (STIMs) coupled with the fact that solder joints are generally prone to thermo-mechanical fatigue failures. The inevitable solder voids, if not controlled tightly, can even increase the thermal resistance of STIMs to a comparable value to that of conventional polymer-based TIMs. The impact of voids has been well investigated for small area solder joints (flip chip solder bump and BGA) but research on thermal fatigue and thermal performance of large area solder joints (STIMs) due to the presence of voids has not had much attention compared to small area solder joints. Hence, it is crucial to investigate STIMs performance and the contribution of solder voids to the thermo-mechanical and thermal behaviour of solder TIM.

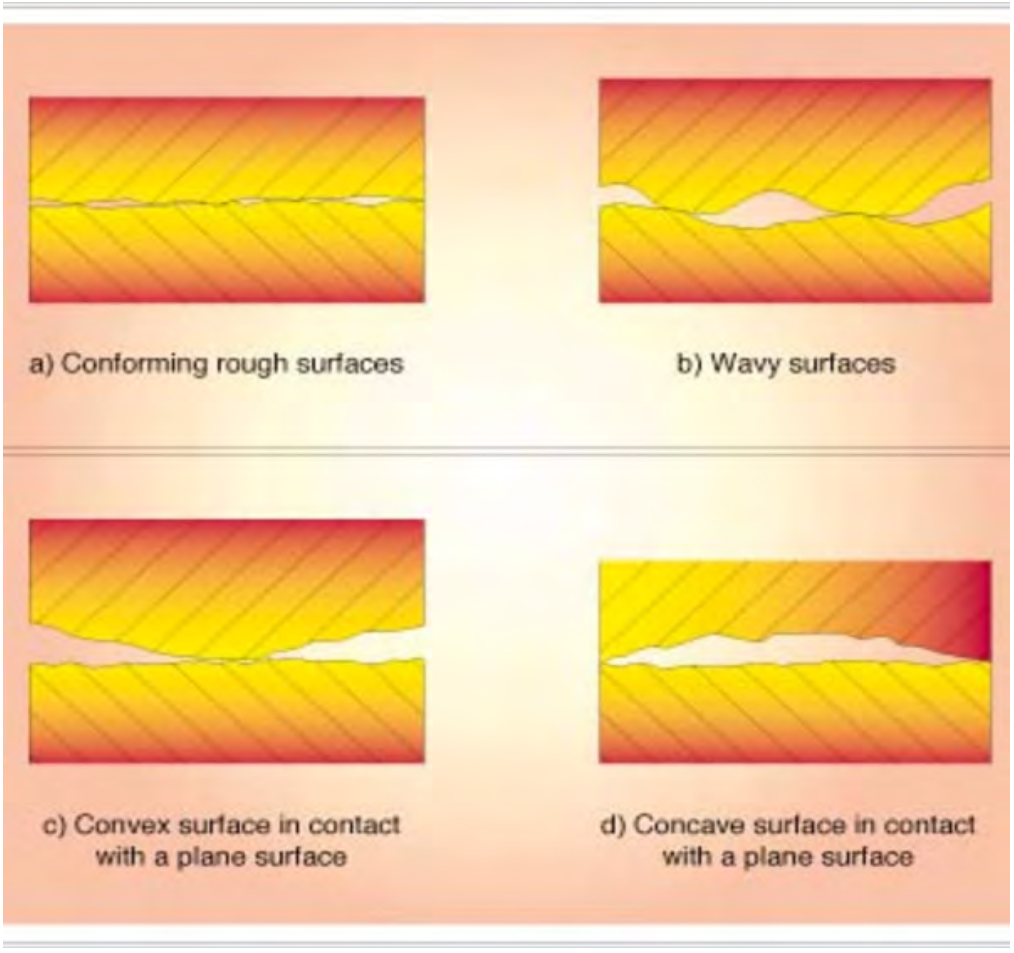



Figure 1.2-1: Different types of surface roughness[32]

### 1.3 Aim and objectives of the present work

Based on the aforementioned problem statement in (section 1.2), the aim of this work is to study the thermo-mechanical and thermal performance of voided and un-voided STIM for a chip-scale packaged power device. In order to achieve this aim, the objectives of the research work are to:

- carry out a comprehensive review of TIMs and materials exhibiting properties that suggest their suitability for use in thermal interface applications. The study will identify issues and concerns associated with the TIMs with more emphasis on voiding associated with solder-based TIMs
- investigate the thermo-mechanical fatigue life of lead (Pb)-free STIMs at various representative thermal cyclic loading conditions
- characterise the effects of different patterns of solder voids on the thermo-mechanical performance of Pb-free STIM
- evaluate the contribution of different sizes, locations and configurations of solder voids on the overall thermal performance of a chip scale package assembly
- compare and correlate voiding level and mechanical durability of various Pb-free STIMs subjected to thermal ageing

It is pertinent to note that the aforementioned tests will focus on component-first-level packaging (Figure 1.3-1) which can be extended/extrapolated to system-level packaging like in ECU (Figure 1.3-2).

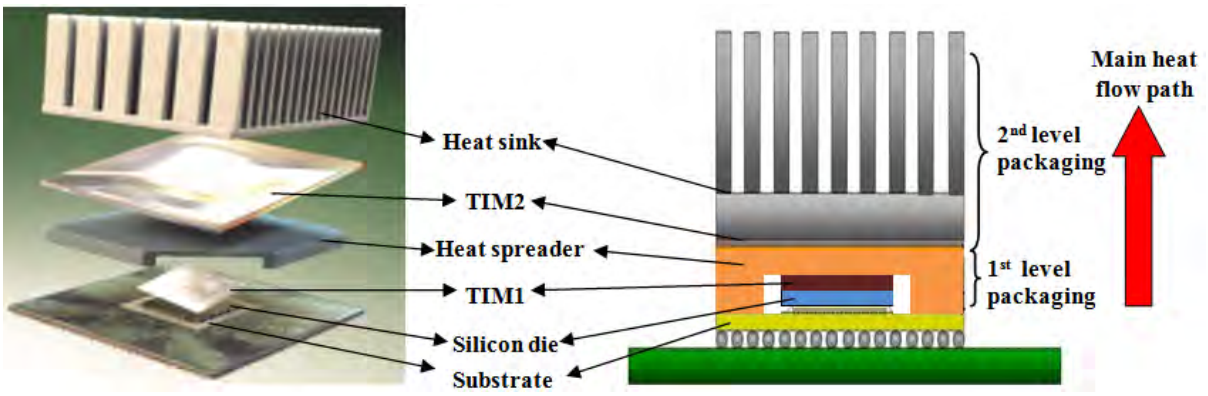



Figure 1.3-1: Packaging materials in typical power module package (component-level)[33]

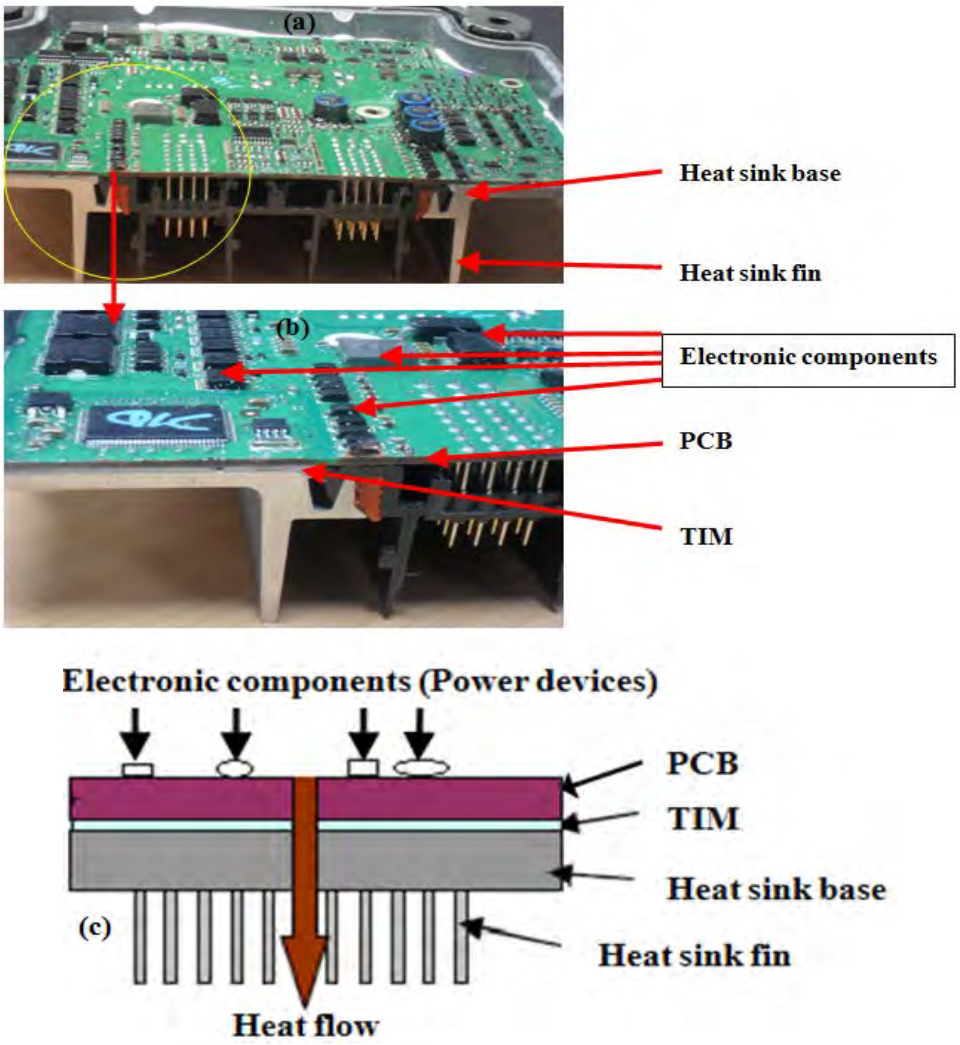



Figure 1.3-2: Packaging materials in typical power module package (system-level) (a) showing ECU heat sink base and heat sink fin (b) showing TIM, PCB and electronic components (c) schematic diagram of ECU showing heat flow path

## 1.4 Programme of work for this study

The research work reported in this thesis started with a comprehensive review of thermal interface materials (TIMs) used in thermal management applications and materials exhibiting properties that suggest their suitability for use as TIMs. The search concentrated on materials used for a wide range of applications, from domestic equipment to aerospace and was not constrained by manufacturing considerations, but identified any manufacturing issues or concerns associated with the materials. The review identified solder thermal interface material (STIM)as a feasible technology which manifest promising potentials for use in automotive ECU applications due to its higher thermal conductivity and low thermal resistance compared to its polymer based counterparts. However, voiding which was identified as one of the main manufacturing defects of solder joints remains a major

reliability concern in the use of solder as TIMs coupled with the fact that solder joints are generally prone to thermo-mechanical fatigue failures. Solder voids could affect the mechanical and thermal reliability of solder joints. Generally, previous research suggest that the level of void effect may depend on the solder properties, geometry of the joint, size, location and the pattern of void and the loading type.

Hence, more studies are needed for an in-depth understanding of the precise contribution of different features (size, fraction, spatial distribution, etc.) of voids to the mechanical and thermal behaviour of Pb-free STIM. This is crucial especially considering that most of the experiments and modelling on solder joints have been carried out on the effect of void on other applications of solder interconnects such as BGA, solder bumps and also under different loading rather than thermo-mechanical. Additionally, some of the studies reported in literature were carried out only on Pb-based and as such have only considered very limited range of void sizes and percentage. In some of the finite element modelling studies, the material property used in modelling solder does not incorporate visco-plastic or creep deformation.

The foregoing formed the motivation for this research. Experiments were designed to address the aforementioned concerns. The four-case experiments include; "*Case A*" with two geometric models (GMs) for thermo-mechanical characterisation of two standard Pb-free solders as STIMs; "*Case B*" incorporating a thermo-mechanical parametric study, with eight geometric models for study on impacts of different void configurations, five geometric models for study on different void locations and four geometric models for study on different void depth; "*Case C*" incorporating a thermal parametric study with eight geometric models for study on impacts of different void configurations, four geometric models for study on different void location, four geometric models for study on different void depth and fourteen geometric models for study on the effect of chip heat generating area on thermal resistance values; "*Case D*" with sixteen test vehicles for comparing and correlating the voiding level and mechanical durability of different Pb-free solders. The geometric models served as input to ANSYS finite element analysis (FEA) software employed in the study. The modelling steps involved meshing the geometric models, applying the constitutive models of materials, boundary conditions and load. The sixteen samples were reflowed in a reflow oven, characterised for void percentage using X-ray tool, subjected to thermal load and shear test. The parameters used in explaining the results include - stress, strain energy, plastic work, plastic work density for the thermo-mechanical analysis; thermal resistance, junction

temperature for the thermal analysis; void percentage and shear strength for the experimental work. The programme of work is depicted in Figure 1.4-1.

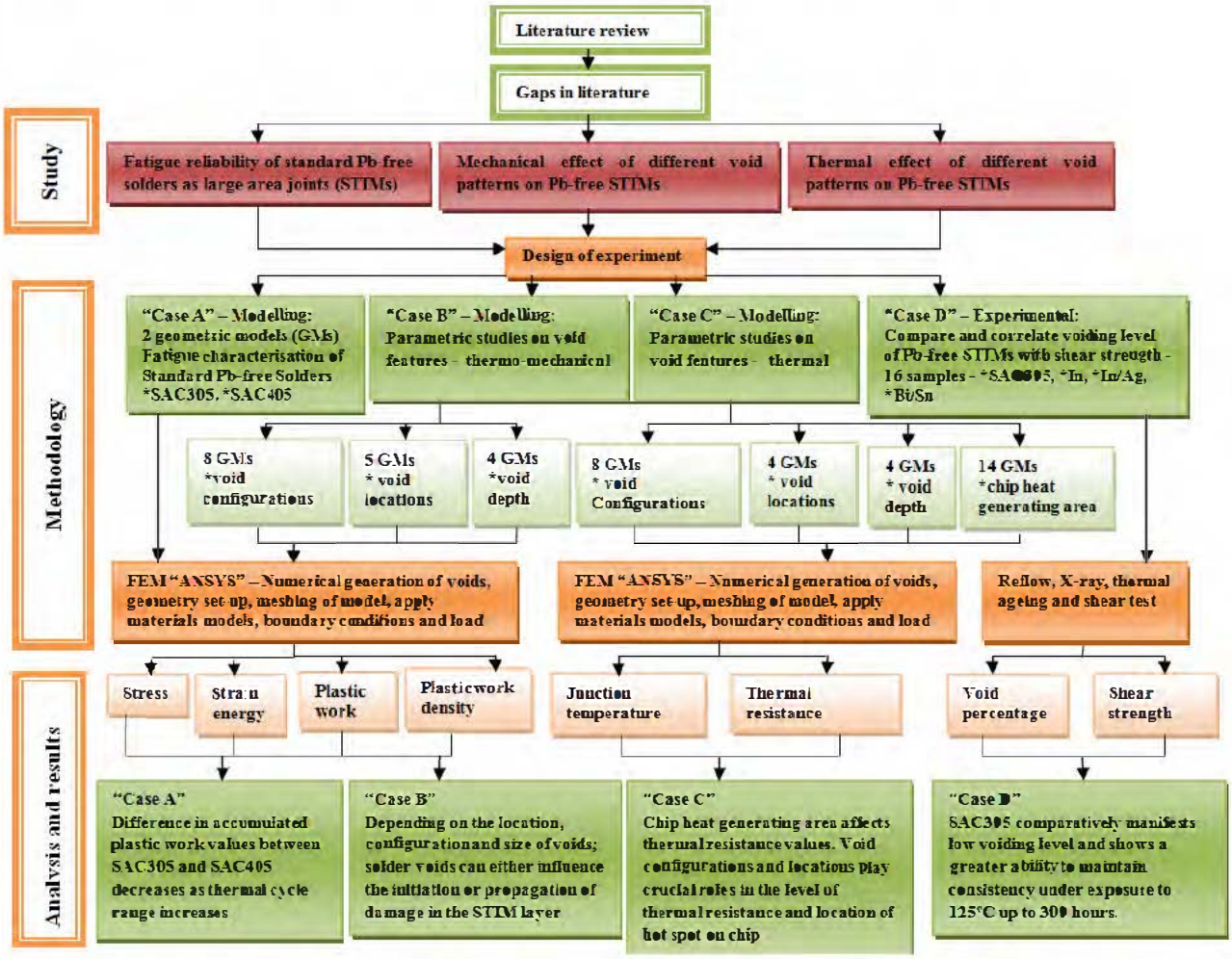



Figure 1.4-1: Programme of work for this PhD research

## 1.5 Major findings

Since most of the concepts reported in this thesis have been published, to the author's best of knowledge, many findings from this work are considered significant:

i. The difference in accumulated plastic work values between SAC305 and SAC405 decreases as thermal cycle range increases and is lowest (8%) under thermal load case C (-65°C to +150°C) compared to other studied cases of thermal cyclic loading (-55°C to 80°C and -55°C to 125°C).

ii. For all cases of cyclic thermal loading considered in this study, the maximum values of induced strain energy are all located in the corner regions of the studied solder joints at the side next to the silicon die. This is identified as the critical region and analogous to the crack path as observed in an experimental work elsewhere.

iii. The method of employing damaged parameters averaged over certain thickness of element layers for fatigue lifetime prediction is questionable when the geometry of the solder joint is different from small area solder joints such as flip-chip solder bumps or BGA solder joints. As these damaged parameters are conventionally extracted from a certain volume taken around a critical region in the height direction of the solder bump or solder ball, it is unclear the pattern of the chosen volume of elements in large area solder joints like the studied solder die-attach.

iv. The sensitivity of solder joint fatigue life to the configuration of voids increases as the void percentage increases.

v. The effect of large voids on obtained damage parameters in the studied solder joints was more profound compared to small randomly distributed voids. It was observed that the small voids around the critical region of the solder joints appeared to enhance stress and strain localisation around the maximum damage site thus facilitating damage initiation. However, the small voids also showed potentials of arresting the damage propagation by blunting the crack tip and thus increase the overall fatigue life of the solder joint.

vi. Strain energy in the solder joint increases as void gets closer to the critical site which may enhance damage initiation. Void further away from the critical region did not alter/influence damage distribution in the solder joint.

vii. Voids located in the surface of the solder joint were more detrimental compared to void embedded in the middle of the solder layer. Precisely, void situated in the surface between the solder joint and silicon die (where the critical site is located) was more detrimental to the solder joint reliability compared to void located in the solder/copper interface. Through void (void extending through the entire solder thickness) resulted in the most damaging parameter compared to the shallow void cases.

viii. Thermal resistance values are dependent on the heat generating area of the chip.

ix. Large single void has a more detrimental impact on thermal resistance compared to small distributed voids of equivalent void percentage.

x. Shallow voids formed in the solder die attach layer next to the surface of the heat generating chip result in a relatively higher thermal resistance than equivalent shallow voids present at other vertical positions further from the heat generating chip.

xi. Thermal resistance is highest for voids present near the center of the heat source. A void at the edge (very far from the heat source) of the solder die attach layer may not result in hot spot (representing the hottest spot at the chip back surface).

xii. The shear strength of SAC305 is relatively higher than other Pb-free solders evaluated in this study. There was no significant change in the magnitude of shear strengths of SAC when subjected to thermal ageing at 125$^{o}$C up to 300 hours. This suggests a greater ability of SAC305 alloy to maintain consistency under exposure to high temperature for a long time.

## 1.6 Thesis outline

This report consists of ten chapters with sections and subsections. References are listed in the last chapter (chapter 10).

*Chapter one*

This contains a clear introduction to the topic which identifies the rationale behind the research. The aim, objectives and scope of the research effort are also featured in this chapter.

*Chapter two*

This provides a comprehensive review of state-of-the-art polymer-based TIMs and STIMs and emerging nanotechnology-based TIMs. The review focuses on the exploration, characterisation, identification and understanding of all the parameters and mechanisms that have an impact on the thermal and also mechanical performance of the TIMs. This chapter will contribute to the understanding of the in situ behaviour and reliability (like impact of thermal cycling, aging effects) of TIMs.

Chapter three

The purpose of chapter three is to present detailed information on voiding associated with STIMs. The main factors that lead to void formation are discussed in this chapter. Also reported in this chapter is a review of the mechanical and thermal influence of voids on solder joints with highlights of the gaps in literature. Finally, available standard void inspection criteria are elaborated in this chapter.

*Chapter four*

This chapter introduces finite element modelling (FEM) of STIM layer. The development of numerical models used for the implementation of circular random solder voids in a STIM layer is presented in this chapter. This is accomplished using an algorithm that can successfully generate random circular voids within a defined representative volume element

(RVE).The theory of solder constitutive material model and a summary of the modelling assumptions are presented in this chapter to describe the modelling process adopted for the STIM.

*Chapter five*

A detailed finite element analysis (FEA)of the effect of silver content for Sn-Ag-Cu (SAC) alloy compositions on thermal cycling reliability of the Pb-free solder TIMs (die-attach) is presented in this chapter. Results of the thermal fatigue performance of two standard SAC alloys as TIMs subjected to various representative thermal cyclic loading profiles are reported in this chapter. The results are discussed in terms of stress, strain and accumulated plastic work in the solder joints. Based on the results, a suitable SAC alloy is then selected for further analysis on the thermo-mechanical and thermal effects of voids on the SAC alloy as STIM.

Chapter six

This chapter details the results of FEA study on the impacts of different void sizes, configurations and locations on thermo-mechanical performance of the selected SAC STIM. The random small and large voids in the STIM layer generated using a pre-defined algorithm is employed for a comparative study on the effects of different void configurations (large voids vs. small voids) on thermo-mechanical performance of the STIM layer. Also, the effects of different void locations and depth on the thermo-mechanical performance of the STIM are covered in this chapter.

*Chapter seven*

In this chapter, thermal simulations are carried out to characterise the thermal impacts of different patterns of solder voids on the overall thermal performance of a chip-scale package assembly. A brief introduction on the theory of thermal impacts of voids on TIMs is followed by the definition of boundary conditions and presentation of FEM results. Thermal performances are evaluated using key thermal parameters including chip junction temperature, thermal resistance and location of hot spots. The FEM results are presented for the effect of different void sizes, void configurations and void locations. New symmetric voided die-attach TIMs are generated for study on the effect of heat generating area of a chip on thermal resistance values.

*Chapter eight*

This chapter presents the results of an experiment work conducted on different Pb-free solder compositions as TIMs. The solders are reflowed according to the manufacturer's guide and then subjected to different hours of thermal ageing. The level of voiding and shear strength values for the Pb-free solders are evaluated and then compared with the selected SAC alloy.

*Chapter nine*

This chapter highlights the conclusion, contributions, future work and recommendations based on work carried out.

The Appendix contains details of the MATLAB algorithm and ANSYS code used in generating random voids in the STIM layer and calculating the accumulated plastic work in the solder joints, respectively.

## 1.7 Publications

**Journal papers from work reported in the thesis**

- **Otiaba K.C.** et al. (2011) "Thermal interface materials for automotive electronic control unit: Trends, Technology and R&D challenges" Microelectronics Reliability Journal, 51(12), pp. 2031–2043. As of December 2012, this journal remained in one of the top twenty five Hottest articles "Most Downloaded Microelectronics Reliability Articles" since December 2011 when it was published (SciVerse Scopus).

- **Otiaba, K.C.** et al., (2012), Numerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device" Microelectronics Reliability Journal, 52(7), pp. 1409–1419

- **Otiaba, K.C.** et al., (2012), Finite element analysis of the effect of silver content for Sn-Ag-Cu alloy compositions on thermal cycling reliability of solder die attach, Engineering Failure Analysis Journal, 28 (2013), pp.192-207

**Other journal papers**

- **Otiaba, K.C.** et al., (2011) "Thermal Management Materials for Electronic Control Unit: Trends, Processing Technology and R and D Challenges" Advanced Materials Research, 367, pp. 301-307

- E.H. Amalu, W.K. Lau, N.N. Ekere, R.S. Bhatti, S. Mallik, **K.C. Otiaba**, G. Takyi, (2011) "A study of SnAgCu solder paste transfer efficiency and effects of optimal reflow profile on solder deposits" Microelectronic Engineering, 88, (7), pp. 1610–1617

**Journal paper submitted (Under review)**

- **Otiaba K.C.** et al. "Numerical assessment of the effect of void morphology on thermo-mechanical performance of solder thermal interface material"

**Conference papers**

- **Otiaba, K.C.** et al. (2012), Influence of thermal ageing on process-induced voids growth and shear strength for selected lead free solder thermal interface materials, IMAPS 2012, 45th International Symposium on Microelectronics, USA, September 9 - 13, 2012

- **Otiaba, K.C.** et al. (2011) "Emerging nanotechnology-based thermal interface materials for automotive electronic control unit application" 18th IEEE European Microelectronics and Packaging Conference (EMPC), 12-15 Sept. 2011

- **Otiaba, K.C.** et al. (2011) "Comparative study of the effects of coalesced and distributed solder die attach voids on thermal resistance of packaged semiconductor device" 17th IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 27-29 Sept. 2011

- **Otiaba, K.C.** et al. "Thermal effects of die-attach voids location and style on performance of chip level package" 3rd IEEE International Conference on Adaptive Science and Technology (ICAST), 24-26 Nov. 2011

- M. Ekpu; R. Bhatti; N. Ekere; S. Mallik; E. Amalu; **K. Otiaba**, (2011) "Investigation of effects of heat sinks on thermal performance of microelectronic package" 3rd IEEE International Conference on Adaptive Science and Technology (ICAST), 24-26 Nov. 2011

- M. Ekpu; R. Bhatti; N. Ekere; S. Mallik; **K. Otiaba**, (2012) "Effects of thermal interface materials(solders) on thermal performance of a microelectronic package"

Symposium on. Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP), 25-27 April 2012

# Chapter 2: Literature review 1 - Thermal interface materials: Trends, technology and R&D challenges

## 2.1 Introduction

The heat source (chip) surface and heat sink surface being mated together consist of mixture of surface roughness and surface non-flatness as shown in Figure 1.2-1, page 11, resulting in the interface area being separated by air filled gaps. As air is not a good thermal conductor (0.026 W/mK at room temperature), TIMs owing to their inherent thermal conductivity are employed to fill interstitial air space thereby increases heat dissipation from electronic device. The interfacial thermal resistance due to the interstitial air space is in series with the resistance of any heat sink and still remain even by employing advanced cooling techniques on the side of the heat sink [2]. Hence, thermal interface materials (TIMs) play vital role in electronic packages as they enhance heat conduction to the heat sink.

In ECU, TIMs can be employed between the printed circuit board (PCB) and the housing base plate (system level) as shown in Figure 1.3-2 (page 13) and between the chip (silicon die) of a power semiconductor device and its heat spreader (component level) as shown in Figure 1.3-1 (page 12).

This chapter provides a comprehensive review of state-of-the-art TIMs and emerging nanotechnology-based TIMs focusing on the exploration, characterisation, identification and understanding of all the parameters and mechanisms that have an impact on the thermal and also mechanical performance of TIMs. This chapter will contribute to the understanding of the in situ behaviour and reliability (like impact of thermal cycling, aging effects) of TIMs. This chapter is divided into five sections including the introduction. Section two provides an overview of traditional TIMs including polymer-based and solder-based TIMs. Section 3 is devoted to the implications of emerging nanotechnology in TIMs. The challenges facing the application of conventional and emerging TIMs are discussed in section 4. Finally, section 5 gives the summary of the details discussed in the chapter.

## 2.2 Traditional thermal interface materials (TIMs)

With the exception of pure metals, TIMs are typically made up of polymer or silicone matrix filled with thermally conductive particles (that is metals, ceramics, carbon) [34-36], commonly between 2–25 μm in diameter[37]. Some of the requirements expected of TIMs include [35-37] –

- High thermal conductivity.
- Suitability to application environment.

- Ability to reduce thermal stress between regions with largely different coefficient of thermal expansion (CTE).
- Capability to be reworked.
- Low viscosity at operational temperatures.
- Ability to maintain performance indefinitely.
- Not being able to leak out of the interface.
- Ability to be deformed easily by less contact pressure to contact all uneven areas of both mating surfaces and minimal thickness.

These requirements make the development of new, improved TIMs a complicated process.

### 2.2.1 Polymer-based TIMs

As discussed below, most of the polymer-based TIMs that can be used to reduce total interfacial resistance are classified as thermal greases and thermal pads (soft metals) [38]. The pros and cons of these TIMs are illustrated in Table 2.2-1 (page 31).

#### *2.2.1.1 Thermal grease*

Grease is traditionally referred to as the first class of TIM developed with the aim of filling interstitial space between solid interfaces thereby reducing interfacial air gap [39]. Thermal grease is a form of thick paste composed of thermally conductive filler dispersed in silicone or hydrocarbon oil. Thermal grease usually comes in a syringe, a tube, or a small plastic sachet. Thermal grease typically has a thermal conductivity in the range of 0.4-5W/mK depending on composition [40]. The thermal conductivity of grease can be increased by the addition of more conductive fillers [41], but this may result in an increase in viscosity, bond-line thickness (BLT) and subsequent total effective resistance of the grease [42]. Purely viscous fluid materials are explained by Newtonian and power-law fluid models. The interfacial resistance of thermal grease ranges from 0.2 - 1Kcm$^2$/W. Depending on the type of filler material employed, thermal grease/paste may be categorised into three groups:

***Metal-based thermal pastes****:* These materials employ metals (such as Ag, Cu or Al) as fillers. Although metal based thermal pastes offer better thermal conductivity, they have a high manufacturing cost. The other crucial issue is that these pastes are electrically conductive which limits their use in electronic devices.

***Ceramic-based thermal pastes****:* Ceramic-based pastes are widely used because of their good thermal conductivity and low cost. These materials mainly consist of a ceramic powder

suspended in a liquid or gelatinous silicone compound. The most commonly used ceramics are beryllium oxide, aluminium nitride, aluminium oxide, zinc oxide, and silicon dioxide.

***Carbon-based thermal pastes**:* The most recent development in this category is the discovery of high thermal conductivity in carbon nanotubes (CNTs) and carbon nanofibres (CNFs) [29, 31, 37, 43-47]. Though this technology is still in the laboratory stage, suggestions have emanated that CNTs and CNFs could be employed to improve heat conduction within TIMs. This is further discussed in more details in chapter 7.

In summary, one of the immense advantages of thermal grease is their relative lower cost compared to other TIMs. Also, beneficial is their ability to fill interstitial gaps properly with less pressure. However, it is disadvantageous that thermal grease is vulnerable to pump-out (Figure 2.2-1) and dry-out effects (Figure 2.2-2) when exposed to thermal and power cycle resulting in thermal resistance increase (Figure 2.2-3). In addition, handling of thermal grease tends to be messy and time consuming. Thermal pads prove advantageous in this regard.

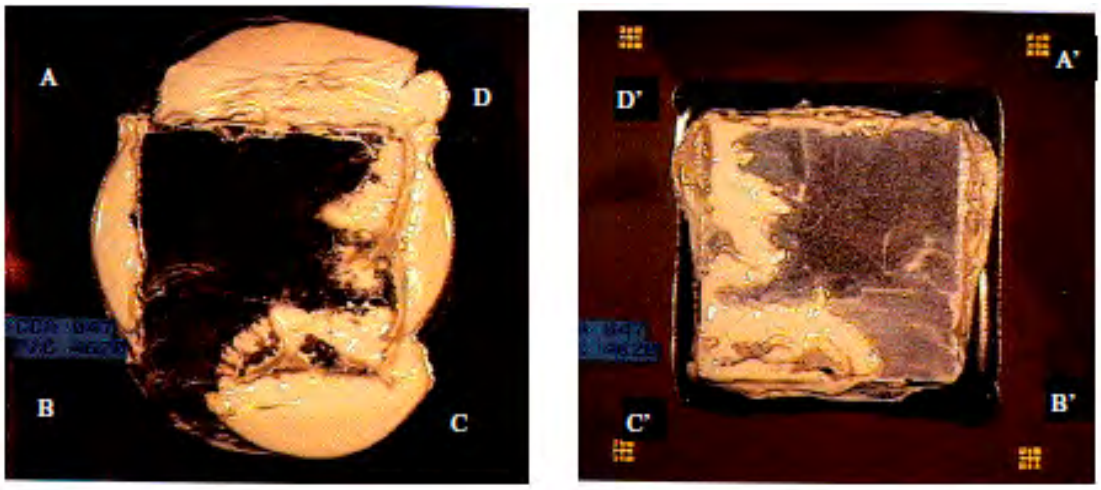



Figure 2.2-1: Typical illustration of thermal grease pump-out[34]

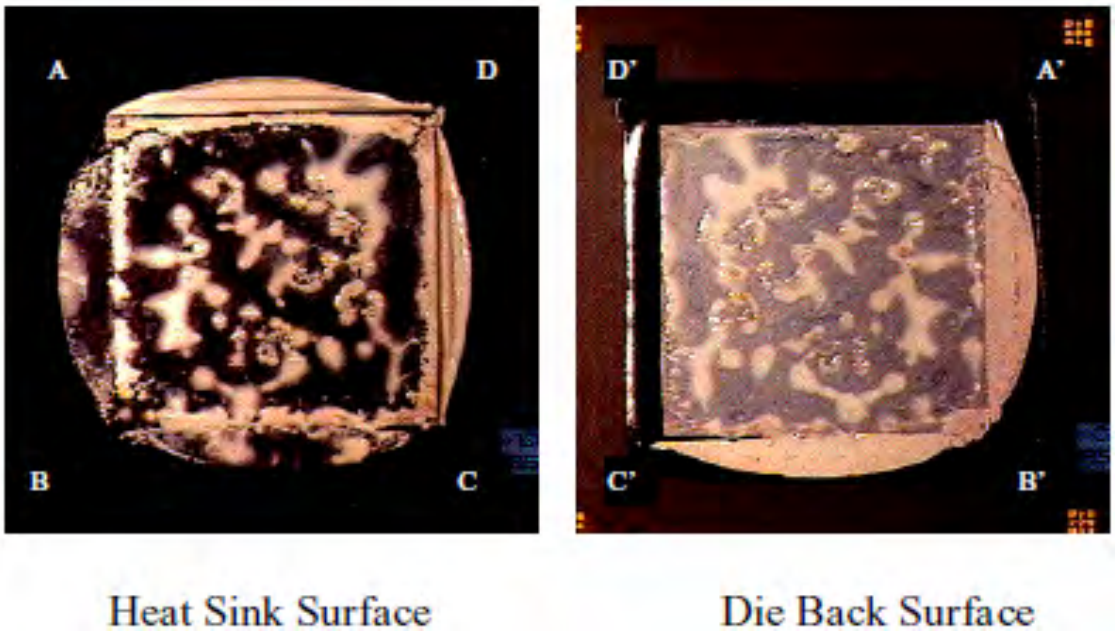



Figure 2.2-2: Typical illustration of thermal grease dry-out[34]

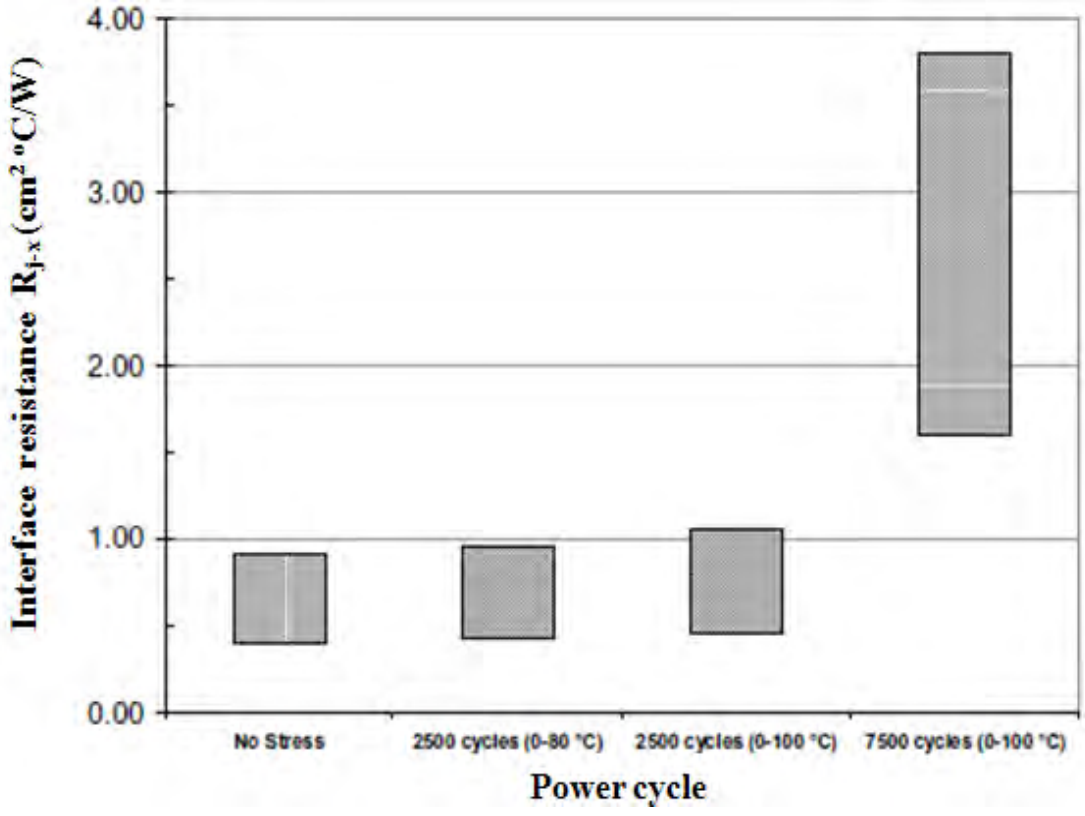



Figure 2.2-3: Impact of environmental stress conditions on thermal grease performance[34]

#### *2.2.1.2 Thermal pads*

These materials are usually in form of a pad and also referred to as elastomeric pads. Pads typically consist of a filled elastomer, with materials such as ceramic or boron nitride

employed as fillers depending on the thermal performance required [34]. These materials are cast and cured to a soft, conformable pad with a dough-like texture. Elastomeric pads are specially suited for applications that require electrical insulation between contacting surfaces as metal particles are seldom used as fillers. Thermal conductive $Al_2O_3$ or ZnO fillers and silicone rubber were utilised for the successful implementation of elastomeric thermal pads by Simet al.[36]. Zinc Oxide (ZnO) filled silicone rubber, manifested better thermal performance than $Al_2O_3$ filled silicone rubber. This can be attributed to ZnO's higher intrinsic thermal conductivity and lower intrinsic CTE value. Nonetheless, there is a reliability concern in the application of ZnO filled silicone rubber as elastomeric thermal pads. Consequently, in order to avoid significant degradation, with the application of small pressure to maintain good conformity at the interface, its uses has been limited to low power devices like chip sets [36].

Thermal pads require high pressure in order to reduce contact resistance. Typically, thermal pads have thickness in the range of 200-1000μm. They should at least be compressible to within 25% of their total thickness because of tolerance variation of large gap situations [34]. Increase in filler materials of thermal pads would improve thermal conductivity but could result to hardening of the pad which can reduce compressibility and boost thermal resistance [48].

Thermal pads can offer good thermal performance without the mess associated with thermal grease, handling of these materials is much easier than thermal grease. Hence, saves time by speeding up the assembly process. These materials at times have an inherent tack that aids placement during assembly [49]. Additionally, they are less likely to be pumped out of the space between the semiconductor package and heat sink/spreader base plate. Thermal pads can also act as a vibration damper and protect the electronic components from mechanical shock. The main disadvantage of thermal pad remains its high thermal resistance in the range of 1 – 3Kcm$^2$/W [39].

#### *2.2.1.3 Other Polymer-based TIMs*

In addition to the traditionally used thermal grease and thermal pads, in use, are other commercially available TIMs like Phase-Change Materials (PCMs), thermal gels, thermally conductive adhesive tapes and solders.

***Phase-Change Materials:*** These materials are usually made of suspended particles of high thermal conductivity, such as fine particles of a metal oxide and a base material [35]. Natural

material such as fully refined paraffin, a polymer, a co-polymer, or a mixture of the three can be used as base material [44, 50]. These base materials have a low melting temperature in the range of 50 – 90$^{o}$C [35, 39]. At room temperature, PCMs are solid and easy to handle. At phase temperature, PCMs change from solid phase to semi-solid (high-viscosity liquid) phase. In reality, these materials do not change phase but their viscosity is reduced which makes them flow like grease [51]. This allows the material to readily conform to both mating surfaces by completely filling the interfacial air gaps. Indeed, the development of PCMs seemed to be triggered by the limitations of thermal grease as elaborated in Table 2.2-1 (page 31) [34].

The low thermal conductivity of PCMs poses an enormous challenge in the design of efficient electronic cooling systems. However, it is beneficial that PCM has a low thermal resistance in the range of 0.3 – 0.7Kcm$^2$/W [39]. Like thermal grease, PCMs require additional barrier for electric isolation. Research is ongoing for various heat transfer enhancement techniques using PCMs.

***Gels:*** These are the fourth class of TIMs widely available in the market [52]. Gels typically consist of thermally conductive fillers (metal or ceramic particle) and silicone polymer with low cross–link density [34]. Silicone is usually employed as the base because of its unique properties including low modulus of elasticity, wetting characteristics and good thermal stability [31]. Gels typically show the properties of liquid and solid. In other words, it is like grease that can be cured [30]. These materials are like grease before cure, with high bulk thermal conductivities (2 - 5W/mK) [34]. Whilst after cure (post-cure), they are like cross-linked polymer with much lower modulus than pads [30]. Post-cure (like pads), gels offer temperature stability (no pump-out), cohesive strength and shape retention [52]. Like greases, gels show low modulus which means they can withstand thermo-mechanical stresses without interfacial delamination. According to a test result by Bischaket al. [52], while traditional thermal pads require 689-2068kPa to provide minimum thermal resistance, gel-based products typically need less than 137kPa for full substrate conformation. In addition, like grease, gels offer good wetting, can surround irregular shapes and stick on to intricate surface features. The thermal resistance of gels is in the range of 0.4 – 0.8Kcm$^2$/W which is comparable to that of grease [39].

***Thermal conductive adhesives:*** Thermal conductive adhesives are available both in liquid and solid form (double sided adhesive tape). The use of these materials eliminates the need

for mechanical attachment (i.e. screws, clips, rivets, fasteners) which can be a disadvantage when reworking may be required. Though these materials have unique properties of inherent bonding agent, they encompass poor thermal conductivity [35]. Its thermal resistance is relatively low in the range of 0.15 - 1Kcm$^2$/W[39].

### 2.2.2 Solder TIMs

Solders are widely used as TIMs to enhance heat conduction between two surfaces [53-67]. This can be attributed to solders' compliance both in the molten and solid state. Solder can melt in a low temperature and the molten solder can properly fill interstitial gaps between two mating surfaces, thus, result in improved interfacial thermal contact conductance. Furthermore, in metallic solid state, solder offer a high thermal conductivity. In comparison to the commercially available aforementioned TIMs, the overall thermal performance of solder is good evident in its lowest thermal resistance <0.05Kcm$^2$/W [39, 63, 68]as illustrated in Table 2.2-1. Hence, solder thermal interface materials (STIMs) appear promising for packaging power electronics as a result of their relative better thermal performance.

Solders used as TIMs (die-attach) can be classified into two groups[69]: hard solders and soft solders. Among the solders that melt below 400$^o$C, only the gold-based eutectics such as Au-12%Ge, Au-20%Sn andAu-3%Si qualify as hard solders. These solders exhibit high strength and are less susceptible to fatigue damage during thermal cycling. Nonetheless, they are relatively more expensive and can potentially transfer high stresses to the chip, which could lead to die fracture especially for small chips (<5mmx5mm) [70]. Hard solders are often employed for niche applications. Soft solders, including essentially all low-melting lead-, tin- and indium- based solders are less expensive and manifest low strength and high ductility. As such, these solders comparatively induce lower stress to the bonded silicon die but are generally characterised by fatigue cracking when subjected to thermal cyclic loading.

In addition to the fact that solders are generally prone to fatigue failures when subjected to temperature or power cycling. Experiments carried out on the failure mechanisms and reliability of solder as TIMs [57, 66, 71-74] has identified process-induced voids (Figure 2.2-4) as a major reliability concern in the use of solder as TIM. Voids (discussed in details in chapter 3) are one of the main manufacturing defects in solder joints of electronic assemblies and are easily formed during the manufacturing process. The recent transition to Pb-free solder has further exacerbated voiding concerns in the use of solder as TIM due to

reportedly[75] poor solderability of Pb-free solders which renders them more prone to voiding.

High-lead solders were very common in past years and often were used for high temperature environments such as automotive applications [76]. This is because of the relatively higher melting temperature of these high-lead solders compared to other soft solder alloys. However, the recent global effort to phase out lead (which is classified as a hazardous material) in electronic products has necessitated lead-free solders. The European Union legislation on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) [77], has banned the use of lead in electronic assembly industry due to health and environmental concerns. This legislation was implemented by the European Union on 1 July 2006, and forbid the use of Pb in electrical and electronic equipment in the commercial market. Consequently, research is on-going to find suitable replacement for Pb-based solder material. NEMI established the following criteria for selecting such Pb-free solder alloy [76]:

- The melting point should be close to that of Sn/Pb eutectic.
- Reliability potentials for Pb-free alloy should be equal to or better than Sn/Pb.
- Preferably, the alloy must be eutectic or at least very close to eutectic.
- The constituents of the alloy should be no more than three elements.
- If feasible, the use of existing patents should be avoided. This would facilitate ease of implementation.

Based on the aforementioned criteria, NEMI went on to recommend that the principal Pb-free solder alloy should be from the tin/silver/copper (Sn/Ag/Cu) family. Study on the thermal fatigue reliability of Sn/Ag/Cu solder alloy family as STIM will be presented in chapter 5.

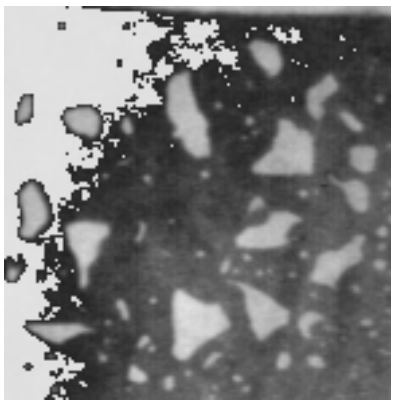


Figure 2.2-4: X-ray image showing solder voids. Void enclosures in the solder layer are visible as bright spots[64].

Table 2.2-1: Thermal Interface Materials properties [17, 31, 34-36, 39, 68, 78]

| TIM TYPE | Typical thermal resistance range ($Kcm^2/W$) | General characteristics | Advantages | Disadvantages |
|---|---|---|---|---|
| **Grease** | 0.2 - 1 | Form of thick paste composed of thermally conductive filler dispersed in silicone or hydrocarbon oil. | • High effective thermal conductivity<br>• Low thermal resistance as a result of thin Joint with minimal attach pressure<br>• Ability to fill interstices and reduce interstitial air<br>• No curing is required<br>• Delamination is not an issue<br>• Low cost<br>• Do not require shape cutting | • Not manufacturing friendly<br>• Pump-out as a result of thermal cycling.<br>• Can dry-out overtime<br>• Can be messy to handle<br>• Difficult to control thickness (uniform application)<br>• Usually do not provide electrical insulation. |
| **Pads** | 1-3 | Consist of a filled elastomer, with materials such as ceramic or boron nitride employed as fillers depending on the thermal performance required. | • Can be handled more easily<br>• Not messy<br>• Thermal compound is distributed uniformly on thermal pads.<br>• Conforms to surface irregularity before cure<br>• Less likely to pump out or leak out of the interface<br>• Resists humidity and can equally act as a vibration damper<br>• Can be easily cut to required size.<br>• Can be fitted with a thin layer of pressure-sensitive adhesive (PSA) to enhance adhesion at the interfaces.<br>• Can be compressed to absorb tolerance variation in assemblies | • Requires curing<br>• Thermal conductivity is lower than that of grease<br>• Delamination can be an issue<br>• Do not have free flow movement<br>• Permanent clamping required<br>• More expensive than grease<br>• Require high contact pressures to conform to mating surfaces<br>• Require high contact pressures to fill voids<br>• Increased thermal resistance as a result of inadequate pressure |
| **PCMs** | 0.3–0.7 | Made of suspended particles of high thermal conductivity, such as fine particles of a metal oxide and a base material. Natural material such as fully refined paraffin, a polymer, a co-polymer, or a mixture of the three can be used as the base material. | • Increased stability and less vulnerability to pump-out<br>• Easier to handle compared to greases<br>• No cure is required<br>• Delamination is not an issue<br>• No dry-out<br>• Ability to conform to profiles of mating surfaces | • Lower thermal conductivity than greases<br>• Limited thermal performance as a result of "phase-change" (polymers and filler combinations) trade off.<br>• Surface resistance can be greater than greases. This can be reduced by thermal pre-treatment<br>• Compressive force required which can cause mechanical stresses<br>• Additional barrier is required for electrical isolation |
| **Gels** | 0.4 – 0.8 | Consist of thermally conductive fillers (metal or ceramic particle) and silicone polymer with low cross–link density. | • Offer properties of solid and liquid<br>• Good wetting capabilities<br>• Able to surround irregular shapes<br>• Adhere to complex surface features<br>• Good shape retention<br>• High cohesive strength<br>• High temperature stability<br>• No pump out or migration concerns | • Cure process required.<br>• Lower thermal conductivity compared to grease.<br>• Delamination can be a concern. |
| **Thermal adhesives** | 0.15-1 | Available both in liquid and solid form (double sided adhesive tape). | • No pump out.<br>• No migration.<br>• Do not require mechanical clamp.<br>• Conform to surface irregularity before cure | • Cure process required<br>• CTE variation induced stress is a concern. Since cured epoxies have modulus.<br>• Delamination post reliability test is a concern. |
| **Solders** | <0.05 | Offer compliance both in the molten and solid state. Can be independent of polymers. | • High thermal conductivity<br>• Low thermal resistance | • Voiding is a concern<br>• Complexity in processing<br>• Rework challenges<br>• High cost |

## 2.3 Emerging nanotechnology in TIMs

The unique properties of one dimensional structure and materials have gained much attention in recent years for thermal management applications. Among such materials, carbon-nanotubes (CNTs) and carbon nanofibres (CNFs) seem promising TIMs owing to their special structural, mechanical and more importantly thermal properties [47, 79-81]. The inherent thermal conductivity properties [79, 82] of CNTs are excellent, and the ability to fabricate them in a controlled manner has been instrumental in realizing their potentials. Since the discovery of Multi-Walled CNT (MWNT) in 1991 by Iijima [83] and Single-Wall NanoTube (SWNT) in 1993 by Iijima and Ichihashi [84] and Bethunes et al. [85], significant effort has been devoted to understanding and characterizing their properties. The most interesting properties of CNTs are the ballistic transport of electrons and the extremely high thermal conductivity along the tube axis [79, 86]. Also, phonons propagate easily along nanotubes [87]. Reported values of thermal conductivity are shown to be as high as 3000 W/mK [80, 88-89] and 3500W/mK [90] for a MWNT and SWNT, respectively, at room temperature. Carbon nanofibres grown from chemical vapour deposition (CVD) were measured to have a thermal conductivity in the range of 35 W/mK which increased to 2000 W/mK following annealing at 3000$^{o}$C [91-92]. Many of these values are comparable or even higher than that of diamond [93], giving them the greatest thermal conductivity of any known material. Many research works have already been published and patents filed on CNTs and CNFs potentials as TIM, some of which have been referenced in this chapter [94-97]. Unsurprisingly, recent findings have shown that CNT-based interfaces can significantly conduct more heat than comparable state-of-the-art commercial TIMs at the same temperatures as shown in Figure 2.3-1. CNTs/CNFs can be employed as TIM fillers or TIM structure.

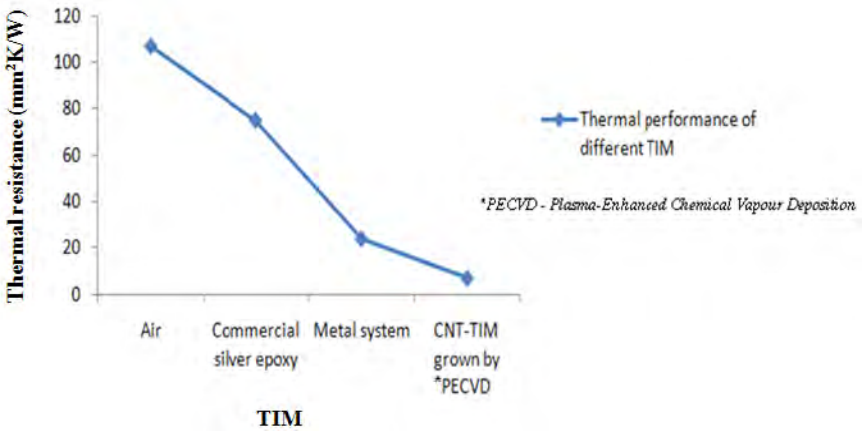



Figure 2.3-1: Measured total thermal resistance of different TIMs[98]

### 2.3.1 CNTs as fillers

The discovery of high thermal conductivity in CNTs and CNFs has emanated suggestions that they could be employed as highly heat conductive fillers to improve thermal conductivity of TIMs. Many works [94, 99-104] have been carried out in this regard. Remarkable improvements in the thermal conductivity of the TIM were achieved in each application. For instance, Hu et al. [102] employed the combination of CNTs and traditional thermal conductive fillers for TIMs. They accomplished a thermal conductivity value seven times that of the base material, approximately double the thermal conductivity of the equivalent TIM composite with only conventional fillers. Though the thermal conductivity of TIM could be improved by CNTs inclusion, Hu et al.[2] and Zhang et al. [105] suggest that the potential heat conduction of CNTs is not fully optimised when employed as fillers. The low efficiency could be as a result of firstly, the random dispersion of CNTs, which means that heat conduction is only through few portions of CNTs by effect. Secondly, heat is not directly conducted from one side to the other via CNTs. As a result of CNTs' small diameter, CNTs are discontinued by other lower thermal conductive fillers or the base fluid which could deteriorate the thermal performance of the CNT composites [2]. The evolution of aligned CNT array as a better choice for TIM's basic structure is therefore not surprising.

### 2.3.2 CNT arrays

Carbon-nanotube array interfaces are promising candidates for improved TIM of high power devices which can be attributed to their excellent compliance and high thermal conductivity[106]. The use of CNT arrays in an aligned manner has attracted much interest in recent times because they possess the highest value of thermal conductivity along their axis [107]. In this approach, vertically aligned CNTs is placed in the interface between the metallic heat sink such as aluminium and microelectronic devices (Figure 2.3-2). The overall heat conduction is determined by the thermal conductivity of the CNTs themselves and the thermal conductance at the two surfaces at the two ends (electronic components and heat sink devices) of the CNTs. Many works [2, 45, 82, 98, 105-111] propose that CNT arrays when employed as interface materials offer improved thermal management due to their ability to significantly aid heat conduction with relatively high effective thermal conductivities (~ 80 W/mK). However, to fully realise the unique thermal properties of aligned CNTs array, more research is ongoing. The most challenging issue is attaining thermal contact between surrounding surfaces and vertically oriented CNTs/CNFs [31, 37, 112] as shown in Figure 2.3-3.

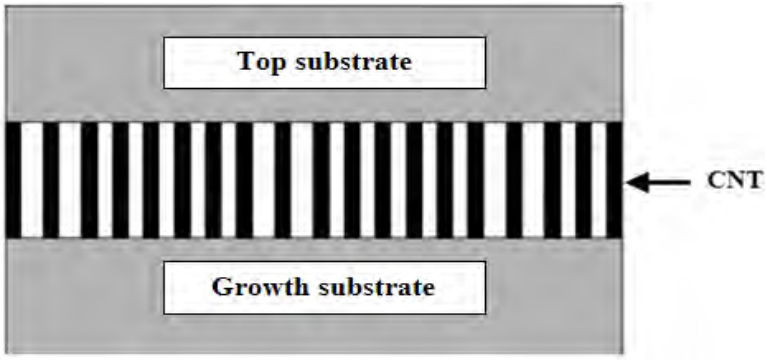



Figure 2.3-2: Schematic diagram of CNT array grown in the back of a substrate

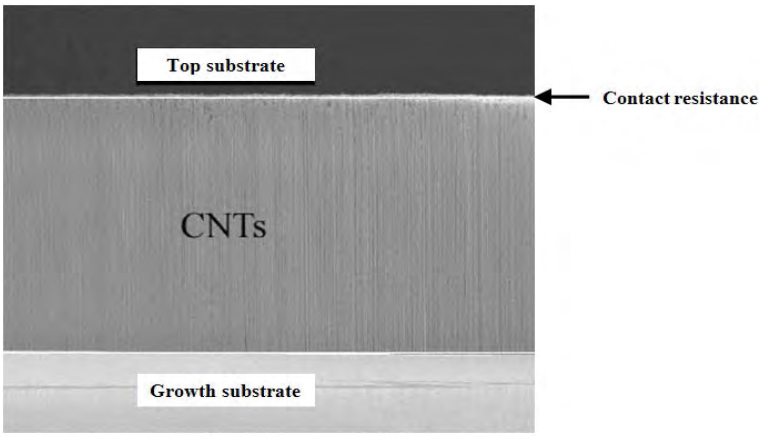



Figure 2.3-3: SEM images of an aligned CNT film showing contact resistance[43]

The poor thermal/mechanical contact could be as a result of variations in the length of CNTs/CNFs resulting in increased thermal resistance between mating surfaces as evident in Reference [113]; where short nanofibres gave an estimated thermal conductivity which is several orders of magnitude less than that of long nanofibres (see Table 2.3-1). Ngo et al. [47] demonstrated how improved mechanical contacts can be achieved by increasing attachment pressure and gap-filling CNT arrays through copper electro-deposition. They created a CNF-Cu composite array by gap-filling copper between vertically aligned carbon nanofibres (VACNFs) as illustrated in Figure 2.3-4. This offers a suitable mechanical anchor for the nanofibres to the substrates and also provides lateral heat spreading. Values of thermal resistance as low as 0.25cm$^2$ K/W for pressures approaching 413kPa were obtained with the contact measurement technique they employed. Though improved mechanical contacts can be achieved by increasing attachment pressure and gap-filling, other key concerns like constriction effects and acoustic mismatch at the contact points may not be addressed with increased pressure [2].

Table 2.3-1: Interfacial thermal resistance of materials explored by Chuang et al. [113].Errors represent the standard deviation of several measurements made on each sample

| Material | Thermal resistance (K-cm$^2$/W) |
|---|---|
| *PECVD Nanofiber (long) | 2.7 ± 0.2 |
| PECVD Nanofiber (short) | 12.3 ± 0.1 |
| *PECVD MWNTs | 3 ± 0.8 |
| *ThCVD MWNTs | 2.5 ± 0.7 |

**PECVD – Plasma enhanced chemical vapour deposition*

**ThCVD – Thermal chemical vapour deposition*


Figure 2.3-4: (a) SEM micrograph of as-grown CNF array taken at 45° viewing angle. (b) Copper gap-fill using chromium and (c) copper gap-fill using titanium as the working electrode [47]

A few practical solutions exist to reduce the effect of the total contact thermal resistance without an overall increase in attachment pressure [2]. Firstly, is the combination of dry CNT arrays with other conventional TIMs that offer high wetting properties, including PCMs [45, 97] and thermal greases [102].Xu and Fisher [45] have reported the least resistance values of 19.8mm$^2$K/W and 5.2mm$^2$K/W for copper-silicon interfaces with dry CNT arrays and PCM-CNT arrays, respectively, under moderate pressure. Secondly, is the growth of vertically orientated CNTs on both of the contact surfaces to form an interwoven mesh (cross-talk interface) [82, 114] as shown in Figure 2.3-5. Carbon-nanotube array interfaces have been reported to produce thermal resistances as low as 8mm$^2$ $^o$C/W and 4mm$^2$ $^o$C/W (similar to that of a soldered joint), for arrays grown on one side [115] and both sides [108] of surface, respectively, under moderate pressure. Hu et al. [2] suggested that the "brush-brush" contact thermal conductance between two free MWNT arrays could be quite low resulting in an increase in thermal resistance. The CNT transfer processes demonstrated by Zhu et al. [43]

and Tong et al. [116] seem promising as regards eliminating the “brush-brush” thermal contact resistance. Zhu et al. [43] employed a conventional solder reflow process (peak temperature at 250$^{o}$C) for the assembly of open-ended CNT structures aligned to a eutectic tin-lead solder paste deposit printed on a copper substrate as shown in Figure 2.3-6**.** The superb mechanical bonding strength on the CNT and solder interfaces should effectively assist in the reduction of the thermal contact resistance. They reported a thermal conductivity and thermal resistance of 81W/mK and 0.43cm$^{2}$K/W, respectively, for the assembly with CNT height of ~180μm. Tong et al. [116] demonstrated the CVD growth interface of MWNT-Si and MWNT-glass using indium to uniformly bond the whole MWNT top surface to the glass. They revealed that such contact has an overall thermal conductance about an order of magnitude higher than the measured thermal conductance for the direct contact MWNT-glass interface. It should be noted that an insulating layer like mica could be used to provide electrical isolation if required when CNT is employed as TIM [52].

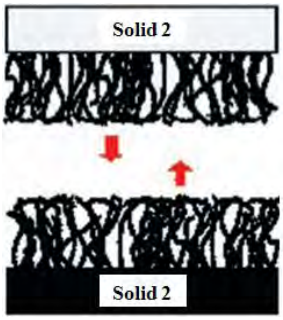



Figure 2.3-5: Schematic diagram of CNT array grown at two surfaces[12]

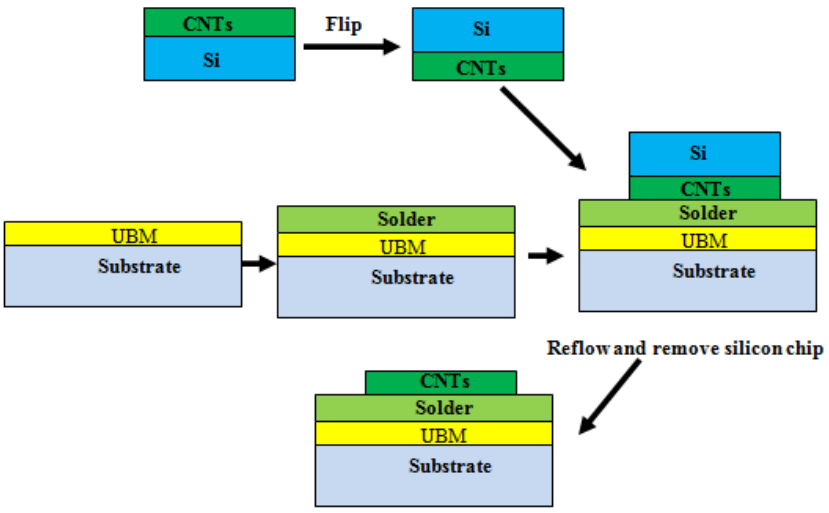



Figure 2.3-6: Schematic diagram of the "CNT transfer technology" for assembling aligned open-ended CNT films

### 2.3.3 CNT mechanical properties

Carbon-nanotubes, besides their outstanding thermal properties, are known to offer extraordinary mechanical properties [117-121]. Thus, CNTs could be exploited to address the key challenges emanating from the use of polymer-based TIMs (such as dry-out over time, pump-out during cyclic thermal loading and non-uniform applications) and STIMs (like solder voids and fatigue failure). Works [118, 122-124] have shown that nanotubes can sustain large strain deformations such as twisting and buckling without showing signs of fracture, they have the intriguing capability of returning to their near original, straight, structure following deformation as shown in Figure 2.3-7. Such behaviour is highly unusual and could play a significant role in increasing the energy absorbed during deformation of CNT-filled composites during high temperature loading [117]. Ajayan [117] reports that despites CNT's high elasticity and high conductivity, it is one of the strongest materials and often robust in most harsh environments. CNT array [125-130] and CNT-based polymer composites [104, 131-143] have been largely studied for their mechanical strength and visco-elastic properties.

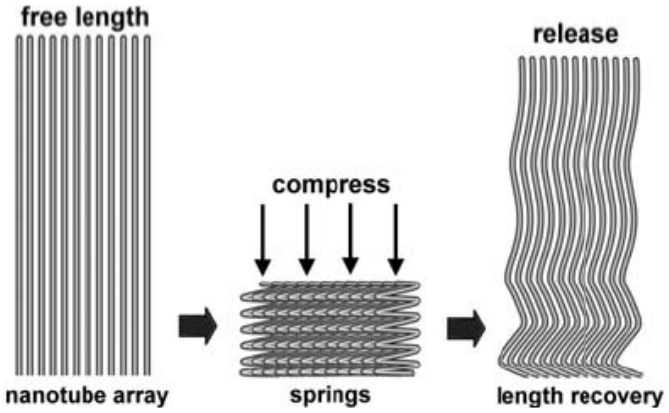



Figure 2.3-7: Compression testing of aligned CNT films. A schematic illustration shows a CNT array compressed to folded springs and then regaining the free length upon the release of compressive load [130]

Vertically aligned CNT arrays create parallel paths across mating surfaces with each path containing one CNT and two junctions at top and below surfaces. Hence, this maximises thermal conductivity of CNT array and enhances temperature stability (no pump-out). Suhr et al. [129] showed that long, vertically aligned MWNTs manifested viscoelastic behaviour analogous to that observed in soft-tissue membranes under repeated high compressive strains. The mechanical response of the CNT arrays showed preconditioning, characteristic viscoelasticity-induced hysteresis, nonlinear elasticity and stress relaxation, and large

deformations, under compressive cyclic loading. Additionally, Suhr [129] did not observe any fatigue failure at high strain amplitudes up to half a million cycles. Cao et al. [130] reported that free standing films of vertically aligned CNTs exhibited super-compressible foam-like performance. Under compression, the CNTs collectively formed zigzag buckles that could fully unfold to their near original length upon release of load resulting in a strong cushioning effect (Figure 2.3-8 and Figure 2.3-7). Compression stress-strain curves also manifested large hysteresis, indicating substantial energy loss (damping) which might be as a result of the friction between the CNT surfaces when in motion [130]. References [125-128] have also reported good mechanical responses and significant level of energy dissipation of CNT arrays under high-strain rate deformation.

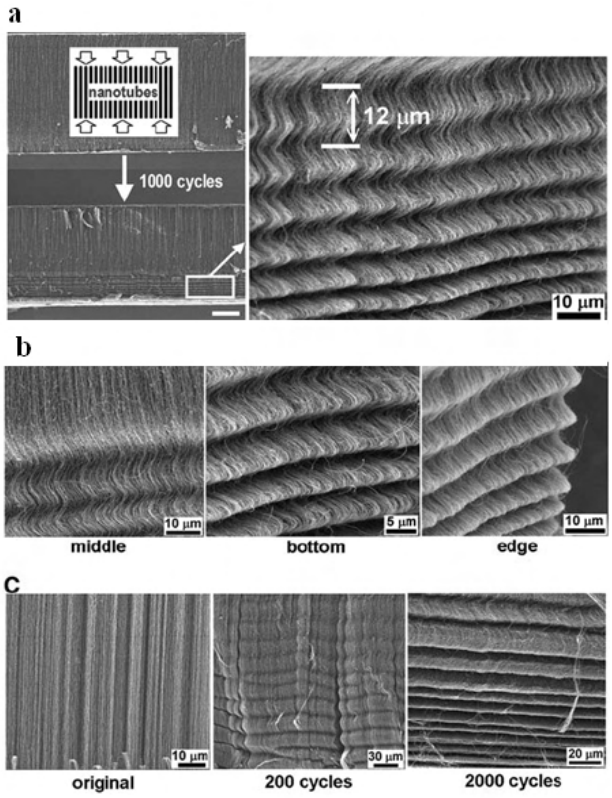



Figure 2.3-8: SEM characterization of buckled CNTs under compression.(a) SEM of an original freestanding film (left, top) (thickness 860 mm) and a compressed film (left, bottom) (ε = 85%, 1000 cycles), with a reduced thickness of 720 mm, showing horizontal lines (wavelike buckles) uniformly distributed across the film section. Left scale bar, 200 mm. (Left, inset) Illustration of compression along the axis of nanotubes. (b) Slight buckles in the middle section, heavy buckles (almost completely folded) near the bottom of film, and the zigzag edge of the compressed film. (c) SEM image of a 1.2-mm-thick film before and after compression, showing the evolution of buckles with increasing compression cycles [130].

Nonetheless, in the as-grown state, aligned CNT films are only held together by weak van der Waals forces [144] and the substrate resulting in fragile adhesion between the tubes. This leaves pure CNT arrays with low resistance to shear and prone to splitting [145] when a stress is applied. No wonder there has been a recent exploitation of CNT-based composites (with interest in matrix materials such as polymers, ceramics and metals). CNT-polymer composites enhance stress distribution of the composite film through load transfer from the polymer to the CNT network [145]. Some experiments [104, 132-143] have provided valuable insights into the mechanical characteristics of CNT-reinforced polymers, though with conflicting reports at times on the interface strength in CNT-polymer composites. Teo et al. [145] demonstrated a hybrid film consisting of CNTs and amorphous diamond (a-D). This unique structure referred to as carbon-based nanomattress encompassed extraordinary mechanical and viscoelastic properties. It exhibited good thermal performance (high temperature stability) and could protect components from mechanical vibration and wear [145]. Nanotube reinforcements have also resulted in an increase in the toughness of the nanotubes-based ceramic matrix composites by absorbing energy during their highly flexible elastic behaviour [146-147] under compressive loads.

The aforementioned studies indicate that CNT arrays and composite materials could potentially be employed as intrinsic damping materials coupled to its thermal management capabilities. These unique properties of CNTs are crucial for CNT-based TIMs especially for the high temperature and harsh under-hood automotive ambient applications. Future research should be focused on understanding the long term reliability and performance degradation of CNT-based TIMs when exposed to cyclic temperature loading. Such data appears to be lacking in the literature.

### 2.3.4 CNT fabrication

Among the various means of CNT synthesis, Chemical Vapour Deposition (CVD) appears the most promising method for industrial-scale production [43, 79, 148]. This can be attributed to CVD's price per unit ratio and its capability to grow nanotubes directly (well aligned) on a desired substrate [43, 79, 105-106, 109, 149]. However, direct synthesis of CNT array interfaces is a concern. This is because the temperatures at which these CNT array thermal interfaces are grown (>800 $^{o}$C) may be too high for temperature-sensitive packages employed in the assembly processes of standard electronic device. Apparently, the electrical and mechanical performance of most metal contacts and interconnects degrades when exposed to high temperatures up to 450$^{o}$C for more than a limited time [148]. Cola et al.

[109] proposed an insertable CNT array/foil as a viable method to apply CNT arrays to an interface without exposing mating materials to adverse CNT growth temperatures. This technique seems promising considering the low thermal resistances ($10mm^2\ ^oC/W$) achieved under moderate pressure. Zhu et al. [43] developed a CNT transfer process which is similar to flip-chip technology as shown in Figure 2.3-6. They employed a conventional solder reflow process (peak temperature at $250^oC$) for the assembly of open-ended CNT structures aligned to a eutectic tin-lead solder paste deposit printed on a copper substrate. This CNT transfer technology enables the separation of the high temperature CNT growth and the low temperature CNT device assembly. References [148, 150-152] reported other progress in low temperature growth of CNT arrays. These low temperature synthesis approaches appear advantageous for their ability to be incorporated into existing manufacturing processes and their good thermal interface conductance. For instance, CNT arrays can seamlessly be grown at low temperatures on sensitive substrates.

### 2.4 Challenges facing TIMs applications

Thermal grease is predominantly employed in automotive applications which can be attributed to its low thermal resistance, low cost and ability to fill interstitial gaps between mating surfaces [40]. Nevertheless, their reliability and suitability for automotive applications is yet to be established especially for under-hood automotive environment considering the pump-out and dry-out effects associated with thermal grease (Figure 2.2-1 and Figure 2.2-2) [40, 153]. Thermal pads were developed as alternative TIMs considering their inherent manufacturing benefits coupled to their provision of interfacial electrical isolation. Thermal pads are however limited to low and medium power devices application as a result of their intrinsic high thermal resistance and reliability concerns [34, 39]. Therefore, thermal pad is not a good option for high power electronics. Phase-Change Materials is a technology furnished to encompass a combination of the thermal properties of thermal grease and the ease of assembly associated with thermal pad. PCMs manifested good reliability and high-performance (can withstand mechanical shock and vibration) in a reliability test carried out by Viswanath et al. [34]. Nonetheless, it was shownby Prasher [68] and Mirmira [154] that the performance of a PCM degrades when exposed to elevated temperature over a period of time (thermal aging) as illustrated in Figure 2.4-1. Prasher and Matyabus [155] in a separate study related the pump out problem of grease to the ratio of storage shear modulus (G') and loss shear modulus (G''). They suggested that G' of grease should be greater than G'' in order to avoid pump out [155]. This perhaps necessitated the development of Gel TIM. Gel is

in essence just cured grease [68]. Confocal Scanning Acoustic Microscopy(CSAM) analyses by Wakharkaret al. [156] revealed that TIM formulations that lack a gel point, such that G'/G" < 1, appear to form voids due to pump out akin to those observed in grease under temperature cycling ( see Figure 2.4-2 for a representative image). Further results by Wakharkar [156] showed that while TIM formulations that lack a G'/G" crossover rapidly degrade during temperature cycling, gel TIMs with G'/G" > 1 in essence showed the same degradation rate during thermal cycling (Figure 2.4-3). Hence, one of the primary challenges for gel TIM formulation remains the optimisation of the mechanical properties such that the cured gel absorbs the thermo-mechanical stresses emanating from the CTE variations of the mating surfaces [155].

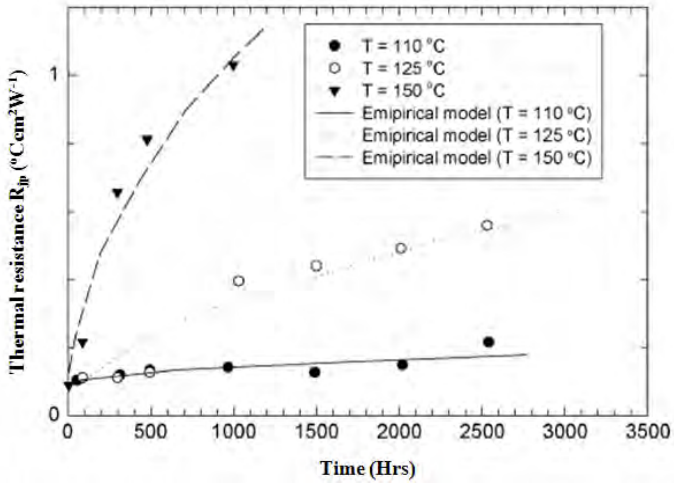



Figure 2.4-1: Degradation of thermal resistance of PCM with time[68, 154]

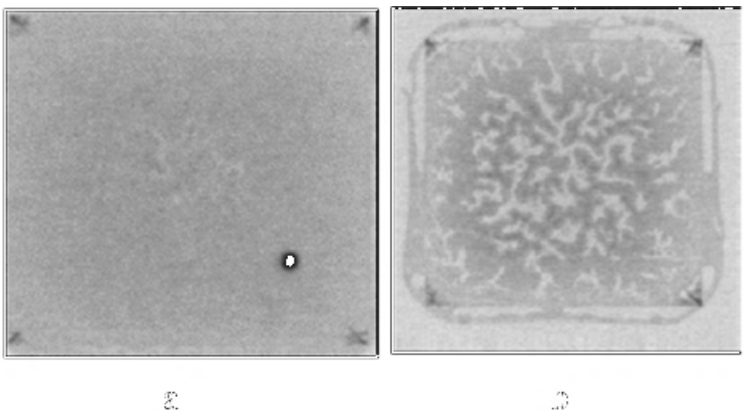


Figure 2.4-2: CSAM images before (a) and after (b) reliability stressing showing the formation of voids in a gel TIM lacking a G'/G" crossover [156], voids are shown in the TIM layer as visible bright spots

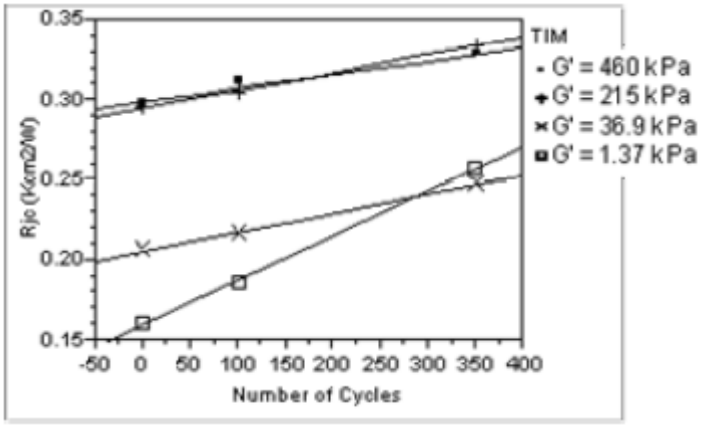



Figure 2.4-3: Plot of mean thermal resistance ($R_{jc}$) vs. number of temperature cycles. The slopes show the degradation rate of the material during temperature cycling [156]

Given the foregoing, it appears that polymer-based TIMs degrade when exposed to temperature excursions [96] and therefore a concern especially when the harsh under-hood ambient in automotive is into consideration. STIM is not susceptible to dry-out/pump-out effect and relatively manifests the least thermal resistance (as shown in Table 2.2-1) compared to its polymer-based counterparts. Thus, STIM appears promising for packaging power electronics due to its improved performance in comparison to commercially available polymer-based TIMs. However, solder joints are generally susceptible to voiding which could impact the reliability of STIMs. Thus, voiding remains a key concern in the application of solders as TIMs and will be discussed in more details in the next chapter (Chapter 3).

It is worth noting that the discovery of CNTs potentials as TIMs owing to their high thermal conductivity values in axial direction stands out as the most recent development to improve TIMs' efficiency. Nonetheless, CNT technology is still underdeveloped. Further practical approaches and extensive modelling must be found to characterize the performance degradation of CNT based TIMs in order to realize the promise of high thermal conductivity of CNTs with expected reliability. Undoubtedly, the development of affordable synthesis techniques is also vital to the future of carbon nanotechnology especially in the automotive industry. As with every other technology in its infancy, CNT application as TIMs may recently seem more complex and costly than the conventional TIMs; however, it is important to know that CNT concept as TIM has good potentials and could lead to various creative/novel ideas that would be favourable in terms of cost and manufacturability. Indeed, there is much development space for the CNT assembly as TIMs.

## 2.5 Summary

Thermal interface materials play vital role in the overall thermal management of electronic devices. This chapter presented a review of various classes of TIMs that could be applicable to ECU. Polymer-based thermal interface materials including thermal grease and pads are the conventional technologies for attaching the heat generating electronic device to heat sink; however, these traditional materials encompass poor thermal performance and account for the largest thermal resistance in the electronic package. The review identified Solder thermal interface material (STIM) as a promising feasible technology to package high performance power electronics due to its better thermal and mechanical performance compared to the conventional polymer-based TIMs. Nonetheless, voiding (discussed in details in the next chapter) remains a major reliability concern of STIMs coupled with the fact that solder joints are generally prone to fatigue failure under exposure to thermal cyclic loading. Further practical approaches and extensive modelling must be found to characterize the performance degradation of CNT based TIMs in order to realize the promise of high thermal conductivity of CNTs with expected reliability.

# Chapter 3: Literature review 2 - Solder voids

## 3.1 Introduction

Solder voids are defined as cavities and bubbles in a given solder joint. As highlighted in chapter 2, though STIMs relatively appear to offer improved performance compared to their polymer-based counterparts, voiding has been identified as one of the major reliability concerns in the use of solder as TIMs.

This chapter initially presents the various categories of voids in electronics interconnects with emphasis on process-induced solder void which is the focus of the current work. Subsequently, overviews of the critical parameters that contribute to the formation of process-induced voids are given. This is followed by the highlights of available industry standards for the inspection of process-induced voids. Then, literature reviews on the effect of process-induced voids on the mechanical and thermal performance of solder joints are discussed. The gaps identified from the literature review that requires further attention are then presented before the summary of the entire chapter is finally given.

## 3.2 Categories of voids that exist in electronic interconnects

At least three categories of voids exist in electronics interconnects. The first type known as Kirkendall voids refers to voids that are formed due to difference in diffusion rates of different elements (such as Copper (Cu) pad and Sn-rich solder). The element with a faster diffusion rate dissolves into the other leaving behind some tiny voids in the process; in the aforementioned example, Cu diffuses much faster in Sn than Sn does in Cu leaving behind atomic vacancies and depletion sites in the copper layer. The nucleation of this vacancies form Kirkendall voids (as shown in Figure 3.2-1) inside the inter-metallic (IMC) layer. These voids grow with thermal ageing as a result of the increase in IMC growth rate. Hence, Kirkendall voids often occur at the interface of the two elements and cannot be detected with an X-ray machine. Kirkendall voids can be observed by cross-sections and scanning electron microscopy (SEM) [157].

The second type of void are voids that coalesce and grow as a result of grain boundary sliding during accumulation of fatigue damage due to temperature cycling or power cycling. Intrinsically, the grain structure of solder is unstable [158]. The grains would potentially grow in size with time as the grain structure cushions the internal energy of a fine-grained structure. This process of grain growth is enhanced by high temperatures and strain energy input during cyclic loading. Hence, the grain growth process indicates the accumulation of fatigue damage. In lead-based solders, contaminants like lead oxides could be concentrated at the grain boundaries as the grains grow, thereby weaken these boundaries. Consequently as

schematically shown in Figure 3.2-2, after the elapses of ~25% of the fatigue life, micro-voids would potentially begin to form at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks eventually coalesce into macro-cracks and could lead to total fracture of the solder layer [159].

The third type of voids which is the focus of the present work is relatively larger voids referred to as the process-induced/manufacturing voids (Figure 3.2-3). These voids occur during the manufacturing processes and are classified as manufacturing defects. The advancement to lead-free solders has even escalated concerns emanating from process-induced voids due to its comparatively poor solderability [15]. Studies have reported the occurrence of these voids in excess of 50% of solder joint volume in some Pb-free solders [16,17]. In other words, these voids could cover up to 50% area of a solder joint [160] and could even be more detrimental to flip-chip package solder interconnections because of the relatively smaller size of the package. Process-induced void poses a concern to the mechanical and thermal performance of STIMs as will be properly discussed in Section 3.5. It has been reported that these voids in lead-based solder interconnection of ignition modules can result in automotive engine failures [161]. Moreover, these voids are unfortunately almost unavoidable in solder joints during the manufacturing process as a result of the complexities and interactions associated with the many factors that affect the voids formation. Therefore, it is imperative to study and evaluate the influence of manufacturing voids on the performance of STIM.

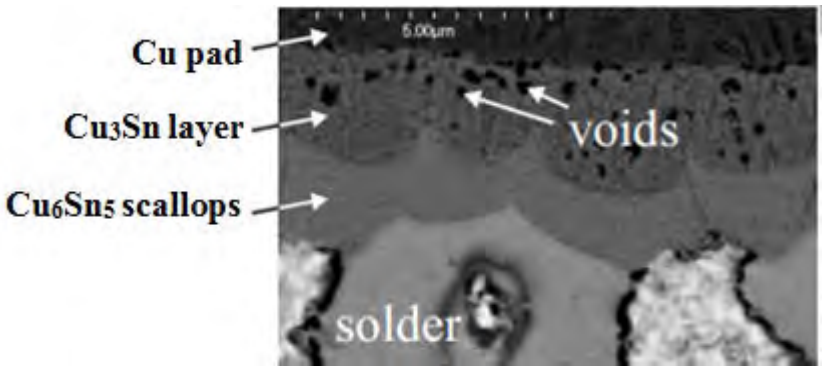



Figure 3.2-1: Micrograph showing Kirkendall voids in the interface region between the solder and Cu pad [162]

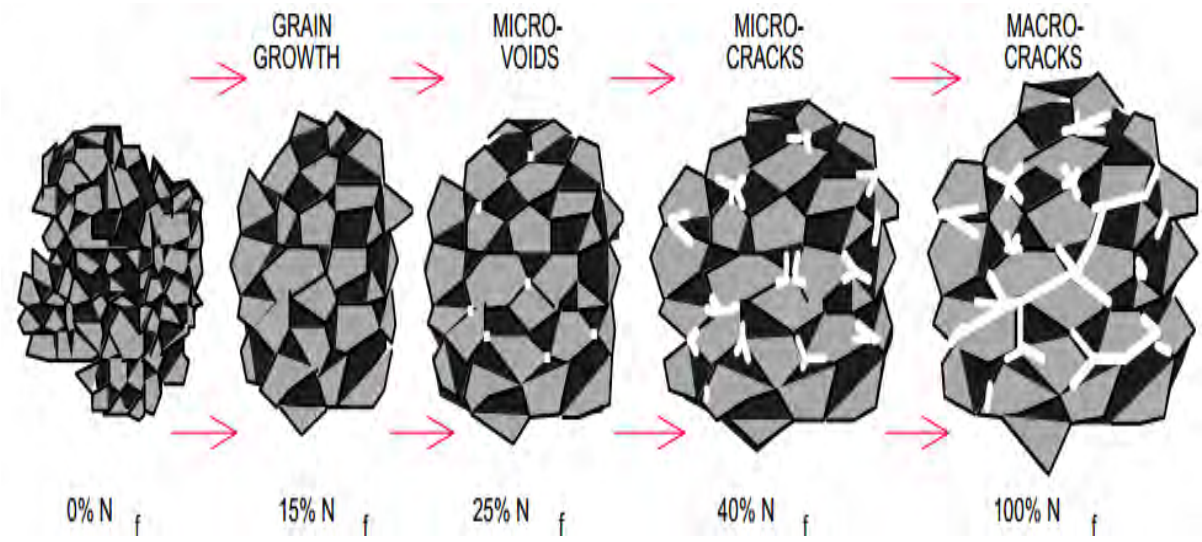



Figure 3.2-2: Depiction of the effect of accumulation of fatigue damage on micro-voids[159]

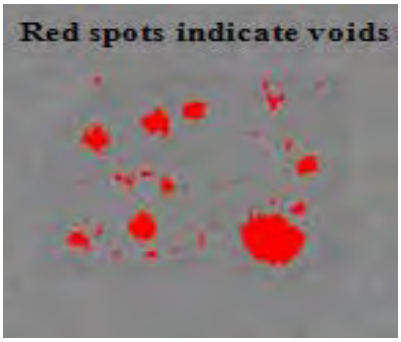



Figure 3.2-3: X-ray image showing voids in solder die-attach. Void enclosures in the solder layer are visible as red spots

## 3.3 Critical parameters that contribute to the formation of process-induced voids

It has been reported [163-164] that process-induced voids mainly occur during manufacturing due to:

- The entrapment of gas bubbles formed by reactions occurring between materials including fluxes during the reflow soldering process.
- Poor wetting of solder due to defective or contaminated backside metallisation of the silicon die or heat spreader/sink.

Furthermore, over the years, researchers have classified the factors that can lead to the formation of void during the manufacturing processes into four categories – methods/machine, materials, human factors and environment [165] (Figure 3.3-1).

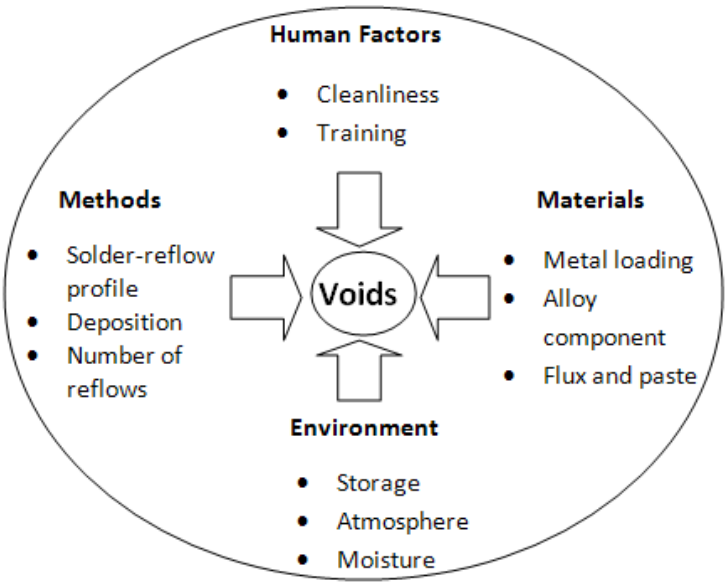



Figure 3.3-1: Factors contributing to void formation

The four factors and their sub-categories have been fully explained in literature [165-166] and hence only a brief overview of the critical parameters in electronic assembly is presented in this section.

### 3.3.1 Methods/Process

The method of assembly which usually includes reflow profiling is a critical parameter that contributes to void formation.

***Reflow profile***

Reflow is a very crucial process in the assembly of electronic components. Reflow soldering can be done using different methods such as forced convection reflow, infrared reflow and in-line conduction reflow[167]. In reflow soldering, the temperature of the solder paste/preform is raised until the solder melts and forms a joint, after which the temperature is slowly decreased to room temperature. At times during reflow soldering, an inert gas such as nitrogen ($N_2$) is employed to prevent solder oxidation. Typical reflow process consist of several steps which include preheat, soak, reflow and cool. These steps are schematically depicted in Figure 3.3-2.

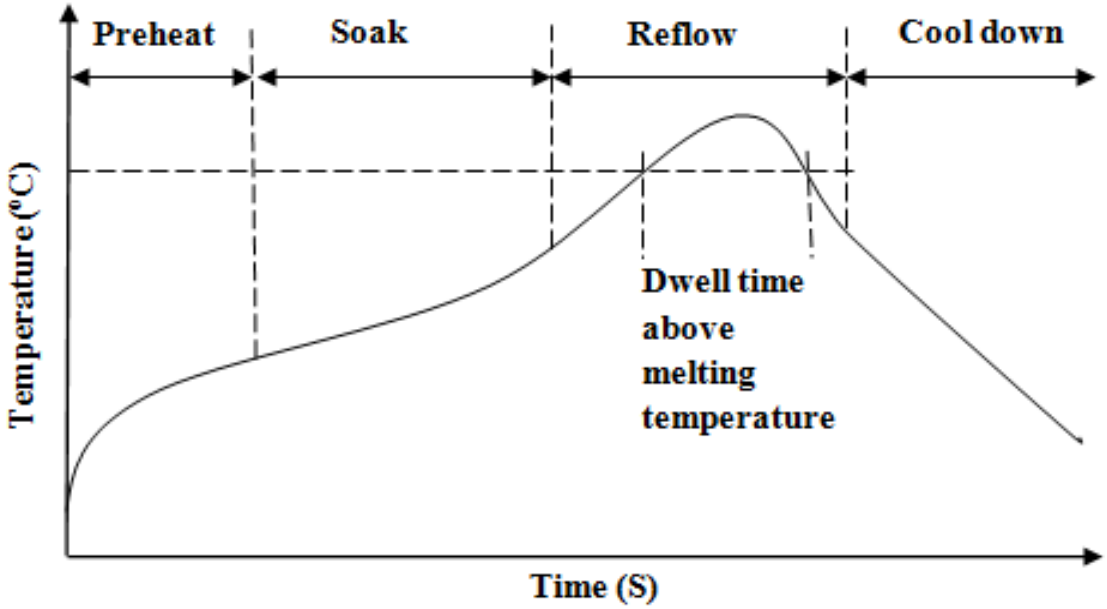



Figure 3.3-2: A typical Ramp-to-Spike reflow profile

During the preheat step, temperature is gradually and uniformly raised on the board in order to reduce excessive temperature gradients. Soak comes after preheat with the main goal of this step being to evaporate solvents and activate flux. Also, soak step assists to further equilibrate the temperature across the electronic component before proceeding to the reflow step. In the reflow zone, the temperature of the solder is increased until it melts and then the solder is left in the molten state for a certain time to achieve good wetting and intermetallic formation with other metals. Reflow temperatures depends on the melting temperature of the solder, solder composition, solder manufacturer's guide and the type of reflow oven used. Cooling is the last step in the reflow process. A higher cooling rate often results in finer grain and shinier joints. Fast cooling rate is usually not recommended in order to avoid thermal shock.

The impact of reflow profile on voiding will be discussed based on outgassing control and wetting control. This is because void content can be reduced by decreasing the outgassing rate and improving the solder wetting ability.

***Outgassing control***

Generally, as temperature rises, the rate of outgassing of virtually all fluxes increases initially and then gradually decreases after reaching a certain peak point [168]. Ideally, the reflow profile should be preferred in such a manner that the reflow process is completed before major outgassing begins and the volatiles are dried out before the solder melts. While a low

peak temperature would promote the reduction of outgassing when the solder is in a molten state, a long, hot soaking would enhance the elimination of volatiles.

***Wetting control***

A reflow profile with high temperature and long-time appears favourable. This is because fluxing reaction increases with elevated temperatures and long times and an increase in fluxing reaction improves wetting which in turn can reduce voiding. Nonetheless, care should be taken when increasing the temperature as wetting behaviour can be impeded by flux loss and oxidation which happens when the flux dries out as a result of high increase in the reflow temperature. The optimal reflow profile should be balanced considering both outgassing and wetting as parameters.

### 3.3.2 Human factors

Human error including input from operators is one of the factors that can contribute to void formation during the manufacturing process. Such human factors include handling and training.

***Handling and cleanliness***

Inappropriate handling (manual and/or automated) of the components and machines during manufacturing process can have a negative impact on the integrity of the electronic assembly. This issue is even more critical when the manufacturing process is not automated. Voids could occur at the surface between the solder layer and metallised silicon die or heat spreader as a result of poor solder wetting due to contamination of the backside metallisation of the die and/or substrate during manufacturing.

**Training/education**

It is essential to properly train the operators in order to minimize human errors during the manufacturing processes. Operators should be familiar with the overall manufacturing and assembly process as any mistakes from their side can result in manufacturing defects such as voids. Voids could occur at the surface between the solder layer and metallised silicon die or heat spreader as a result of poor solder wetting due to defective/improper backside metallisation during manufacturing.

### 3.3.3 Materials

The forming of a good solder joint requires the right solder alloy, flux and of course heat.

***Solder reaction with substrate***

Solder that can readily react with base metal to form inter-metallic compound enhances mixing between the solder and base metal at the atomic level. This subsequently improves solder wetting and thereby decreases the potential of void occurrence. The surface tension of the solder also plays a key role in the course of solder joint formation and the impact of solder surface tension on voiding is twofold. Firstly, solder with a low surface tension spread more easily and as a result could reduce voiding by easily removing trapped flux from within the solder joint. Secondly, solder alloys with low surface tension has a low resistance to joint volume expansion caused by the presence of void [168-169].

***Solder powder size and metal content***

Void content increases with decreasing solder powder size and increasing solder metal content [168]. The latter is partly attributed to an increase in solder powder oxide which results to a high level of outgassing due to a greater fluxing reaction while the former is as a result of the increase in surface area and oxide level associated with reduced powder size.

***Flux***

Oxides form at a significant rate on the surface of heated metals when soldering. The occurrence of voids increases with the oxidation of solder or substrate. Nonetheless, low voiding could be achieved when a high activity flux is employed; a high activity flux efficiently removes oxide thereby promotes cleanliness of the surfaces and wetting of the solder as a result of the enhancement in the metallurgic attraction of molten solder to the substrate. It should be noted that flux could also adhere to residual oxides during reflow as flux is often in direct contact with the surface(s) to be soldered. This could significantly increase the feasibility of having some anchored flux being entrapped in the molten solder which may result in voiding. As void formation is also driven by the rate of outgassing at a temperature above the melting point of a solder, a flux material with a low outgassing rate when the solder is in a molten state appears a preferable choice. The outgassing may not result in voiding if the flux can be separated from the interior of the solder joint.

Owing to the poor wetting ability of Pb-free solder alloys, the fluxing activity factor usually dominates the outgassing factor in Pb-free soldering [168].

### 3.3.4 Environment

In general, an inert atmosphere decreases the risk of void occurrence by facilitating wetting even though this effect may not be significant for fluxes or solder pastes with a high fluxing capacity and good oxidation resistance.

Humidity can also have an influence on voiding by interfering directly with the soldering or by promoting the outgassing of components. Flux outgassing may be increased if the humidity is high which can subsequently result in more voiding. Furthermore, the moisture within components or boards can also increase voiding.

## 3.4 Inspection criteria for process-induced voids

This section will be discussed in two sub-sections covering the IPC (Institute of Interconnecting and Packaging Electronic Circuits) criteria and military criteria.

### 3.4.1 IPC standard

IPC (Institute of Interconnecting and Packaging Electronic Circuits) published the standards for electronic manufacturing and for quality and reliability inspections. IPC provides the standards for acceptability of electronic assemblies [170] and design and assembly process implementation for BGAs [171], which defines the accept/reject criteria for BGA solder joints. Voids inspection criteria are based on the size of the void (which is calculated based on the percentage of the joint horizontal cross-sectional area covered by the voided area as depicted in Figure 3.4-1 and location of void inside the BGA solder ball. Based on IPC-A-610C, solder joints with more than 25% voiding are classified as defects while solder joints with 25% or less voiding percentage are acceptable. IPC-7095 further ranges voids from 9% to 36% depending on the vertical position of the voids (Table 3.4-1). These types of voids are further classified into three size groups as shown in Table 3.4-2. Class 3 voids are the most preferable because the area covered by the voids is less than 9%.

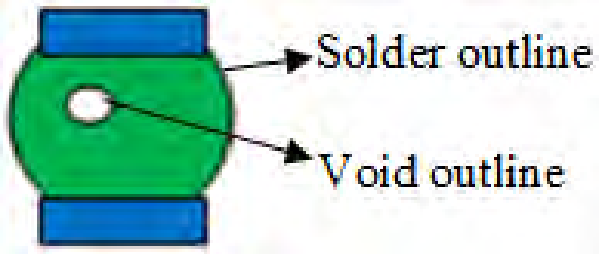



Figure 3.4-1: schematic of a solder ball and void (as inspected by X-ray, from top view)

Table 3.4-1: Void types

| **Inspection criteria** | **Void within the ball** | **Void at the package interface** | **Void at the substrate interface** |
|---|---|---|---|
| **Void in BGA ball prior to attachment to PCB** |  Type A |  Type B | - |
| **Void in BGA ball after attachment to PCB** |  Type C |  Type D |  Type E |

Table 3.4-2: Classification of voids

| **Void Type** | **Void Description** | **Class 1** | **Class 2** | **Class 3** |
|---|---|---|---|---|
| A | Inside ball at incoming | 60% diameter = 36% area | 45% diameter = 20% area | 30% diameter = 9% area |
| B | At package interface at incoming | 50% diameter = 25% area | 35% diameter = 12% area | 20% diameter = 4% area |
| C | Inside ball after PCB reflow | 60% diameter = 36% area | 45% diameter = 20% area | 30% diameter = 9% area |
| D | At package interface after PCB reflow | 50% diameter = 25% area | 35% diameter = 12% area | 20% diameter = 4% area |
| E | At the substrate interface after PCB reflow | 50% diameter = 25% area | 35% diameter = 12% area | 20% diameter = 4% area |

The aforementioned criteria may not be applicable to large area solder joints like the die-attach layer (solder thermal interface material layer). This is because a 0.1mm size void in a

BGA of 1mm ball size is different from a 0.1mm size void in a STIM layer which is rectangular in shape. The ratio of the void to ball in terms of area for BGA would be definitely much smaller compare to that of STIM layer.

### 3.4.2 Military standard

The military standard MIL-STD-883D, method 2030 [172] as presented in this section is related to rectangular solder joints. The MIL-STD-883D, method 2030 [172] (Table 3.4-3), for the ultrasonic inspection of die attach requires that the overall solder void should not exceed 50% of the total joint area, a corner void (Figure 3.4-2a) should not be bigger than 10% of the total void area and that a single void (Figure 3.4-2b) should be smaller than 10% of the total solder joint area.

Table 3.4-3: Solder joint ultrasonic inspection criteria outlined in MIL-STD-883D, method 2030 [198]

| Void pattern | Voiding percentage |
|---|---|
| Overall voiding | ≤ 50% |
| Single void | ≤ 10% |
| Corner void | ≤ 10% |

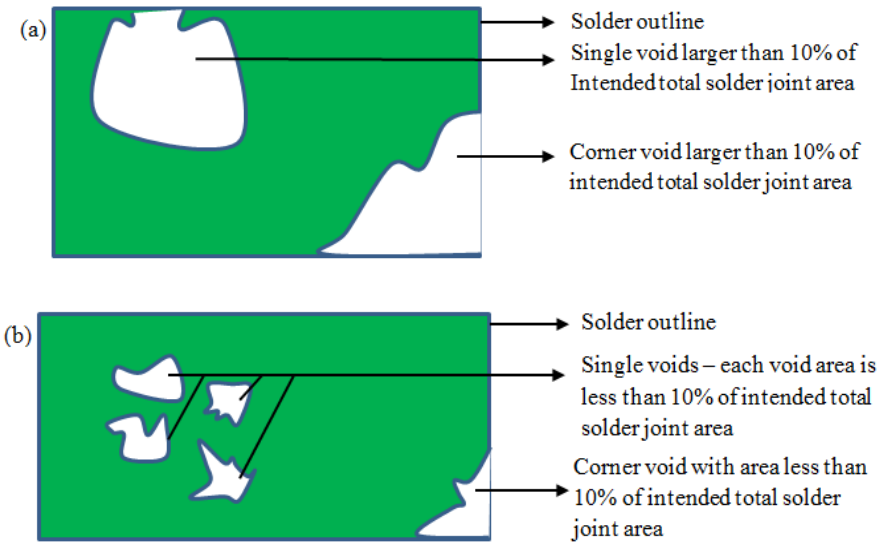



Figure 3.4-2: Schematics showing solder joint ultrasonic inspection criteria outlined in MIL-STD-883D(a) reject (b) accept

## 3.5 Effect of process-induced voids on the reliability of solder joints

Numerous studies have been carried out on the influence of voids on mechanical and thermal performance of solder joints and the overall electronic package. For instance, with regards to the effect of voids on mechanical durability of solder joints of different electronic packages;

Ladani and Dasgupta [173] used three dimensional (3D) finite element analysis(FEA) to study the effect of void size, location and spacing on the durability of Pb-free solders in BGA package. The results of the solder ball with different void sizes under temperature cycling showed that durability is a non-monotonic function of void size. Durability increases for void size larger than 15% of the area fraction of the ball and durability starts to reduce as the void gets larger. Their results also showed that voids located closer to the damage initiation site and propagation path decreased solder joint life. In a separate study, the same authors [174] examined damage initiation and propagation in BGA solder joints with voids, under thermo-mechanical loading. They concluded that generally, voids were not detrimental to thermal cycling durability of the BGA assembly, except when a large portion of the damage propagation path is covered with voids. They also reported that small voids can arrest damage propagation, but in general do not provide a great increase in the durability because the damage zone deflects around the void and also continue to propagate from other critical regions in the solder ball. Ladani and Razmi [175], investigated the interaction effect of void volume and standoff height on the thermo-mechanical durability of BGA solder joints using a 3-D visco-plastic (FEA). Their results showed a non-monotonic trend as the void size and standoff height increases. They found the critical size of void to be 35%.

Yunus et al. [176] determined the effect of voids on the mechanical deflection (torsion test) and thermal-mechanical reliability of BGA/CSP solder joints. The authors' results showed that voids reduce the life of the solder joints and that voids which are greater than 50% of the solder joint area reduce the mechanical integrity of the solder joints. It was also indicated in their results that though small voids have an effect on the reliability of the solder joint, the level of effect of such small voids depend on the frequency and location of the voids.

Dudek et al. [177] employed high resolution X-ray tomography to study solder voiding in Sn-3.9Ag-0.7Cu/Copper solder joint. They incorporated the 3D virtual micro-structural data into 3D finite element models in order to simulate deformation. It was shown that the presence of a large void at the solder/copper interface significantly increases the extent and severity of

strain localisation at the interface. Apparently, their results did not show a correlation between the size and shape of voids and the reflow process used to process the joints.

Yu et al. [178] examined the effect of process-induced voids on the thermal fatigue resistance of CSP solder joints. Their results suggested that though small void appear not to have effect on fatigue life, voids with diameter of at least 30% of the solder diameter did reduce the fatigue life when such voids were located along the crack propagation route. Also, their estimation of fatigue life employing FEA and Milner's law showed that voids not only have an effect on crack initiation but also on crack propagation.

Zhou and Qiu [179] studied the effect of voids on thermal fatigue reliability of BGA package using sub-modelling technique including the critical solder joint. They reported that the effect of voids on the reliability of solder joint was twofold; firstly, their result suggested that the creep shear strain and equivalent creep strain of solder joints with voids are not always higher than the solder joints with no void. Secondly, their results indicated that crack does not always initiate and propagate from the position of voids in solder joints. They therefore recommended that the position and size of voids should be taken into account when setting standards for solder voids inspection.

Terasaki et al. [180] analysed the effect of positions and sizes of voids on crack paths and the fatigue life of a BGA. Their results showed that crack paths and the fatigue life were both dependent on the positions and sizes of voids. Two-dimensional (2D) analytical results indicated that a circular void and a semi-circular void on the joint interface mainly reduce fatigue life. Their three-dimensional analytical results revealed that spherical and hemispherical voids have almost similar effects when the void area ratio is 11% or less. Nonetheless, when the void area ratio was higher than 15%, the hemispherical voids relatively had more detrimental effect on the fatigue life.

Chang et al. [75] employed Finite Element Modelling (FEM) for an investigation of the effects of void size (Figure 3.5-1) and location on the reliability of Sn-Ag-Cu as STIM. Their results showed that void size does not have a significant effect on the strain/stress distribution of the solder joint except when the void is located near the corner of the solder layer. In an experimental study to investigate the degradation of Sn-Ag-Cu as heat-sink attachment under thermal shock, Chang et al. [181] reported that the heat sink attachment with voiding areas of 33-48% experienced thermal shock above 3000 without failure, although there was degradation.

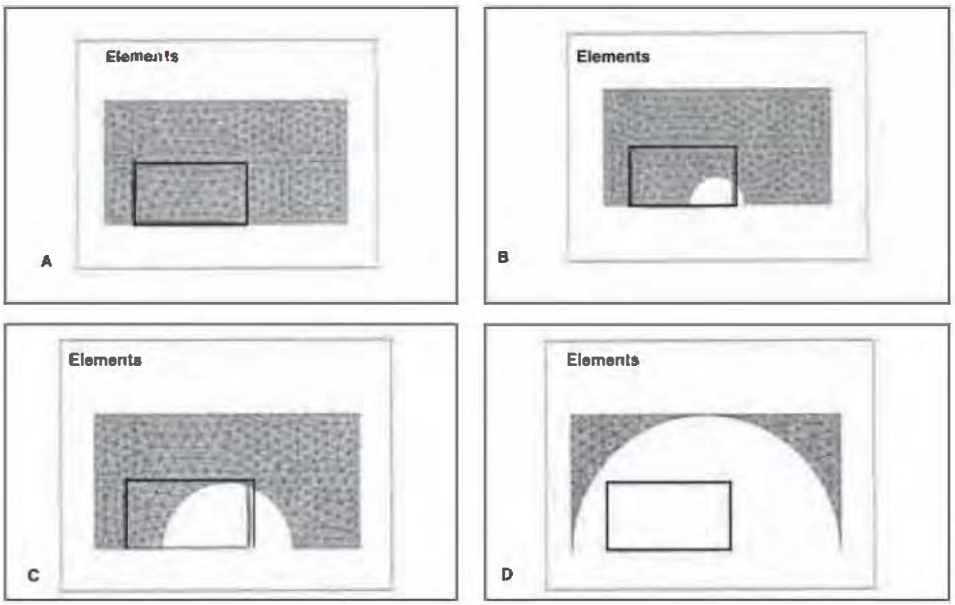



Figure 3.5-1: Heat-sink attachment model for different voiding percentages.(Black rectangle is the location of die.) A - 0%; B - 5%; C - 20%; and D - 79%.[75]

Gonzalez et al. [182] used two-dimensional FEM to study the fatigue shear strength of voided lead-free solder joints of a flip chip package. The authors' results showed that accumulated inelastic strain of a solder joint with a single void (Figure 3.5-2b) is not larger than that of void-free solder joint (Figure 3.5-2a) and that several voids in the same solder joint (Figure 3.5-2c) can reduce fatigue lifetime of the joint.

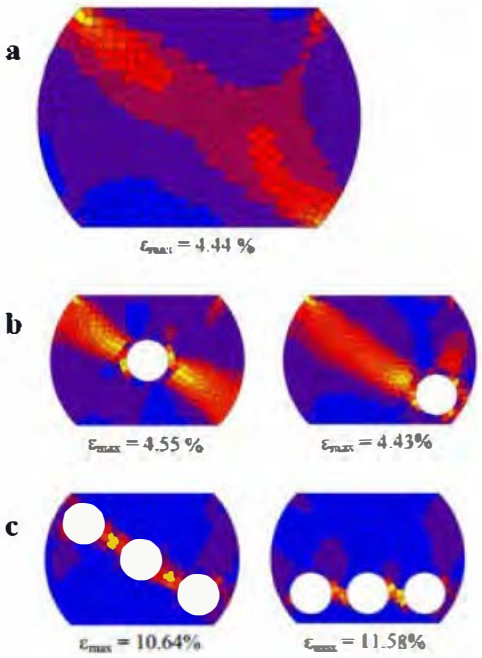



Figure 3.5-2: Equivalent creep strain in a solder joint (a) without any voids (b) with a void in different locations (c) with several voids [182]

Lau et al. [157] studied the effect of void size, location and fraction on the reliability of Sn-Pb solders for bump chip carriers (BCCs) under thermal cycling load employing two-dimensional FEM. Their result showed that in general, the larger the void percentage, the larger the creep strains. They reported that the void size and void location could play significant roles in the accumulated inelastic strain of the solder joints. Their results also suggested that joints with less than 20% void fraction did not affect the reliability and that crack propagation could be arrested by the presence of a void.

Zhu et al. [183] investigated the effect of voids (Figure 3.5-3) on the thermal fatigue reliability of BGA solder joints. They concluded that void reduce the fatigue life of the solder joints though they did not provide a quantitative value of the size of void.

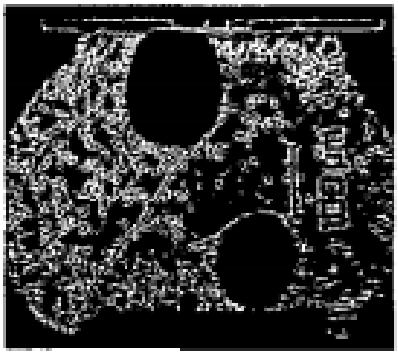


Figure 3.5-3: Voids found in failed solder ball[183]

In terms of the effect of solder void on thermal behaviour of an electronic package;

Chang et al. [75] investigated the effect of solder void size and location on thermal resistance of power devices using three dimensional (3D) finite element modelling. Their result suggested an increase in chip temperature and thermal resistance with increase in void percentages. Thermal resistance increased to 6.53% and 27.18% when the void percentages were 20% and 79%, respectively.

Fleischer et al. [62] used experimental and numerical methods to predict the relationship between void geometry in STIM and package thermal resistance. Package thermal resistance was observed to increase as void percentage rises. Thermal resistance increased to 30% with 73% voiding for random voids. This was in contrast with contiguous voids, with package thermal resistance increase of up to 200% for 73% voiding.

Biswal et al. [184] employed finite element analysis (FEA) to assess the impact of solder voids (voided STIMs) on the overall heat conduction of a high power module. It was found

that solder voids of relatively large radii impede heat conduction process to a great extent than small distributed voids.

Zhu [185] used FEA to study thermal impact of solder voids on a power device. Results showed that large, coalesced (Figure 3.5-4a) and/or edge voids have greater impact on the thermal resistance of the device than small, distributed voids (Figure 3.5-4b). It was also suggested that the temperature in the chip is much more sensitive to a void extending across the chip width than a void along the chip length.

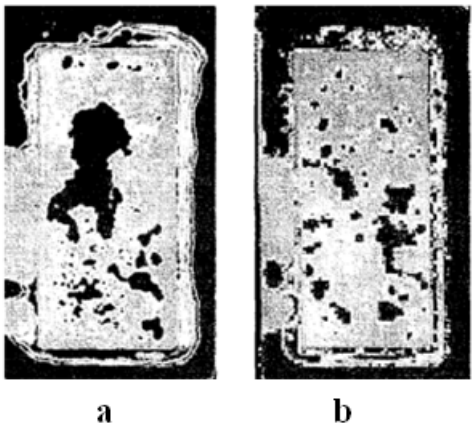



Figure 3.5-4: (a) Coalesced, large void (b) Distributed small voids [185]

### 3.5.1 Gaps in literature

Most of the previous studies suggest that the level of void effect would depend not only on void size but also on the configuration and location of the voids. Since the formation, size, location, frequency and volume fraction of voids are dependent on many factors that are extremely difficult to control practically during the manufacturing process, many researchers have employed FEM to study the precise effect of different void patterns on solder joints; In some of the finite element approaches such as the study by Chiriac and Yu [186], the material property used in modelling solder does not incorporate visco-plastic or creep deformation. Creep or visco-plasticity cannot be ignored in thermo-mechanical modelling of solder especially considering the high homologous temperature of solders. Many of the studies have investigated only the effect of voids on Pb-based solders and as such have only considered very limited range of void sizes and percentage [160, 187]. Voids occurrence is more and could even be more detrimental in Pb-free solder joints' especially considering the observation of voids in excess of 50% of some solder joint volume in some Pb-free solders [160]. Additionally, creep and plastic properties of Pb-free solders differ from Pb-based solder and damage accumulation may be influenced by solder properties.

Most of the experiments and modelling have been carried out on the effect of void on other applications of solder interconnects such as BGA, solder bumps and also under different loading rather than thermo-mechanical; none of the aforementioned studies has provided detailed information on the thermal and thermo-mechanical effects of void on the application of Pb-free solder as die-attach (TIM) for chip scale packaged device. While most of the previous studies on voided STIMs such as that by Fleischer et al. [62], Biswal et al. [184] and Zhu [185] have only concentrated on the thermal influence of certain features of voids on different electronic packages; Chang et al. [75], attempted to investigate the impact of different void percentages and locations on the thermo-mechanical reliability of Sn-Ag-Cu alloy as STIM. The study by Chang et al. [75] was without much details and analysis on the effect of different solder void features, this could be perhaps attributed to the shortcomings of the numerical models used in the study.

Furthermore, available results on the effect of voids on the thermo-mechanical behaviour of small area solder joints such as BGA or solder bumps are inconclusive or contradictory; for instance, some of the aforementioned studies indicated that voids do not always have an effect on solder joints reliability [179, 182] and that certain voids can even increase reliability [157] while other studies [175, 188] concluded that certain percentage of voids is detrimental to the solder joint thermo-mechanical performance. Generally, previous research suggest that the level of effect may depend on the solder properties, geometry of the joint, size, location and the pattern of void and the loading type.

Hence, more studies are needed for an in-depth understanding of the exact contribution of different features (size, fraction, spatial distribution, location) of voids to the mechanical and thermal behaviour of Pb-free STIMs. It is crucial to carry out such study for a range of void percentages and configurations associated with Pb-free STIMs and using representative constitutive material models. Data emanating from this study would provide the basis for representation of the effects of voids on thermal and mechanical performance of Pb-free STIMs.

### 3.6 Summary

Voiding remains a major reliability concern of STIMs coupled with the fact that solder joints are generally prone to thermo-mechanical fatigue failures. The occurrence of these voids in solder joints are unfortunately almost unavoidable during the manufacturing process as a result of the complexities and interactions associated with the many factors

(methods/machine, materials, human factors and environment) that affect voids formation. The impacts of these voids on the thermal and mechanical performance of solder joints are not well studied and scarcely available in literature especially with regards to STIMs (large area solder joints). Generally, available results from literature suggest that voids could have detrimental impact on the thermal and mechanical reliability of STIMs depending on the percentage, location, configuration and size of voids. Consequently, research questions were formulated to further investigate STIM and the influence of the different void features on the mechanical and thermal performance of STIM (solder die-attach) as will be reported in subsequent chapters.

Results emanating from such studies on mechanical and thermal effects of different void configurations on STIMs would certainly be very helpful to commercial industries especially when there is no generally accepted standard on distribution (vertical/spatial location) of die-attach voids for such industries, to the authors' knowledge. It is pertinent to note that the IPC standard for void inspection criteria reported in this chapter is meant for BGA and the failure criteria (MIL-STD-883D) for STIMs (also presented in this chapter) are high standards for military and aerospace applications.

# Chapter 4: Finite element modelling of voided solder die-attach

## 4.1 Introduction

An in-depth comprehension of the redistribution of temperature, strain and stress in the solder die-attach structure as a function of the voids size, voids distribution and voids location is required in order to achieve a better understanding of the complex structural and thermal behaviour of solder joint with voids. These void features are crucial in understanding the local and macroscopic temperature, stresses and strains in solder joint. As mentioned in Chapter 3, Section 3.5.1 (Gaps in literature), many researchers have employed FEM to study the precise effect of the different void patterns on solder joints. This is because the formation, size, location, frequency and volume fraction of voids are dependent on many factors that are extremely difficult to control practically during the manufacturing process.

FEM is widely accepted in analysing the mechanics and reliability of materials and structures like an electronic package. FE method gives valuable insights on evolution characteristics of internal states in the solder joint and low cycle fatigue deformation and failure prediction of the solder [189]. The post processing capabilities of FE offers user the opportunity to capture details with regards to the stresses and strains that are imposed in the system that is being tested. Among other commercial software tools that can be used for FEM, ANSYS Inc. FEM software is one of the most matured, widely distributed and popular commercial and academic package available. ANSYS has been previously employed for the successful analysis of various electronic assemblies from numerous industry sources and academic sources [190]. In many of these sources, empirical data that validates the accuracy of the FEM tool is presented within +/-2x, which is considered state of the art for such complex analysis. Nonetheless, it is crucial to understand the Physics behind the software. Correct prediction of the solder joint response is significantly dependent on details of geometric model including the accuracy of material data used in the modelling and suitability of constitutive materials model, adequacy of prescribed loading, boundary conditions and mesh density.

This chapter is divided into two main sections with sub-sections; the first section gives a detailed description of the geometric model generation algorithm for voided STIM. The second section discusses the modelling process adopted for the STIM including the theory of solder constitutive material model and a summary of the modelling assumptions. Finally, a summary of the chapter is given.

## 4.2 Numerical generation of solder voids

The first step in FEM is often to generate an appropriate model for finite element analysis (FEA). Hence, a representative volume element (RVE) of the test material (in this case, voided STIM layer) is often introduced [177, 191-192]. Among other factors, the void size and spatial configuration within the generated RVE is crucial in understanding the micro-structural influence on deformation of the test material [191]. Characterisation of void size and distribution/configuration has been conventionally carried out employing two-dimensional metallographic techniques. The problems with this approach are that it is destructive in that voids are damaged during the microscopy. Additionally, void morphologies are misrepresented in size and distribution. This is particularly true since published data showed that void size and distribution are inhomogeneous [177].

A technique referred to as X-ray tomography that can characterise an entire solder volume in a non-destructive manner is gaining popularity over the last few years. X-ray tomography (Figure 4.2-1) has recently been employed as a basis for obtaining micro-structurally realistic representative volume element (RVE) of voided solder joints. In fact, micro-tomography, in particular, has become popular among researchers [177, 191-192] as it makes possible the visualisation of samples with high resolution in 3D. Such 3D reconstruction of the exact microstructure can be easily incorporated into a finite element (FE) model to more accurately predict the performance of a material under load. In other words, X-ray tomography presents a micro-structurally realistic input to FEM. However, the aforementioned technique is relatively new and requires specific specialist software and resources that are very expensive.

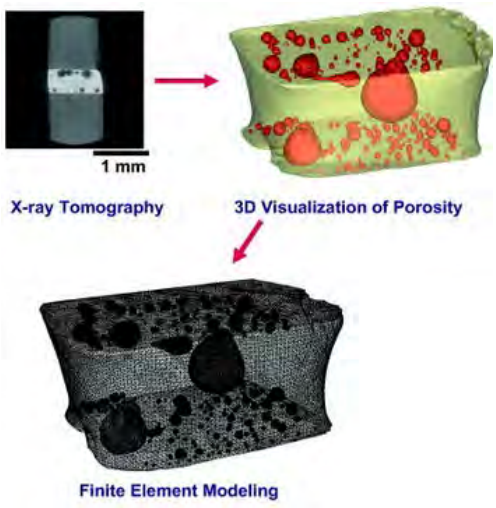



Figure 4.2-1: Schematic of x-ray tomography, 3D visualisation and simulation approach[191]

In order to overcome the complexities posed by X-ray tomography, a few researchers have proposed analytical methods to generate geometry that may be representative of voided solder joints. The progress in this coupled with the improvements in computational power have encouraged extensive modelling of complex physical processes and prediction of damage in solder joints. It is very crucial that the proposed analytical methods reflect the characteristics of real voided solder joints, i.e. heterogeneity and random spatial realisations of voids in a given solder joint. Unfortunately, the solder void patterns generated by current analytical method are often over-simplified by enforcing the void distribution to follow a regular pattern and thus far from reality. For instance, Fleischer et al. [62], in an effort to study the effect of different solder die-attach void distributions (small randomly distributed voids vs. large single void) on a chip-scale packaged power device, modelled solder die-attach voids as evenly spaced square patterns (Figure 4.2-2); Chiriac and Yu [186] in an attempt to study the impact of voids on thermal and mechanical performances of power quad flat no leads (PQFN) packages, modelled voids as orderly arranged circular patterns in the solder layer (Figure 4.2-3). The drawback of these models is that the shape and spatial morphology of voids are not representative of a true geometry of voided solder die-attach. The spatial distribution of the voids is not necessarily random as often observed in micrographs of real solder joint with voids. A practical example of real STIM layer with voids (from another piece of our experimental works) is shown in Figure 4.2-4; Void enclosures in the solder layer are visible as red spots. The void distribution in the micrograph of Figure 4.2-4 is random in location and shapes. A simplistic approach of assuming the voids as regular square patterns would clearly introduce errors to the analysis. For example, Kouznetsova et al. [193] studied the influence of spatial arrangement of voids within constitutive matrix models with non-linear loading histories including hyper-elastic, elasto-visco-plastic with softening and elasto-visco-plastic with hardening. Their results showed that while there is a small (but evident) effect in the elastic region, spatial distribution of voids has a significant influence in the results obtained for post-yield region.

Therefore a probable approach is to incorporate in a chosen 2D RVE (under certain assumptions) the spatial and geometric randomness of the voids. This work incorporates the spatial randomness, after the Monte Carlo implementation [194]. However, the geometric randomness in other words polydispersity of voids has not been incorporated. This challenge will serve as inspiration to future work.

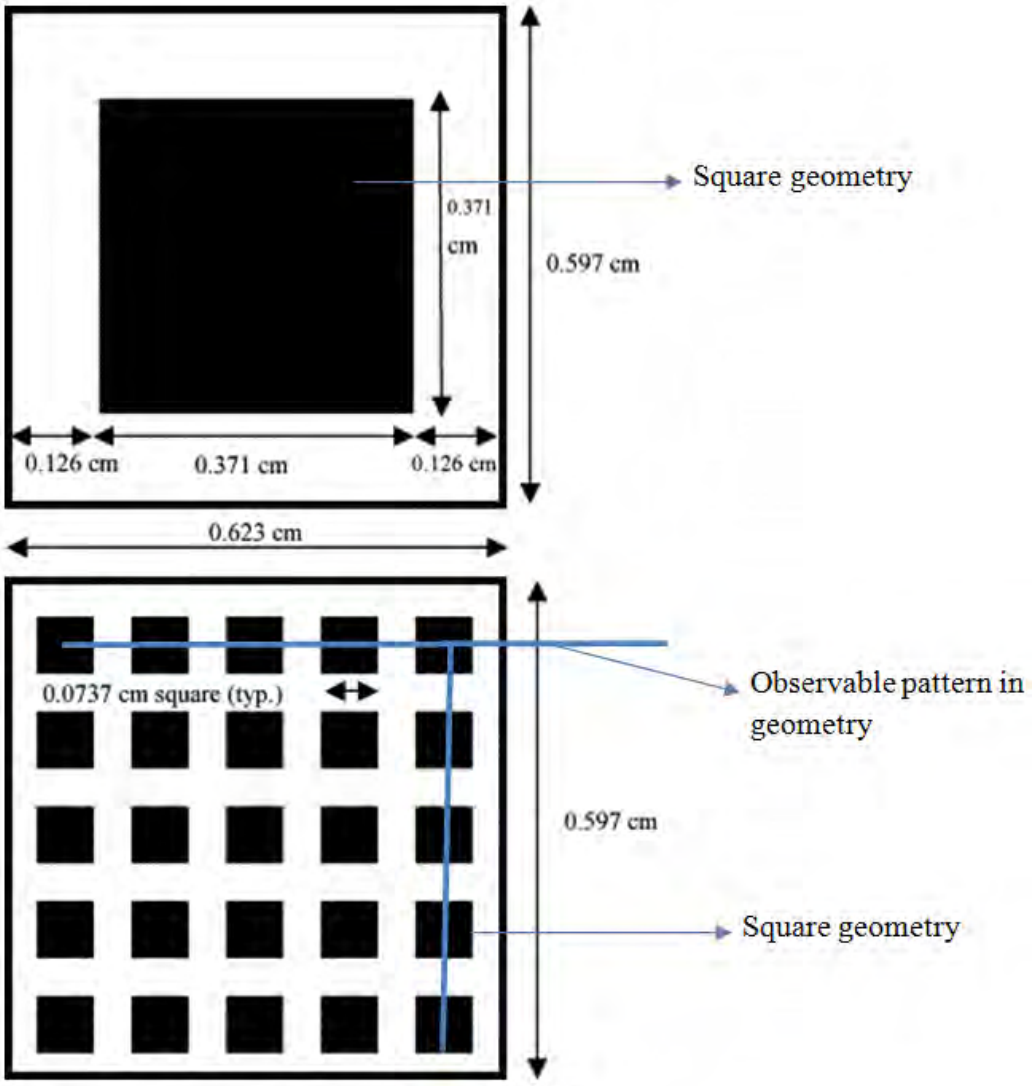



Figure 4.2-2: Shows the void model implemented by Fleischer et al.[62]

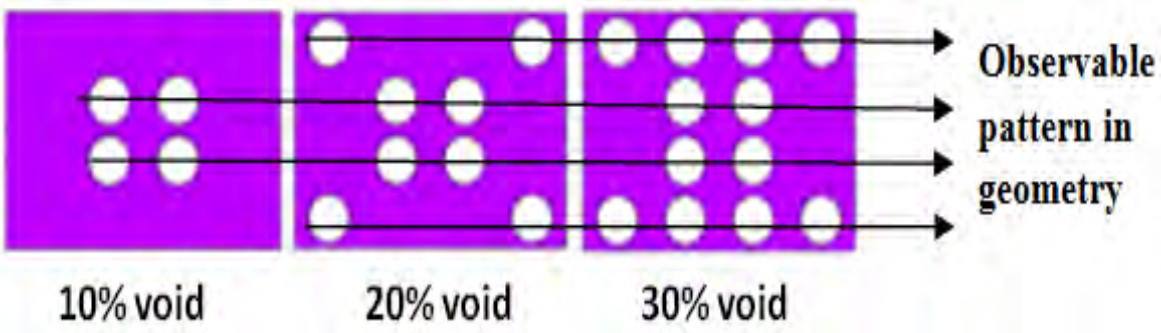



Figure 4.2-3: Shows the void model implemented by Chiriac and Yu [186]

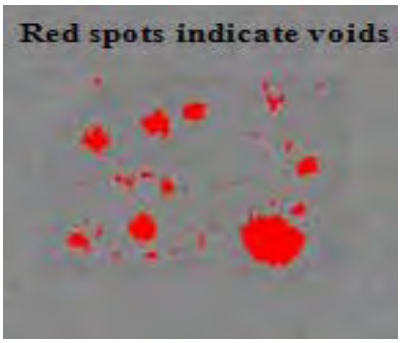



Figure 4.2-4: X-ray image showing voids in solder die-attach

In this work, a MATLAB algorithm called Monte Carlo Representative Volume Element Generator (*MCRVEGen)* was developed to generate the expected randomly positioned voids within a 2D RVE window. The inspiration for the algorithm was taken from existing algorithms that are attributed to Okereke et al. [194-195] and Melro [196]. This is the first time this approach has been used for solder voids modelling.

### 4.2.1 Monte Carlo generation of 2D RVEs

Monte Carlo methods are a class of computer algorithms that rely on repeated sampling method to compute their results [197-198]. The results are probability distribution of possible outcomes. Monte Carlo methods are often used in computer simulations of physical systems. They can be used to model phenomena (such as random occurrence of voids in solder joint) with substantial uncertainty in inputs.

With regards to this work, the Monte Carlo approach of solder geometric model generation adopts a random placement of any inclusions (in this case, circular voids) within a defined RVE size. This strategy is common in the composite modelling community where the inclusions are typically circular shaped fibres within a rectangular shaped matrix. The principle applies likewise in this work except that the inclusions are voids. The approach described here was made popular by Okereke and Akpoyomare [194] who applied this approach for analysis of mechanics of unidirectional (UD) composites. The Monte Carlo imposed randomness, as applied in this work is more suitably referred to as pseudo-random since it is computer-generated randomness. Once a 2D RVE window is defined, the *MCRVEGen* algorithm continues to populate a defined RVE window (often square) with non-overlapping circular voids until a defined volume fraction is reached. A flow chart of the algorithm for Monte Carlo 2D RVE Generator is shown in Figure 4.2-5.

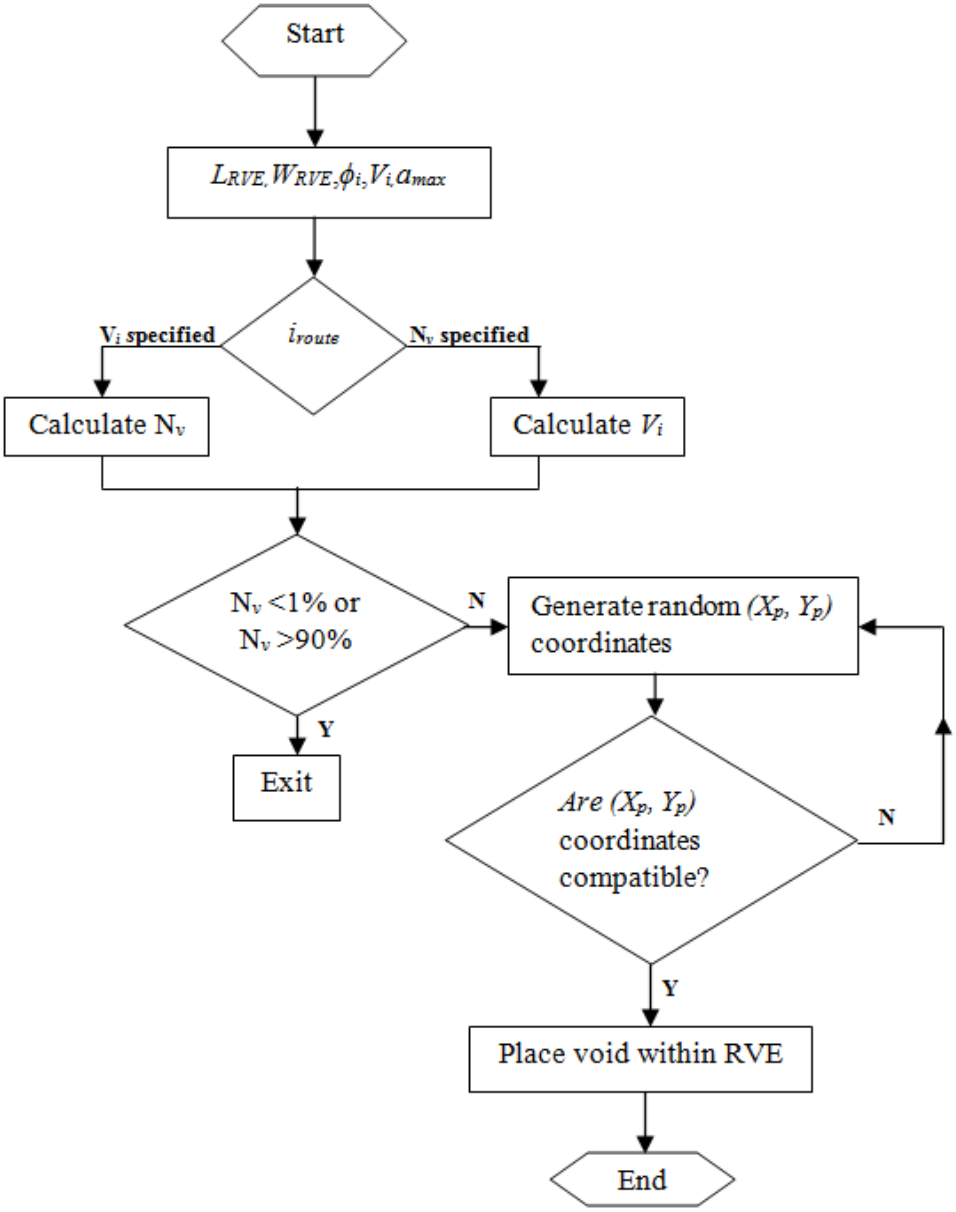



Figure 4.2-5: Flowchart of the algorithm for the Monte Carlo 2D RVE Generator

At the start of the algorithm, a few key parameters are declared as inputs, namely; (a) the dimensions of the RVE window (in this case, the square dimension of the solder die-attach (TIM) layer), $L_{RVE}$ and $W_{RVE}$, (b) the diameter of the circular voids, $\phi_i$, and (c) the required volume fraction of the voids, $V_i$. Two iteration routes, $i_{route}$, exist within the algorithm; the first route would continue the population of the defined RVE window based on the volume fraction of voids that was declared. Alternatively, the second route calculates the number of voids, $N_v$, that would result in the required volume fraction, $V_i$ , which is defined as:

$$V_i = \frac{N_v \times A_i}{L_{RVE} \times W_{RVE}} \qquad (4.2\text{-}1)$$

Where, $N_v$ is number of voids, $L_{RVE}$, $W_{RVE}$, is the length and width of the RVE window, respectively. $A_v$ is cross-sectional area of void which is described as:

$$A_v = \frac{\pi \emptyset_i^2}{4} \qquad (4.2\text{-}2)$$

It is important that the total number of voids $N_v$ is an integer. Where this is not the case following calculations, then an iterative procedure has to be taken by perturbing the RVE window size until the approximate integer value for $N_v$ is obtained.

During the population of the defined 2D RVE window with circular shaped inclusions, the *MCRVEGen* generates the coordinate positions of the circular voids randomly resulting ultimately in an RVE with spatially random spatial distribution of voids. In principle, after the first void is successfully placed, the coordinates of subsequent voids are randomly generated and tested to verify that:

- The coordinate positions are greater than a defined distance, $d_{ove}$, from the previous void.
- Newly generated voids must not overlap with already existing void(s).

Due to the seeming randomness of generating voids within a defined RVE window, the voids can potentially intersect one another. Hence, a methodology was developed to address this; Figure 4.2-6, shows a typical RVE window with origin located at $\{X_{ORVE}, Y_{ORVE}\}$. Assuming that there is, a *qth* void with coordinate $\{X_q, Y_q\}$ and diameter, $\phi_q$, in this window. The distance between the centre of this *qth* void and any other void, *p*, in the defined RVE window can be regarded as $d(p,q)$, where $p = 1,2,3,\ldots q\text{-}1$. A void may be considered to be overlapping if the expression $|d(p,q) < \phi_q|$ is true. $d(p,q)$ (distance between two voids) can be calculated using the Euclidean metric:

$$d(p,q) = \sqrt{(X_p - X_q)^2 + (Y_p - Y_q)^2} \qquad (4.2\text{-}3)$$

The *MCRVEGen* algorithm is set up in such a manner that the expression $|d(p,q) \geq d_{ove}|$ is true, before any void is accepted to be placed within the RVE window. Where;

$$d_{ove} = \psi \phi_q \qquad (4.2\text{-}4)$$

$\psi$ is a dimensionless multiplicative constant and $\psi \geq 1$. It should be noted that any two closest voids will be touching one another if $\psi = 1$. Thus, in order to avoid the voids touching, the numerical method should implement that $\psi > 1$. It is also worth noting that the placement of

voids within the RVE was enforced to only be inside the RVE window such that the problem of boundary or surface voids was prevented. This was done to make for easy implementation of boundary conditions on edges rather than a combination of edges and void curvatures.

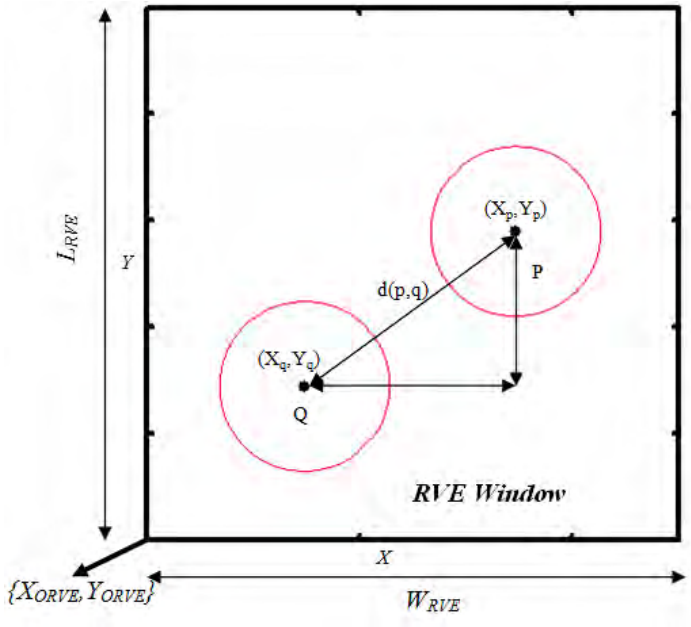



Figure 4.2-6: Illustration showing formulation for calculating distance between/spatial descriptors for two voids

- The inclusion does not result in exceeding the required volume fraction of the defined RVE window and
- The coordinates are within the defined RVE window

If the aforementioned criteria are satisfied for the new position, it is then accepted. Otherwise, the algorithm will attempt to place another randomly generated void position which is again verified until the compatibility criteria are fulfilled. The maximum number of attempts, $a_{max}$, is limited to 100,000. This is because experience has shown that allowing for more attempts may not lead to a successful random void placement.

#### *4.2.1.1 Implementation of MCRVEGen Algorithm*

The *MCRVEGen* algorithm was implemented as a MATLAB script. While keeping the RVE window constant, the algorithm was used to create RVEs with different volume fractions of randomly generated voids. An example of the different void configurations generated in MATLAB using the *MCRVEGen* algorithm is shown in Figure 4.2-7 for 5% void volume fraction.

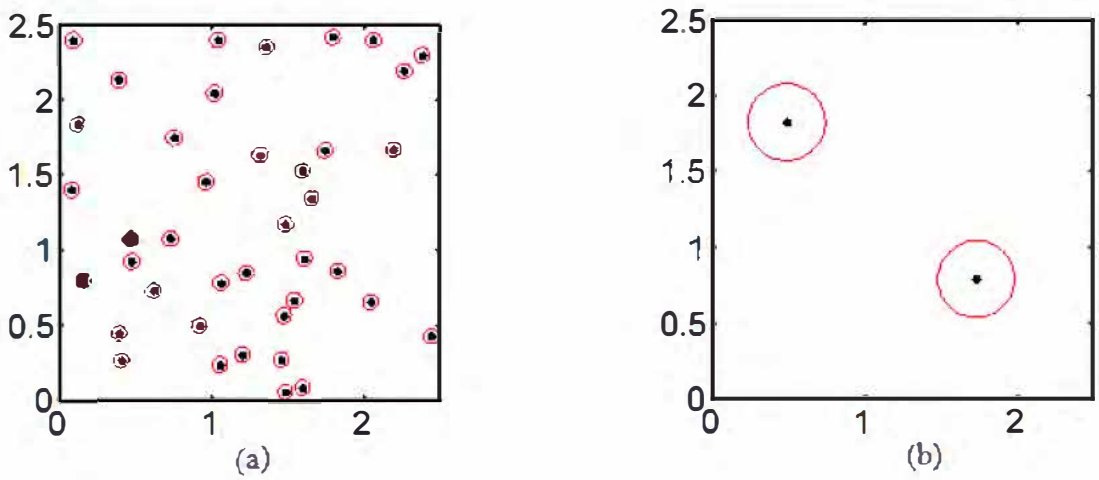



Figure 4.2-7: Typical 2D square RVE for different configuration of 5% void volume fraction (a) small random voids, void diameter = 0.1mm (b) large random void configuration, void diameter = 0.5mm. For axes: I unit = 1mm.

The voids were generated only up to 30% volume fraction due to the limitation of the Monte Carlo approach which is known to have a jamming limit less than 50% [199]. As the density of voids within an RVE window increases, the speed of placing the void reduces as the algorithm searches through increasing numbers of neighbouring voids. A typical performance plot for *MCRVEGen* algorithm for simulating different RVEs of randomly distributed voids is shown in Figure 4.2-8. This plot is based on simulations within a Windows 7 operating system with 2.68 GHz Intel(R) i7 processor.

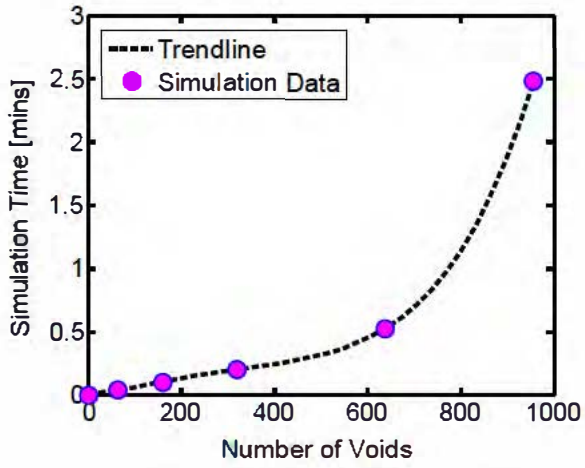
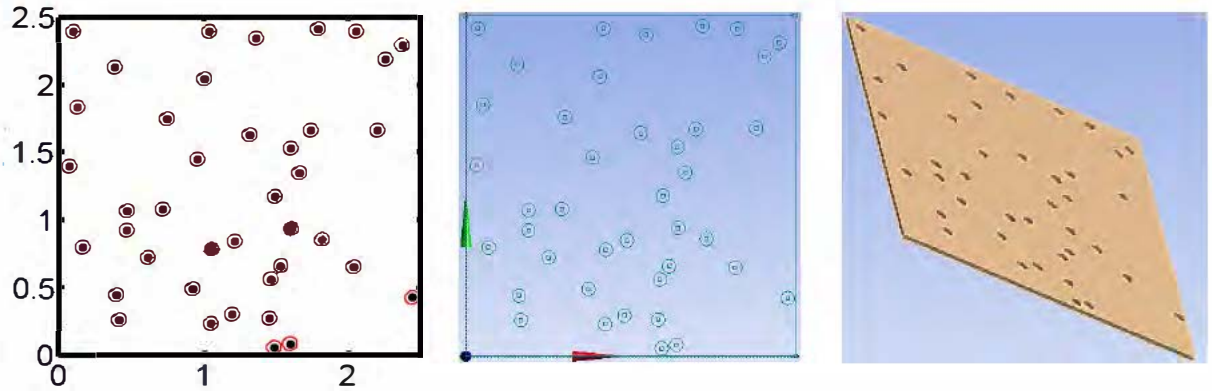



Figure 4.2-8: Performance plot for Monte Carlo 2D RVE Generator

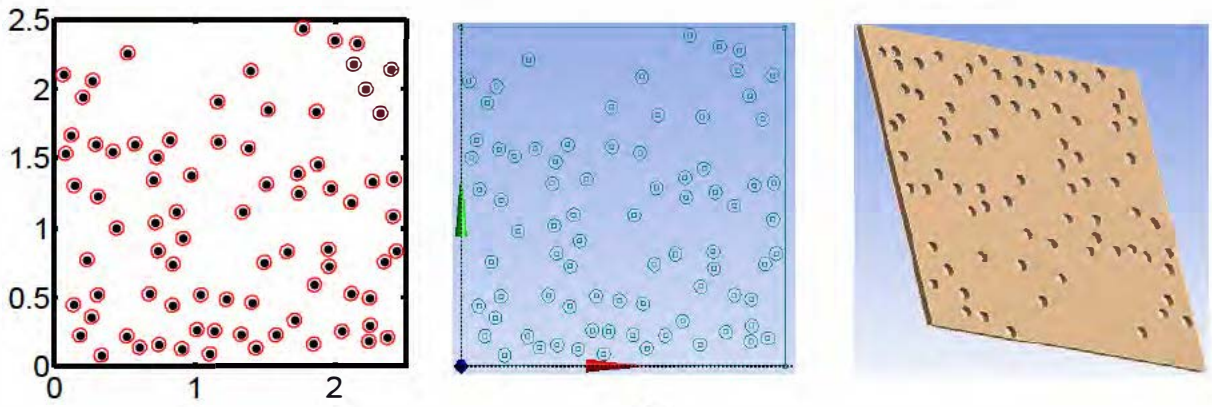
### 4.2.2 Creation of 3D RVEs in ANSYS

After the generation of the 2D RVEs using the *MCRVEGen* as described in the previous sections, the next challenge was the creation of the model within a FEM scheme. In this case,

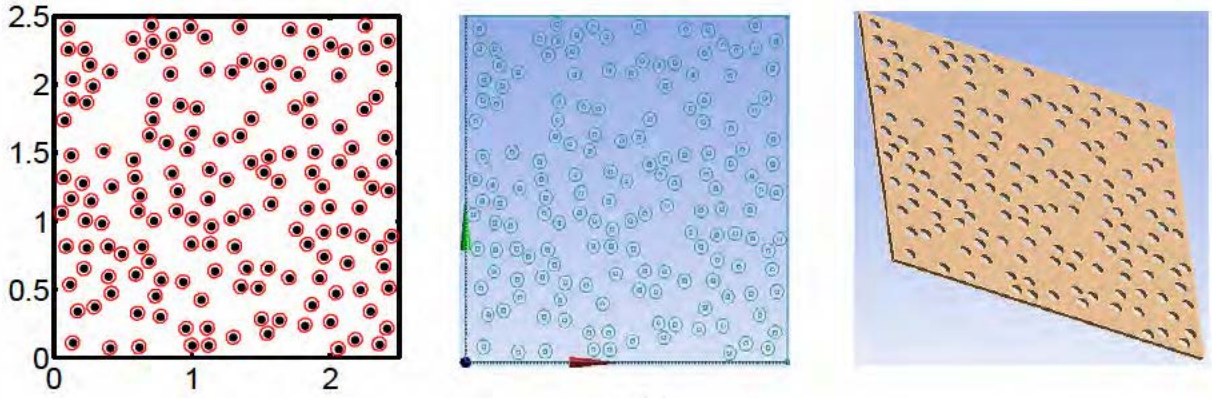
the finite element program employed is ANSYS. This study developed a *java* script which used the input from results of *MCRVEGen* simulation to automatically create the exact 2D RVE with voids (represented as circles). Using ANSYS extrusion tool, the generated 2D RVE was then extruded in out-of-plane direction to form 3D RVE. Typical thickness of the STIM layer is about 0.04mm. The three-step implementation is shown for varying void volume fraction in Figure 4.2-9 for small voids and Figure 4.2-10 for large voids configurations.



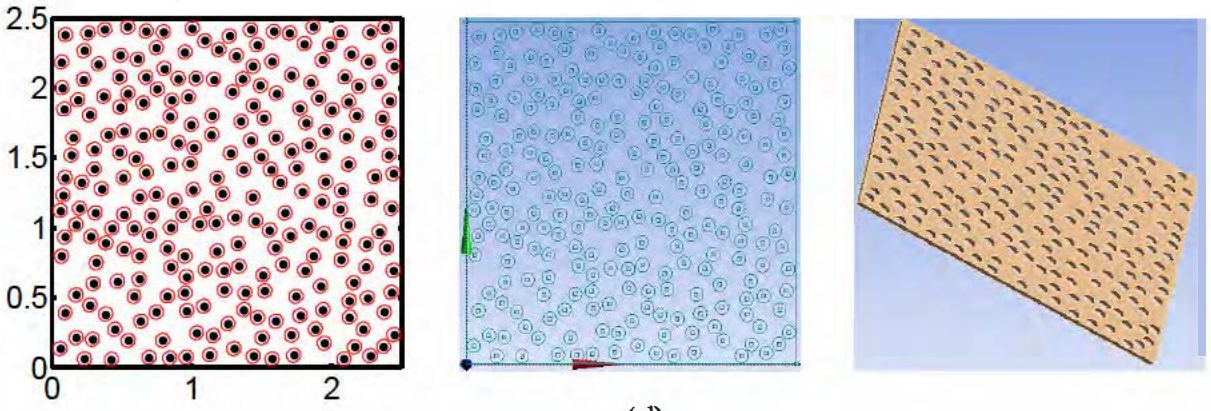

(a)




(b)

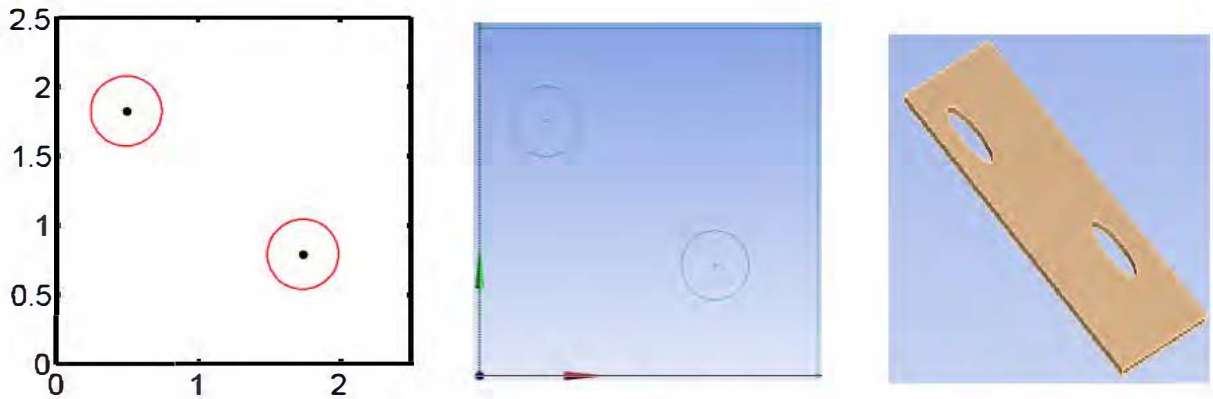



(c)

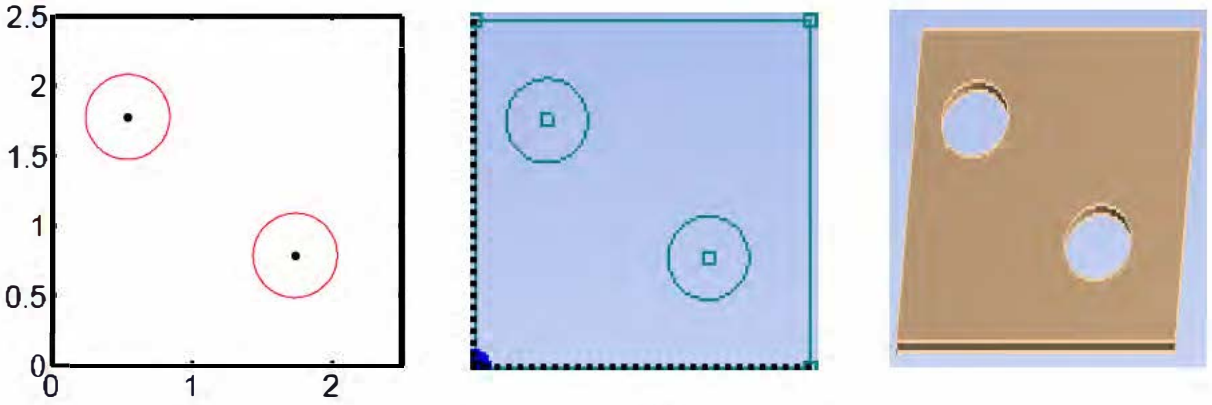



(d)

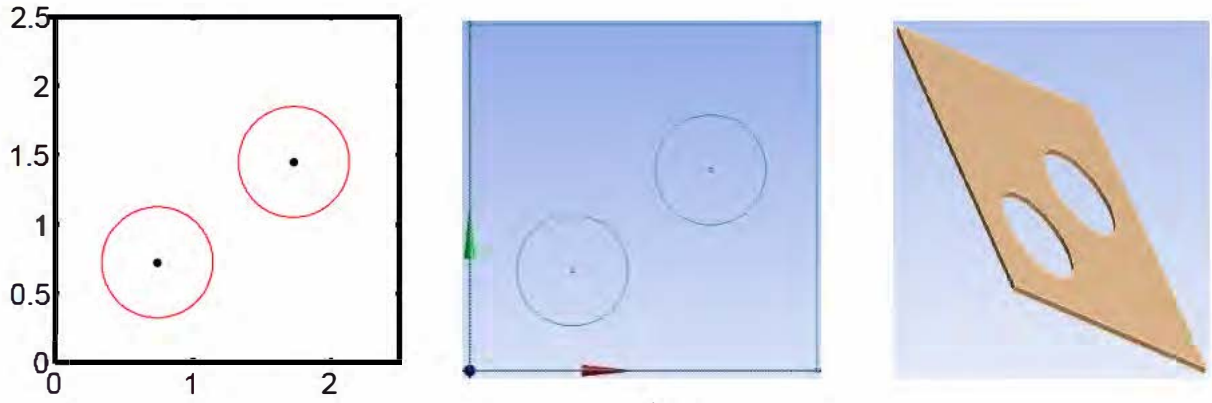
Figure 4.2-9: Illustration of a three-step implementation for creating 3D RVEs with spatially random distribution of voids for *small* voidswhere (left) *MCRVEGen*-generated output, (middle) ANSYS javascript-created 2D RVE and (right) ANSYS created 3D RVE. The figures are for varying volume fraction: (a) $V_i = 5\%$ (b) $V_i = 10\%$ (c) $V_i = 20\%$ (d) $V_i = 30\%$.



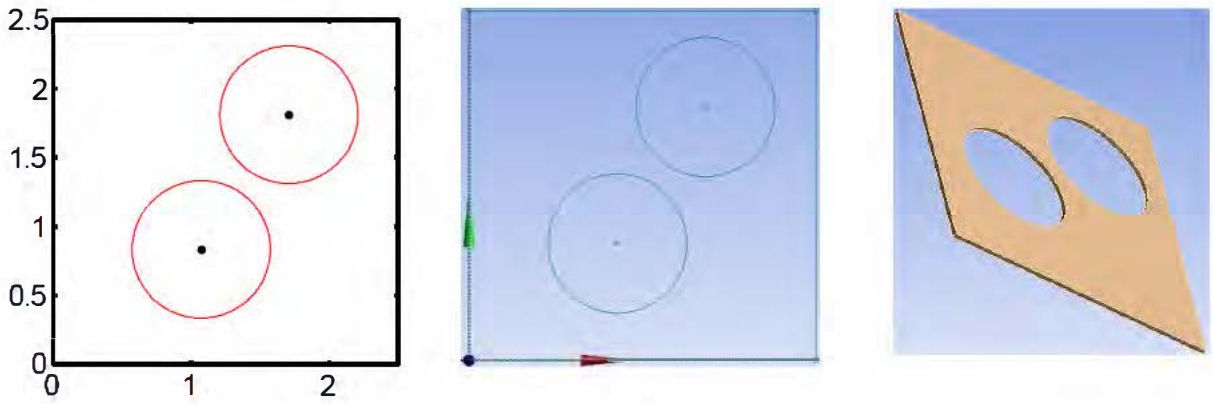

(a)




(b)




(c)




(d)

Figure 4.2-10: Illustration of a three-step implementation for creating 3D RVEs with spatially random distribution of voids for *large* voidswhere (left) *MCRVEGen*-generated output, (middle) ANSYS javascript-created 2D RVE and (right) ANSYS created 3D RVE. The figures are for varying volume fraction: (a) $V_i = 5\%$ (b) $V_i = 10\%$ (c) $V_i = 20\%$ (d) $V_i = 30\%$.

It can be seen from Figure 4.2-9 and Figure 4.2-10 that the distribution of voids is significantly random both for the small and large voids. For the small random voids, the diameters of the voids were kept the same (0.1mm) while the void volume fraction increased from 5% to 30%. For the large voids, the diameters of the voids were allowed to increase (from 0.5mm - 1.0mm) with increasing void volume fraction. Although this current implementation of *MCRVEGen* has achieved the expected spatial randomness of *circular* voids within a defined RVE window, there remains the challenge of incorporating random void shapes – as the latter is a feature of real voids. This work has to be assessed bearing this limitation in mind.

Random distribution of voids through the volume/thickness of a STIM layer is also a feature of real voided solder materials. An ideal model setup will involve 3D RVEs with randomly distributed voids through the thickness of the STIM layer. Such volumetric void-generation feature could be achieved by generating multi-layers of randomly voided STIM and then bonding the different layers together to form a model of STIM layer with through-thickness random void arrangements. This is further demonstrated in Figure 4.2-11.

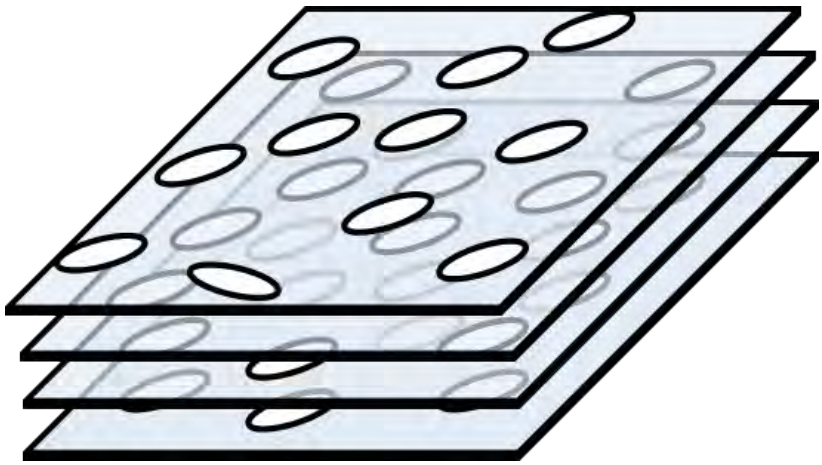


Figure 4.2-11: 3D RVEs with randomly distributed voids through the thickness of the STIM layer

### 4.3 Constitutive model for solder material

Mechanical constitutive material defines the deformation of a material under a load. Hence, constitutive relations that predict strain as a function of stress, time and temperature are influential in the results of Finite Element Modelling (FEM) of materials in an electronic package. The total strain in solder can be separated into elastic and inelastic components as in equation 4.2-1:

$$\varepsilon_T = \varepsilon_e + \varepsilon_{in} \quad (4.3\text{-}1)$$

where,$\varepsilon_T$ = Total strain, $\varepsilon_e$ = elastic strain, $\varepsilon_{in}$ = inelastic strain

The elastic strain component is described by Hooke's law wherein the induced stress in a solder joint is a function of the applied stress and Young's modulus. This is described in equation 4.3-2:

$$\boldsymbol{\varepsilon_T} = \frac{\boldsymbol{\sigma}}{\boldsymbol{E}} \quad (4.3\text{-}2)$$

Where,$\varepsilon_T$= Total strain, σ = Stress in MPa, E = Young's modulus in MPa.

It should be noted that the Young's modulus of solder is often dependent on temperature and usually represented at various temperatures by:

$$E(T) = E_0 - E_T(T) \quad (4.3\text{-}3)$$

Where T is the temperature, $E_0$ is the Young's modulus at $0^oC$ and $E_T$ is the temperature dependent value of Young's modulus.

As shown in equation 4.3-4, the inelastic strain component is estimated as the linear sum of time independent plastic strain, $\varepsilon_{pl}$, time independent creep strain, $\varepsilon_{cr}$ and time dependent visco-plastic strain $\varepsilon_{vp}$.

$$\varepsilon_{in} = \varepsilon_{pl}+\varepsilon_{cr}+\varepsilon_{vp} \quad (4.3\text{-}4)$$

### 4.3.1 Time independent plastic strain

Time independent plastic strain is a non-recoverable plastic deformation that occurs typically due to dislocation pileups from lattice defects. Plastic deformation happens when the stress in a loaded material under a particular strain level reaches a certain yield stress level. Time independent plastic strain is often modelled using a power law in which stress is an exponential function of strain. This is commonly known as exponential hardening model, expressed as –

$$\sigma = K(\varepsilon_{pl})^n \quad (4.3\text{-}5)$$

σ is equivalent stress, K is a pre-exponential factor, n is plastic strain hardening component. K and n are temperature dependent constants. It should be noted that the plastic behaviour of solder, particularly the yield stress is temperature dependent.

### 4.3.2 Time dependent plasticity

Time independent plasticity, otherwise known as creep strain, is a rate dependent plastic strain deformation at constant uniaxial stress [200]. As illustrated in Figure 4.3-1, creep often happen in a material when the homologous temperature is greater than $0.5T_m$ (one half of its absolute melting temperature). Homologous temperature expresses the temperature of a material as a fraction of its melting point temperature using the Kelvin scale as defined in equation 4.3-6 [201].

$$T_h = \frac{T}{T_m} \qquad (4.3\text{-}6)$$

Where $T_h$ is homologous temperature, T is the material's temperature and $T_m$ is the material's melting point temperature.

Solders can creep even at room temperature because of their often high homologous temperature. For example, SAC305 has a homologous temperature of 0.61 $T_m$ at room temperature ($T_m$ = 217°C) while that of 63Sn-37Pb is 0.65 $T_m$ at room temperature ($T_m$ = 183°C). It is obvious that both homologous temperatures are higher than 0.5Tm and thus solders can experience creep even at room temperature. In service conditions, where the operating temperature is usually between -40 to 125°C, the homologous temperature of eutectic Sn-Pb solder is at 0.51 – 0.87$T_m$, while that of SAC305 solder is at 0.48-0.81$T_m$. As can be seen in Figure 4.3-1, all of these ranges are within creep range when devices are under load.

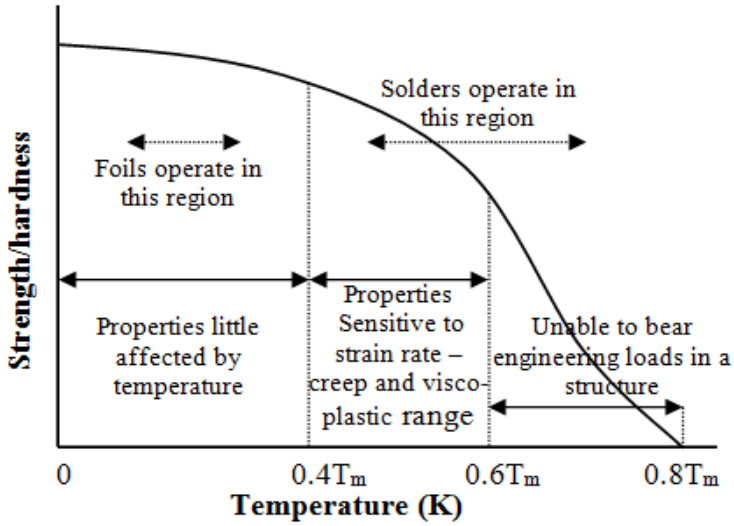



Figure 4.3-1: Strength of a metal as a function of its melting temperature

Creep curve is typically broken into three parts – primary, secondary and tertiary (Figure 4.3-2) after the initial instantaneous strain when a constant load is applied [200]. The initial strain may consist of elastic or time independent plastic deformation as soon as stress is applied. The first stage which is the primary region is characterised by transient creep with rapidly decreasing strain rate due to work hardening which restricts creep occurrence. A long duration of nearly constant slope is often observed in the secondary stage or steady state creep region. This slope is known as the "steady state" secondary creep rate or creep compliance and it is often employed by engineers as one of the crucial parameters used in FEM to predict solder joint reliability. In this stage, strain rate is impeded by strain hardening, and this deters the occurrence of creep, while the associated recovery and re-crystallisation (softening) appear to enhance the creep rate [202]. In the third region, known as the tertiary stage, where nucleation and growth of cavities have been induced [200]. The creep strain rate begins to increase and necking occurs under constant load.

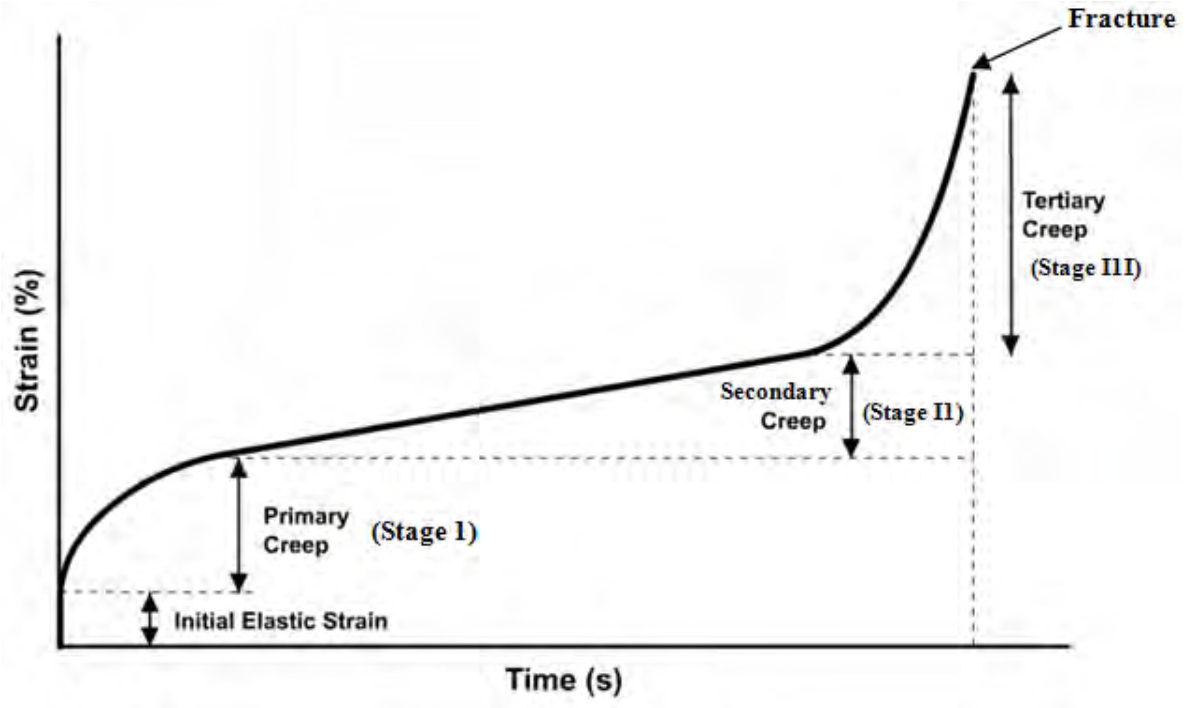



Figure 4.3-2: Schematic showing creep curve. Strain vs. Timeunder constant stress (load) and temperature

Considering that creep is thermally activated, it is unsurprising that the steady state creep strain rate for eutectic and near eutectic solder alloys can be characterised by Arrhenious-type rate model (also known as Norton creep law) type equation. This can be expressed as a power law function:

$$\dot{\varepsilon}_s = A\sigma^n e^{-(\frac{Q}{RT})} \qquad (4.3\text{-}7)$$

Where $\dot{\varepsilon}_s$ is the steady state shear strain rate, $\sigma$ is the current stress, A and n are experimentally determined material constants, Q is the activation energy for creep, R is the universal gas constant and T is the temperature of the solder in Kelvin.

The power law stress dependence breaks down at high stresses. Hence, the strain rate is no longer dependent on the stress to the power, n. The power law breakdown region can be subsequently expressed by the Garafalo model [203]:

$$\dot{\gamma}_s = \mathrm{C}_1 \frac{G}{T}\left[sinh\left(\alpha\frac{\tau}{G}\right)\right]^n . exp\left(\frac{-Q}{kT}\right) \qquad (4.3\text{-}8)$$

Where $\dot{\gamma}_s$ is the steady state shear strain rate, $C_1$ is experimentally determined material constant, G is the temperature dependent shear modulus, T is the absolute temperature, α defines the stress level at which the power law stress dependence breaks down, τ is the shear stress, n is the shear component, Q is the activation energy for a specific diffusion mechanism.

### 4.3.3 Unified viscoplasicity model/Anand constitutive model

Since the time-independent plasticity and time-dependent plasticity (creep) emanates from the same fundamental mechanisms such as dislocation motion, diffusion and climb, it is desirable to have a unified plasticity model that captures both of these mechanisms. Viscoplasticity is defined as unifying plasticity and creep through a set of evolutionary equations where a constraint equation is used to reserve volume in the plastic region [204]. A commonly used unified plasticity model which can be easily incorporated into commercially available FEM software packages is proposed by Anand.

Anand developed a constitutive model for hot working of metals by unifying plasticity and creep through a set of flow and evolutionary equations. There are two main features in the Anand's model. Firstly, there is no explicit yield surface and no loading/unloading criterion is used. Material's instantaneous response is dependent on its current state and plastic strain is assumed to occur at all non-zero stress values, although the plastic flow may be negligible at low stresses. Secondly, a single internal scalar variable called the "deformation resistance" denoted by "s" is used to represent the averaged isotropic resistance to inelastic flow of the material. Anand's model is fully explained in References [205-206]. The model is summarised by equations (4.3-9) – (4.3-11).

The flow equation 4.3-9 represents the specifics of the Anand's constitutive model.

$$\dot{\varepsilon}_{in} = Aexp^{\left(-\frac{Q}{RT}\right)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \qquad (4.3\text{-}9)$$

Table 4.3-1 shows the definition of parameters and other constants associated with the model. In equation 4.3-9, $\dot{\varepsilon}_{in}$, $T$ and σ are inelastic strain rate, temperature in absolute scale and equivalent stress, respectively. The "s", a single scalar internal variable, is the deformation resistance, whose evolution is described by:

$$\dot{s} = \left\{sign\left(1-\frac{s}{s^*}\right)h_0\left|1-\frac{s}{s^*}\right|^a\right\}\dot{\varepsilon}_{in} \qquad (4.3\text{-}10)$$

Where s*, described in equation 4.3-11 is the saturation value of "s" associated with a given temperature and strain rate pair:

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_{in}}{A}e^{Q/RT}\right]^n \qquad (4.3\text{-}11)$$

The Anand constitutive equations presented here accounts for the physical phenomenon of strain-rate and temperature sensitivity, strain hardening or softening characteristics, strain rate and temperature history effects, internal damage and its evolution, crystalline texture and its evolution [207]. In comparison to other plasticity and creep models, Anand's model has been shown to provide reasonable results [23].

Table 4.3-1: Anand parameters definition

| **Parameter** | **Description** |
|---|---|
| $s_o$ (MPa) | Initial value of deformation resistance |
| *Q/R* (1/Kelvin) | Activation energy/Boltzmann's constant |
| *A*(1/s) | Pre-exponential factor |
| ξ (dimensionless) | Stress multiplier |
| *m*(dimensionless) | Strain rate sensitivity of stress |
| $h_o$ (MPa) | Hardening/softening constant |
| ŝ (MPa) | Coefficient for saturation value of deformation resistance |
| *n*(dimensionless) | Strain rate sensitivity of the saturation value |
| *a*(dimensionless) | Strain rate sensitivity of the hardening/softening |

## 4.4 Summary

This chapter covers the methodology adopted in developing the numerical models that were analysed in this work. An algorithm (*MCRVEGen*) was developed for the generation of 3D representative volume element (RVE) of random distribution of voids in a given solder joint. The algorithm is based on a well reported model, where the void placement and subsequent populating of a defined RVE window with voids are done according to Monte Carlo algorithm. This is the first time this approach has been used for solder voids modelling. The generated RVEs were firstly obtained as 2D RVEs using the Monte Carlo approach and the voids within the solder layer are subsequently extruded to form required 3D RVE. While the former was implemented in MATLAB coding environment, the latter was carried out using a Java Script run within ANSYS Design Modeler Scripting User Interface. It is pertinent to note that although the algorithm (*MCRVEGen*) used for the numerical models generation was able to implement random spatial distribution of circular voids adopting a Monte Carlo approach, it is expected that the algorithm can be further improved to incorporate variation of void sizes and shapes within a given representative volume element (RVE) as in existing micrographs of voided TIMs. This would represent an even more realistic voided STIM layer. This chapter also presented the theory and implementation of finite element modelling. It was shown that visco-plastic model can be used to effectively capture the plastic deformation of solder under temperature excursions.

# Chapter 5: Characterizations of Lead – free solders as TIMs under thermal cycling: Numerical modeling – Part I

## 5.1 Introduction

STIM provides both mechanical and thermal connection between the chip and heat spreader. Mismatches in the coefficients of thermal expansion (CTE) of the silicon die and heat spreader induces cyclic mechanical stresses and strains (Figure 5.1-1) in the die-attach (STIM) when the package is exposed to temperature cycling. Two common thermal cycling examples are the heating and cooling that takes place during a typical day in the afternoon and early morning hours, and the heating and cooling within the automotive engine compartment when the automotive is used to travel from one location to the other. As the strength of solder is low compared to other materials that constitute the electronic assembly, cyclic stresses and strains could result in thermo-mechanical fatigue deformation in the part of the solder.

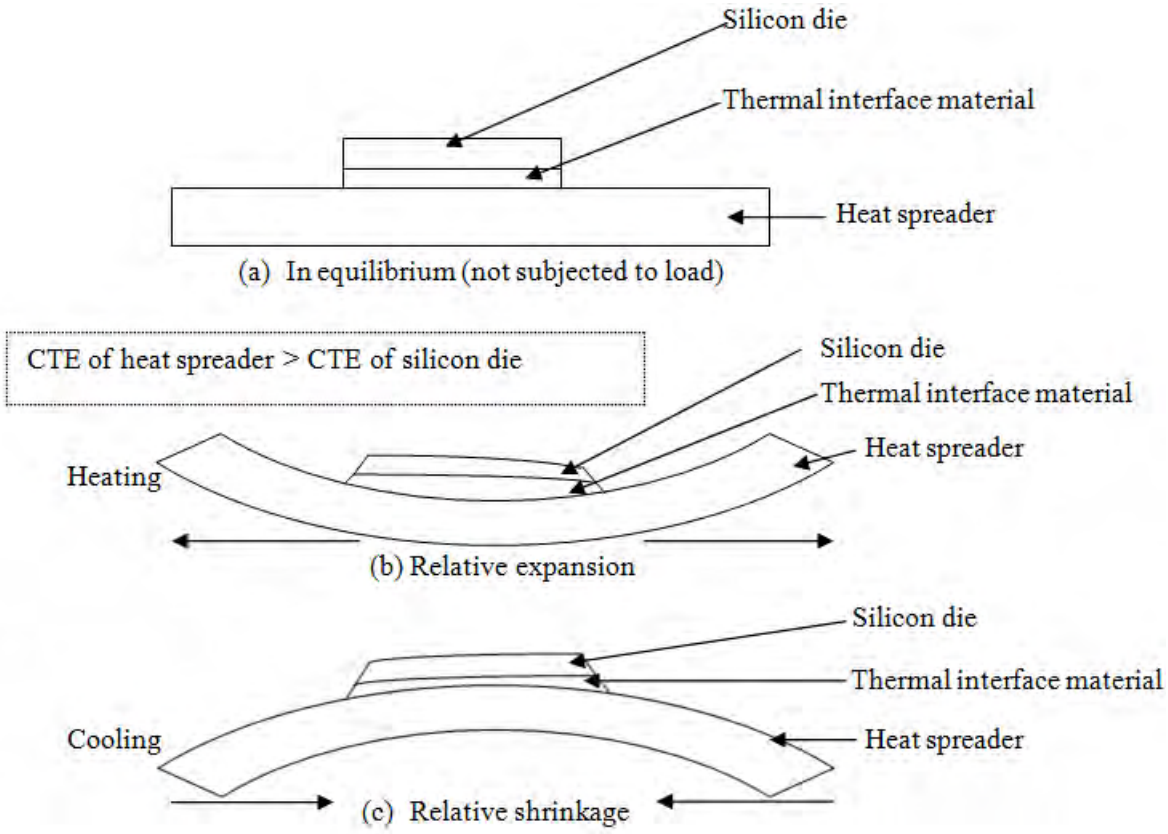



Figure 5.1-1: Schematics (not drawn to scale) showing (a) Assembly in equilibrium (no load) (b) CTE mismatch producing cycling stress due to relative expansion of the assembly during heating (c) CTE mismatch producing cycling stress due to relative shrinkage of the assembly during cooling

Apart from voiding as discussed in the previous chapter, solder joints are generally prone to fatigue deformation. In fact, solder fatigue is a driving failure mode in electronics [208].

Fatigue is a means by which a material is weakened by cyclic loading [209]. The resulting stress often lead to catastrophic failure even though the stress may be below the ultimate tensile stress or even the yield stress. Fatigue behaviour of materials is often characterised into two categories, low cycle fatigue and high cycle fatigue. High cycle fatigue consists of cyclic deformations that are in the elastic regime and have not exceeded the yield point. An example of high cycle fatigue is failure in solder joint due to vibration at moderately low pressure. Low cycle fatigue happens when the cyclic deformations are too large and plastic deformation dominates. Thermal cycling of solder can result in low cycle fatigue with the inelastic strains consisting of both time dependent (creep) and time independent (plastic) deformations. In electronic applications, solder joint fatigue deformation is primarily caused by the stresses due to temperature swings and the mismatches between the CTE of different bonded materials that constitute the electronic package.

Fatigue deformation induced by temperature cyclic loading and CTE mismatches can potentially change the constitutive properties of the solder material which may eventually lead to thermo-mechanical fatigue failure of the joint. Therefore, these changes have to be considered in the selection of Pb-free solder for TIM application and subsequent parametric study of the effect of voids on the selected Pb-free solder material in the next chapters.

### 5.1.1 Effect of silver content in the fatigue performance of SAC Pb-free solder alloys

The optimal silver (Ag) content in the Sn-Ag-Cu (SAC) alloys is crucial in fabricating a STIM that relatively has an improved thermal fatigue performance [210]. While the focus as regards implementing SAC solders as die-attach has been on decreasing thermal resistance path [211] as demonstrated in Section 5.2, it is also highly essential to evaluate and understand the thermo-mechanical reliability of these solders when employed as TIMs under thermal excursions akin to service conditions.

Numerous reports on the effect of Ag content on thermo-mechanical performance of SAC solders in different applications are available in the literature. For instance, Terashima et al.[210] studied the effect of Ag content on the thermal fatigue endurance of Sn-xAg-0.5Cu (x=1,2,3 and 4 in mass%) flip-chip solder bumps. They reported a greater failure rate for solder joints with lower Ag content (x = 1 and 2) in comparison to joints with higher Ag content (x = 3 and 4) when subjected to thermal cycling. Kariya et al. [212] carried out a mechanical shear fatigue test to study the effect of Ag content on the fatigue properties of

Sn-xAg-0.5Cu (x = 1,2,3 and 4) of flip-chip solder bumps. Their results showed that the strength of the solder bumps rises with increasing Ag content. Mustafa et al. [213] examined the effect of solder composition by testing four SAC alloys (Sn-1Ag-0.5Cu (SAC105), Sn-2Ag-0.5Cu (SAC205), Sn-3Ag-0.5Cu (SAC305), Sn-4Ag-0.5Cu (SAC405)) with different silver content (1-4%) under strain controlled cycling. Their results suggested more degradation for solder alloys with lower silver content. Collins et al. [214] investigated the thermal fatigue performances of ceramic chip resistors soldered to printed wiring boards using solder alloys with different silver contents (SAC105, SAC205, SAC305, SAC405). They reported longer fatigue lifetime for SAC405 and SAC305. Yan and Li [215] studied the effects of different Ag contents on the fatigue lifetimes of Pb-free solder joints used for board level assembly of Fan-in Package on Package (FiPoP). They reported the longest lifetime and shortest lifetime for SAC405 (highest Ag content) and SAC105 (lowest Ag content), respectively.

Although the aforementioned studies suggest that mechanical strength and thermal fatigue resistance of SAC solder joints increase with higher Ag content, SAC305 in comparison to SAC405 has gained more popularity in North America, Europe and Asia [216-217]. The favourable preference for SAC305 compared to SAC405 could be because; some studies [212, 218-221] have reported reduced elastic modulus which helps to cushion stress transferred to vulnerable joint regions of SAC alloys with lower Ag content under drop/impact test. No wonder Kariya et al. [212] recommended SAC305 for the solder bump of a flip chip because they surmised the strength and fatigue ductility of SAC305 are better balanced relative to SAC405. Additionally, SAC305 is less expensive due to its lower Ag content in comparison to SAC405. Moreover, Japan electronic industry development association (JEIDA) and National electronics manufacturing initiative (NEMI) have recommended SAC305 [222] and SAC405 [223], respectively. Thus, debate continues over whether the thermo-fatigue performance of SAC305 is comparable to that of SAC405. This subject has been well investigated for small area solder joints (flip-chip solder bump and BGA) but some potential applications have not been studied to compare the thermal fatigue performance of different SAC alloy compositions due to varied Ag content. This study aims to fill this gap by evaluating the effect of different Ag content on the thermal fatigue behaviour of SAC305 and SAC405 solder alloys when used as thermal interface material (large area solder joint) for a chip-scale packaged power device. Solder joint shape/geometry is reportedly one of the main factors that can affect solder joint fatigue performance [224].

Research on thermal fatigue performance of large area solder joints has not had much attention compared to small area solder joints.

In this chapter, finite element analysis (FEA) is employed, firstly, to demonstrate the thermal performances of chip-scale packaged power device without heat spreader and with heat spreader coupled to the backside of the chip using SAC STIM. Based on the simulation results of the global thermal models, a simplified local model was generated. This generated local model is then used for a comparative (non-linear finite element method) study of the mechanics and thermo-mechanical reliability of SAC305 and SAC405 solder alloy compositions as STIMs under different thermal cyclic loading conditions. Three thermal cycle profiles [225] representative of the test methods used by the automotive industry to characterise interconnect reliability of CSP assemblies are used for the performance evaluation. The results are discussed in terms of the von-Mises stress, strain energy and plastic work in the STIM layers. Before the summary of the entire chapter, concerns regarding the application of conventional fatigue lifetime prediction model to STIMs (large area solder joints) were discussed.

## 5.2 Finite element model: Thermal effect of a heat spreader and STIM on thermal resistance

The thermal models (shown in Figure 5.2-1(a) and (b) for packages with and without heat spreader respectively) were created in ANSYS 13.0. Table 5.2-1 specifies the properties and dimensions of the different components of the models. The heat (1W) generating area (active area) is applied as a heat flux on the top surface of the silicon chip. The mesh consists of 1287365 nodes and 438,204 elements. Temperature distributions around the package with and without heat spreader in natural convection (stagnant air) are shown in Figure 5.2-2(a) and (b), respectively. The maximum temperature was attained at the centre of the chip where the heat source is located. The thermal resistance and chip junction temperature were found to be about 3 times higher in the package without a heat spreader compared to the package with heat spreader. It is apparent that improved thermal performance could be achieved through coupling a heat spreader to the backside of the die using a STIM [28]. This is because of the relatively lower thermal conductivity through the front-side intermediate layers of the package particularly the organic substrate and also limited number of solder bumps that make only a small fraction of contact area. A more detailed work on the contribution of the solder balls under the chip (chip front-side) to heat dissipation has been reported in Reference [3]. Hence, subsequent models will consider only the backside of the

package with heat spreader (shown in Figure 5.2-3b) as the representative improved heat removal path under investigation. The focus is on the performance of solder die-attach as will be covered in subsequent sections and chapters of this thesis.

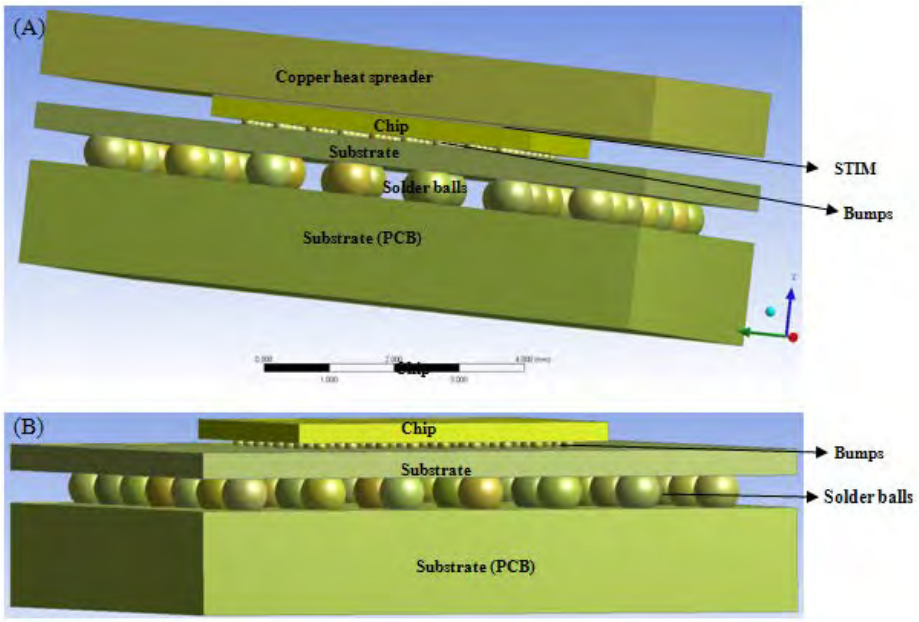



Figure 5.2-1: Model structure for package (A) with heat spreader (B) without heat spreader

Table 5.2-1: Dimensions and properties of models in Figure 5.2-1.

| **Parameter** | **Chip** | **Solder (Sn3.0Ag0.5Cu)** | **Copper heat spreader** | **Bumps** | **Substrate** | **Solder balls** | **PCB** |
|---|---|---|---|---|---|---|---|
| Length (mm) | 5 | 5 | 9.59 | - | 9.59 | - | 9.59 |
| Width (mm) | 5 | 5 | 9.59 | - | 9.59 | - | 9.59 |
| Thickness (mm) | 0.3 | 0.04 | 1 | - | 0.4 | - | 1.6 |
| Radius (mm) | - | - | - | 0.05 | - | 0.33 | - |
| Pitch (mm) | - | - | - | 0.5 | - | 1.27 | - |
| Standoff (mm) | - | - | - | 0.1 | - | | - |
| Conductivity (W/mK) | 120 | *50 | 386 | *50 | 0.3 | *50 | 0.3 |

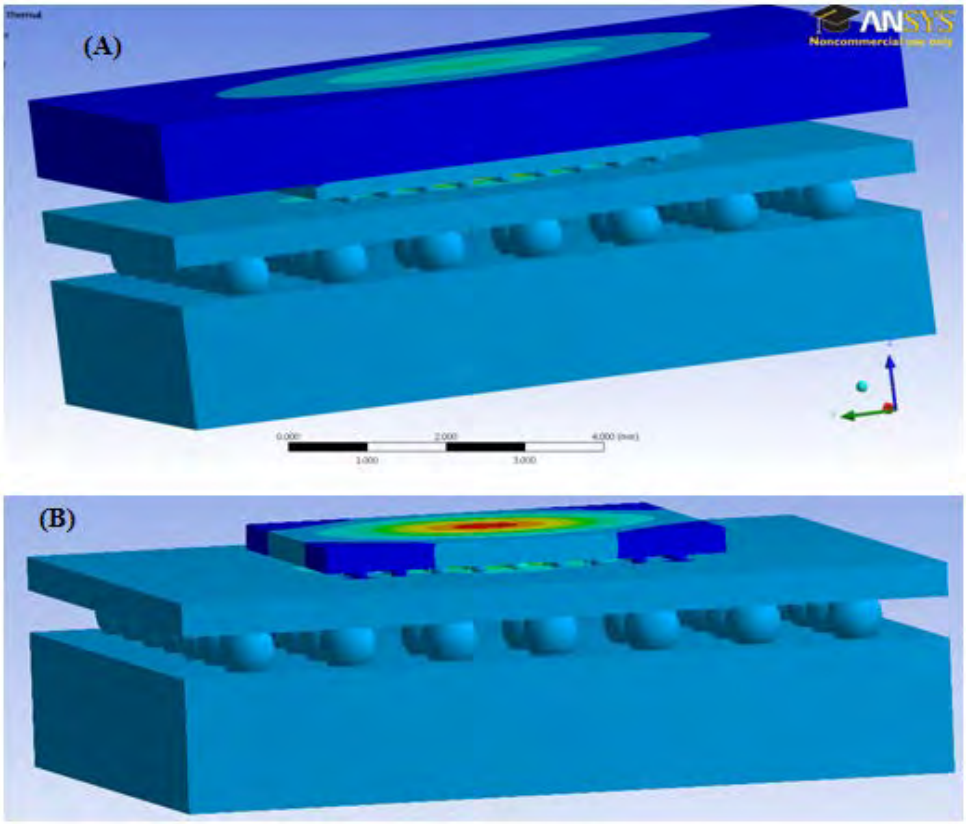



Figure 5.2-2: Temperature distribution for package (A) with heat spreader (B) without heat spreader.

### 5.2.1 Simplified local model for thermo-mechanical reliability modelling: Effect of Ag content on SAC304 and SAC405

As discussed in Section 5.2, thermal analysis of the model indicates that the solder die-attach plays a crucial role in the overall thermal performance of a chip-scale packaged power device. As a result, the local model considers only the backside solder die-attach of the electronic package (shown in Figure 5.2-3b) as a level of interest. It should also be noted that the thermo-mechanical reliability of front side solder bumps (small area solder joint) in flip-chip CSP (Figure 5.2-3a) has been extensively studied by means of finite element simulations. The local (simplified) model consists of a silicon die of the packaged semiconductor power device mounted upon a stack of supporting layers of SAC alloy STIM and copper heat spreader as depicted in Figure 5.2-4. The geometric dimensions of the components of the model assembly are listed in Table 5.2-2.

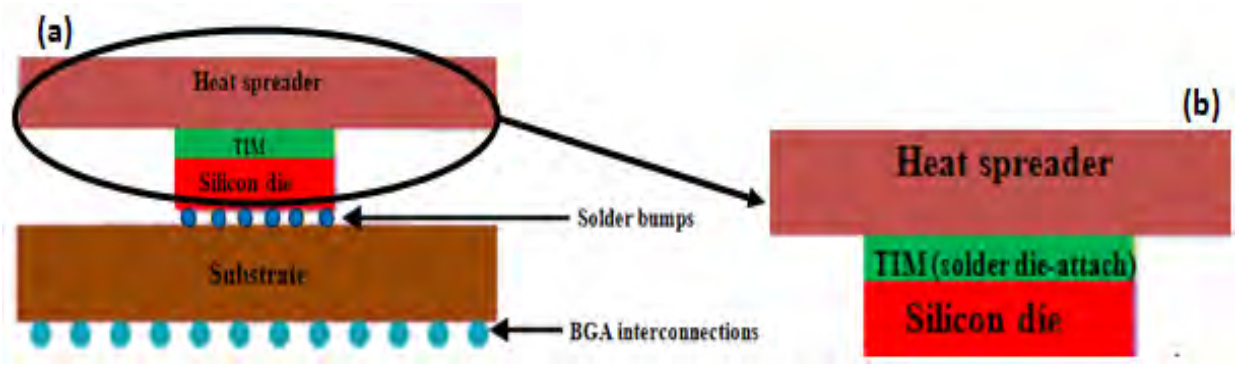



Figure 5.2-3: Schematic of (a) full flip-chip CSP configuration (b) backside of the package considered in the simulation

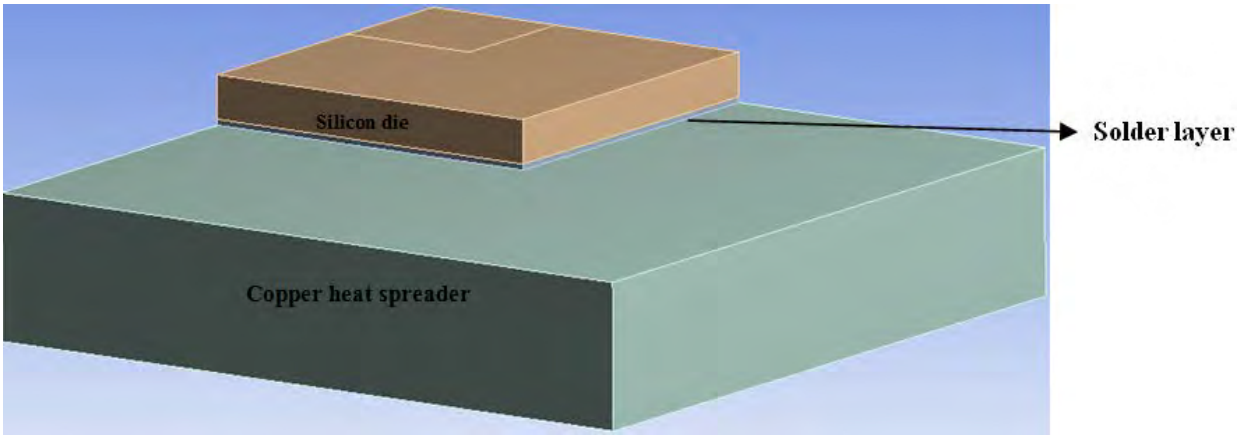



Figure 5.2-4: Simplified model structure

Table 5.2-2: Dimensions of package assembly constituents

| Parameter | Silicon die | Solder | Copper heat spreader |
|---|---|---|---|
| Length (mm) | 5 | 5 | 10 |
| Width (mm) | 5 | 5 | 10 |
| Thickness (mm) | 0.3 | 0.04 | 1 |

The commercial finite element analysis (FEA) software ANSYS V.13 was used for both the finite element modelling and analysis. The FEA program subdivides the assembly into finite elements (mesh) as shown in Figure 5.2-5(a) and a fine mesh pattern (Figure 5.2-5b) is maintained in the solder layer as a crucial area in the analysis. The same mesh distribution/concentration is used across all the cases investigated in a particular study to

ensure correct comparison of the results. The mesh for the assembly consists of 437924 nodes and 86698 elements. Only ¼ geometric symmetry of the 3-dimensional (3D) FE model is used in the analysis so as to reduce computational time and storage space.

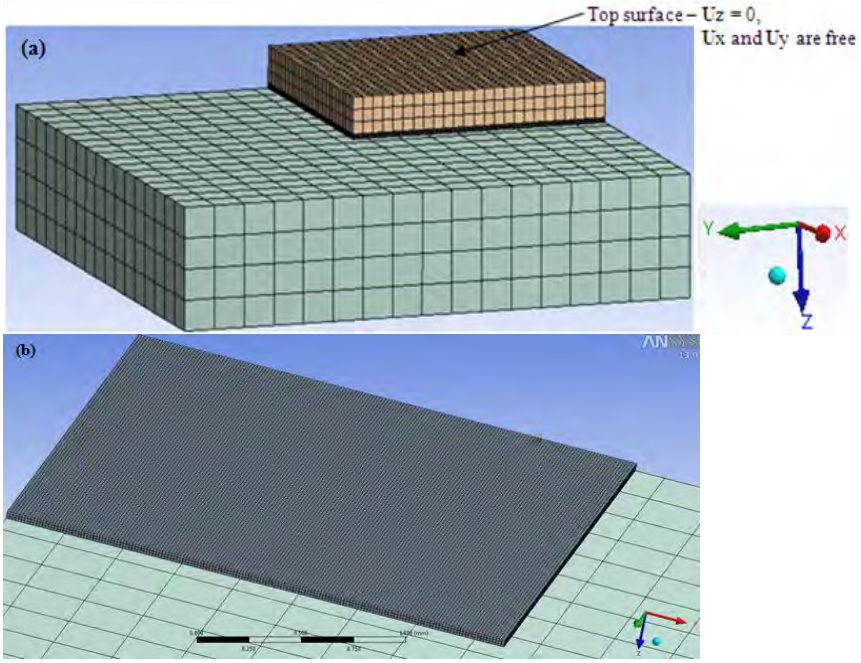



Figure 5.2-5: (a) 3-D meshed model showing the silicon die, solder layer and copper heat spreader. The top surface of the silicon die was fixed in z direction and displaced in the x and y directions (b) a cross-section view of the meshed model showing refined mesh around the solder layer and a relatively coarser mesh in the copper heat spreader

#### *5.2.1.1 Material properties*

The 3D geometric model consists of different layers of materials. The silicon die and copper heat spreader are assumed to be linear elastic with temperature dependent properties as shown in Table 5.2-3. The solder joints are modelled with linear elastic coupled with visco-plastic material properties. The linear elastic properties of the solder joints are shown in Table 5.2-3. A unified inelastic strain theory precisely the Anand's [205] visco-plastic material model is employed to accurately model the plastic behaviour of the SAC alloys under temperature and strain-varying load. The Anand model values for the SAC alloys are listed in Table 5.2-4.

Table 5.2-3: Linear material properties

| Properties | Materials | | | |
|---|---|---|---|---|
| | **Silicon die[226]** | **Copper [226]** | **SAC305[227]** | **SAC405[228]** |
| $E$(GPa) | 132.46-0.00954 $T$(K) | 141.92-0.0442$T$(K) | 38.7 | 49 – 0.07$T$($^o$C) |
| $a$ (ppm/$^o$C) | 2.113 + 0.00235 $T$(K) | 15.64 +0.0041 $T$(K) | 21 x $10^{-6}$ | 21.301 + 0.017$T$ ($^o$C) |
| $v$ | 0.28 | 0.35 | 0.35 | 0.38 |
| $\rho$ (x$10^{-6}$kg/mm$^3$) | 2.32 | 8.96 | 8.41 | 7.4 |

Table 5.2-4: Anand model constants for SAC305 and SAC405 alloys

| **Parameter** | **SAC305[75]** | **SAC405[229]** |
|---|---|---|
| $s_o$ (MPa) | 45.9 | 20 |
| $Q/R$ (1/Kelvin) | 7460 | 10561 |
| $A$(1/s) | 5.87 x $10^6$ | 325 |
| ξ (dimensionless) | 2 | 10 |
| $m$(dimensionless) | 0.0942 | 0.32 |
| $h_o$ (MPa) | 9350 | 8 x $10^5$ |
| ŝ (MPa) | 58.3 | 42 |
| $n$(dimensionless) | 0.015 | 0.02 |
| $a$(dimensionless) | 1.5 | 2.57 |

#### *5.2.1.2 Loads and boundary conditions*

Only thermal cycle load is considered in the FEA since most fatigue failures of CSPs are due to cyclic thermo-mechanical stress and strain in the solder joints [230]. The choice of the nature of the thermal loads used in evaluating the reliability of the SAC alloys is crucial considering that the relative performance of the different Pb-free solders could change with the thermal load parameters such as temperature range. Nonetheless, it is vital that the chosen thermal load reflects the service conditions of the electronic device being considered (in this case, automotive applications). Hence, the FE study was carried out using three different thermal cyclic loading conditions as shown in Figure 5.2-6. The three cases of thermal loads employed are:

- Case A: Thermal cycle ranging from -55°C to +85°C (JEDEC Standard [225]) with 20 minutes dwell at the peak and lowest temperature, the cooling and heating (ramp) rate is 10°C/min. This temperature cycling profile is selected because it is sufficient to test semiconductors in automotive applications situated in the passenger's compartment [231].
- Case B: Harsh temperature cycling between -55°C and 125°C (JEDEC Standard [225]) with 20 minutes dwell at the peak and lowest temperature, the ramp rate is 10°C/min. This thermal cycling range is also suitable for testing microelectronics applications under the hood of automotive [231].
- Case C: Harsher thermal load in the range of -65°C to +150°C (JEDEC Standard [225]), with 20 minutes dwell at the peak and lowest temperature, the ramp rate is 10°C/min. This profile is chosen particularly for testing devices mounted on-engine of an automotive and for applications of semiconductors in power supply controllers [231-232].

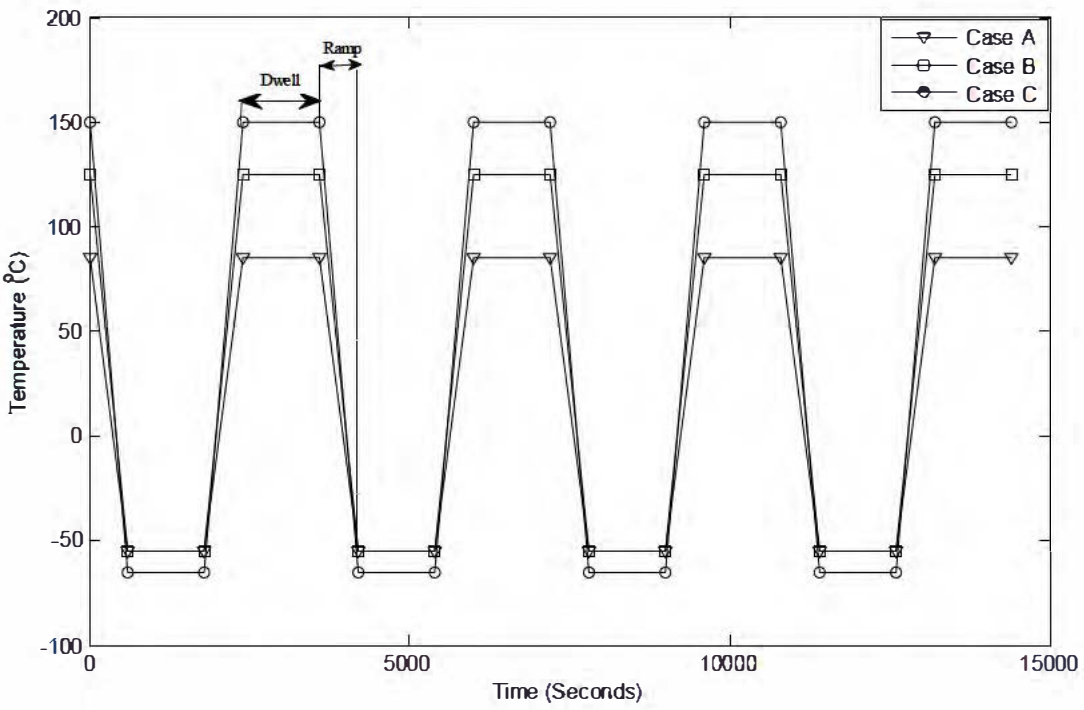



Figure 5.2-6: Temperature cycle profiles used in the simulation

#### *5.2.1.3 Assumptions*

The geometric model of the assembly includes several details for an accurate simulation of the Pb-free solder die-attach. Nonetheless, in order to simplify the FEM study, certain assumptions were made. Some of the assumptions made in the model are:

- All materials including the solder joint were assumed homogenous, process variations were not considered
- This work ignored the growth of inter-metallic (IMC) compounds at different temperatures and has addressed the solder joint as a monolithic entity with one constitutive equation. A recent study [233] on IMC layer reported that factors such as grain shape, randomly distributed grain boundary defects, thickness of the IMC layer and morphology of the solder/IMC interface have an effect on the microcrack patterns and the overall mechanical response of solder joints. These factors are traded off for an in-depth comprehension of the impacts of different numerically generated solder void patterns on thermo-mechanical performance of solder joint. It is also worth noting that the computing efficiency and time would dramatically decrease and increase, respectively with the incorporation of a supposedly thin IMC layer into a STIM layer of 0.04mm thickness
- Linear elastic behaviour was assumed for the package materials except the solder joint

## 5.3 Thermo-mechanical simulation results

The simulation results are discussed in terms of stress and inelastic strain distributions in the solder joints.

### 5.3.1 Study on equivalent von-Mises stress

The thermally induced stresses in the solder joints are due to variations among the CTE of different bonded materials that constitute the electronic package assembly, when exposed to temperature cyclic loading. The time history plot of the stress distributions for SAC305 and SAC405 solder joints under the different temperature cycling conditions are shown in Figure 5.3-1and Figure 5.3-2, respectively. The thermal cycle profiles are superimposed on the plots with ordinate axis as the secondary axis to assist explanation. As seen in Figure 5.3-1and Figure 5.3-2, the cyclic stresses in the solder joints under the different thermal load cases follow similar trend though with variations in magnitude. After the first thermal cycle, the solder joints reach a stabilised cyclic pattern where the highest stress is experienced at the beginning of the low temperature dwell and the lowest stress at the end of the high

temperature dwell because of the viscous behaviour of the joints. Low stress occurs during the high temperature phase of the thermal cycling load, while high stress corresponds to the low temperature phase. Stress relaxation happens both at the high and low temperature dwell phase due to creep effect.

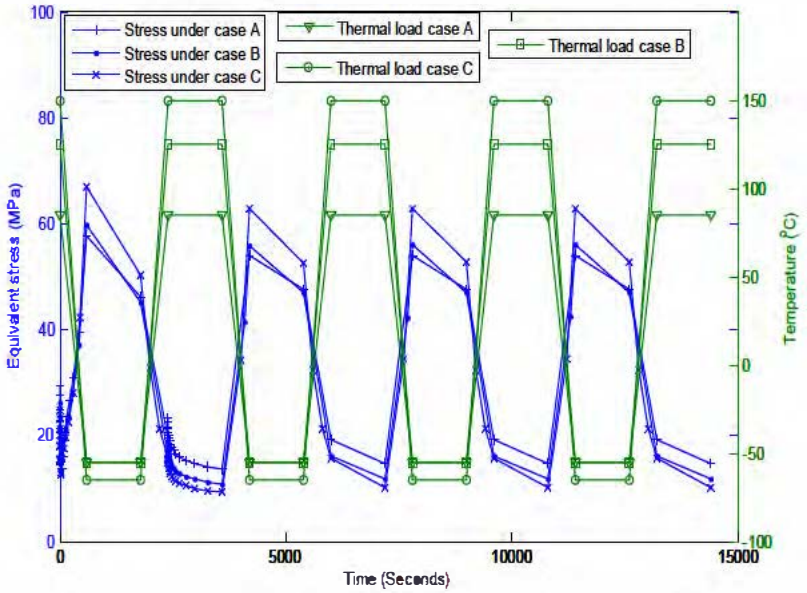



Figure 5.3-1: Stress evolutions in SAC305 solder joints

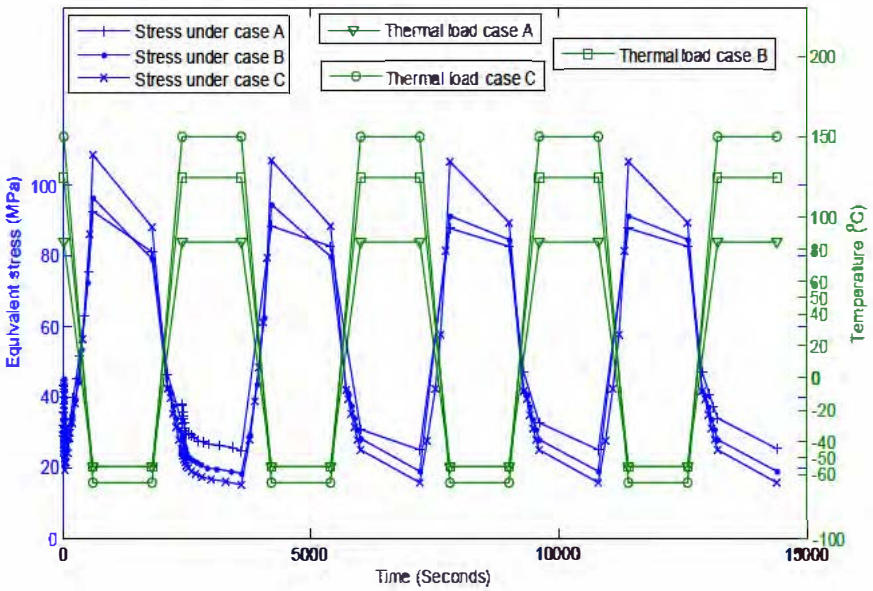



Figure 5.3-2: Stress evolutions in SAC405 solder joints

Figure 5.3-1 and Figure 5.3-2 show that the induced stress in SAC305 and SAC405 solder joints rises with increasing thermal load. For SAC305, the induced stress is relatively highest with a maximum value of 66.88MPa under thermal load of case C, which is the highest temperature range. Case A which comparatively has the lowest thermal range resulted in a maximum stress value of 57.70MPa which is lower than the 59.81MPa observed under case B temperature profile for SAC305 solder joint. Similar trend of maximum stress values increasing with temperature cycle ranges was also observed for SAC405 joint. With regards to SAC405, the maximum induced stress was 108.68MPa, when exposed to temperature cycle loading of case C, 96.34MPa under case B thermal profile and 92.57MPa when subjected to case A temperature load.

The variations in the stress levels result from the difference in the thermal cycle profiles. Expectedly, the higher the temperature load (thermal cycle range), the more the magnitude of the induced stress in the joints and vice versa. Stress in the solder joint is defined by the following equation.

$$\sigma = \frac{F_{max}}{A_{STIM}} \qquad (5.3\text{-}1)$$

Where $\boldsymbol{\sigma}$ is the thermally induced stress, $F_{max}$ is the thermal load and $A_{STIM}$ is the area of the STIM joint.

#### *5.3.1.1 Effect of Ag content on SAC solder joints stress behaviour*

Figure 5.3-3 - Figure 5.3-5 show that under the same thermal cycle condition, the cyclic stress in SAC405 solder joint is significantly higher than that in SAC305. This suggests that stress in the SAC solder joints appreciably rises as the Ag content of the solder increases. Similar result trend was reported in the experimental work of Kariya et al. [212] for flip-chip solder bumps. This is because the lower Ag content in SAC305 compared to SAC405 reduces the elastic modulus (strength) of the solder joint and thereby increases the ductility which tends to absorb more of the induced stress in the joint[218]. No wonder some studies [219] have suggested that SAC305 performs better than SAC405 in drop/impact test where the behaviour of the materials is dominated by elasticity.

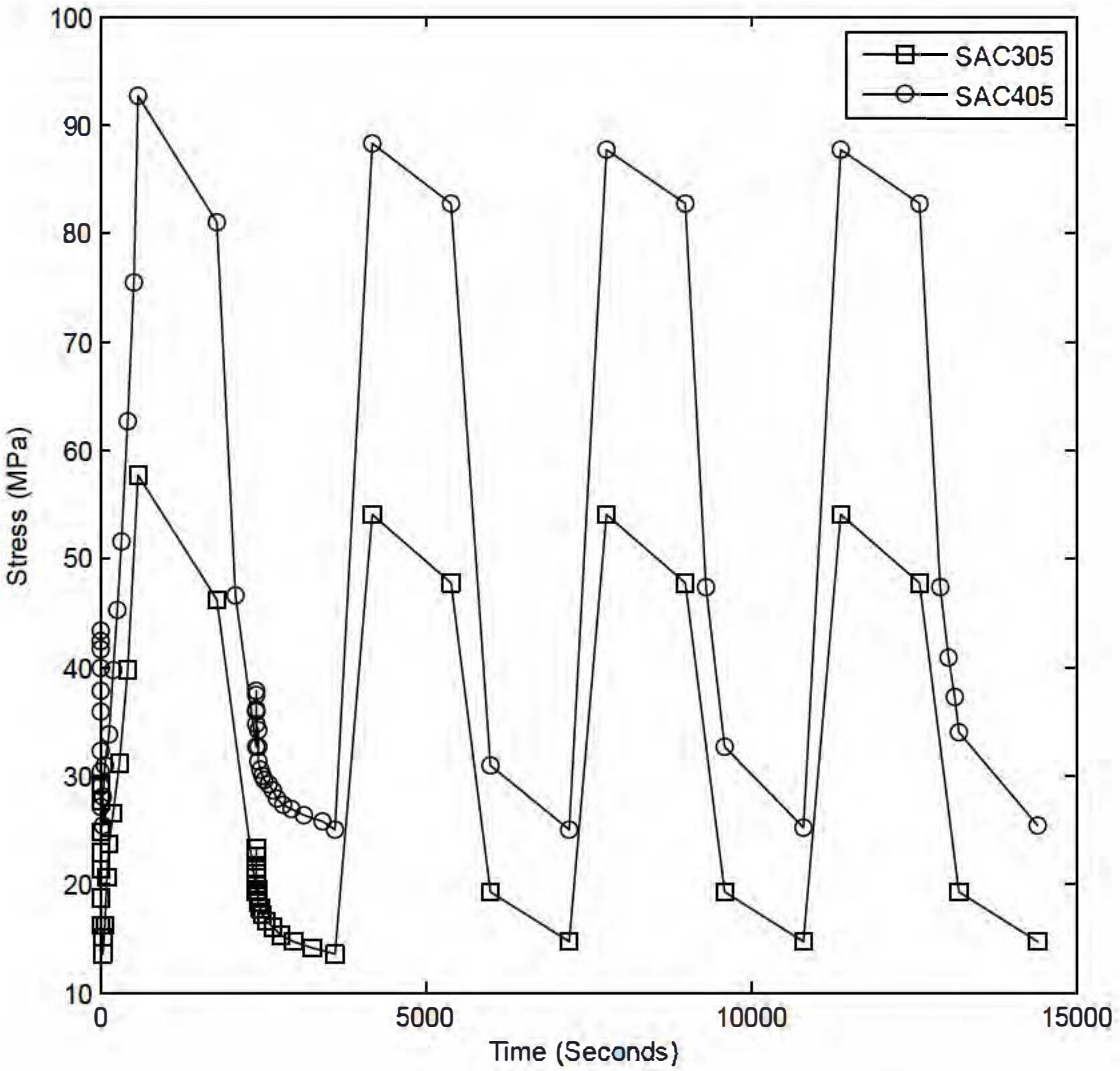



Figure 5.3-3: Effect of Ag content on stress evolution for SA C305 and SAC405 under thermal load case A

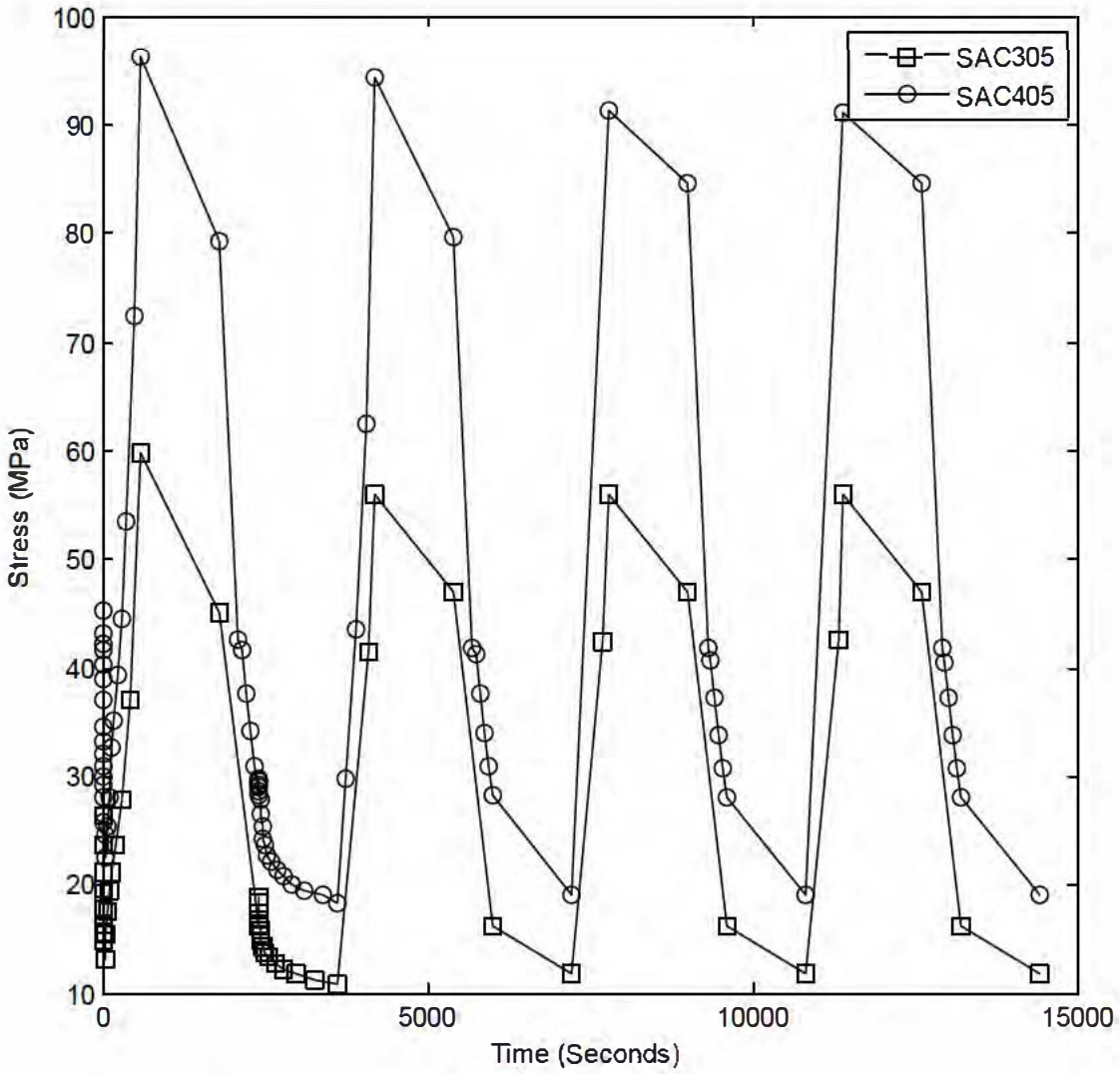



Figure 5.3-4: Effect of Ag content on stress evolution for SAC305 and SAC405 under thermal load case B

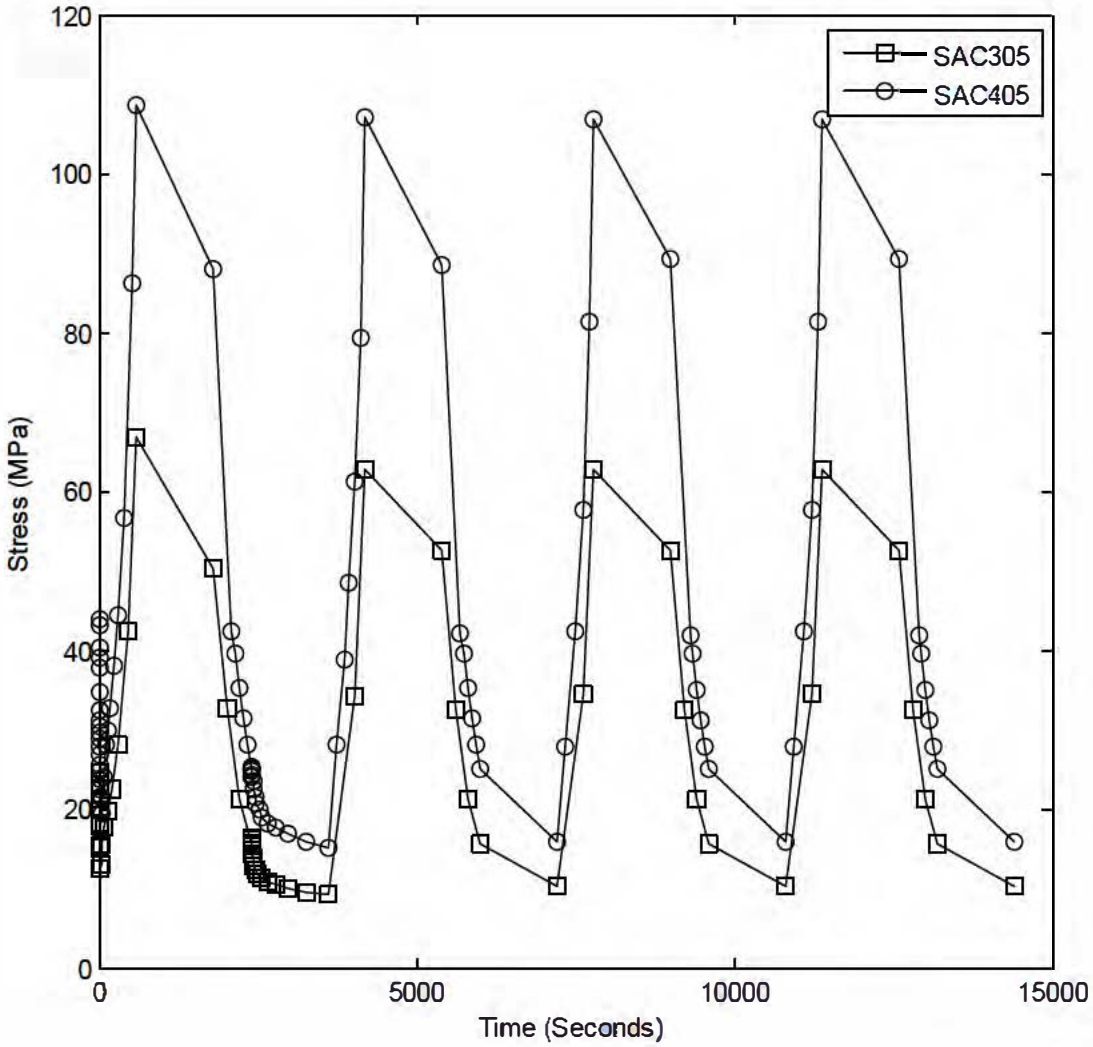



Figure 5.3-5: Effect of Ag content on stress evolution for SAC305 and SAC405 under thermal load case C

The percentage rise in the maximum stress value for SAC405 as compared to SAC305 is about 60% under thermal load case A, 61% when exposed to case B thermal loading and 63% when subjected to case C cyclic temperature profile. Hence, the different thermal cycle ranges appear not to have a considerable effect on the maximum stress rise for SAC405 in comparison to SAC305 across the three studied thermal load cases.

Visual inspection revealed that stresses are relatively higher in the corner region of the studied SAC solder joints for all thermal load cases as depicted in Figure 5.3-6(a-c) and Figure 5.3-7(a-c) independent of the Ag content. The magnitude of the stress appears to increase with higher thermal cycle range.

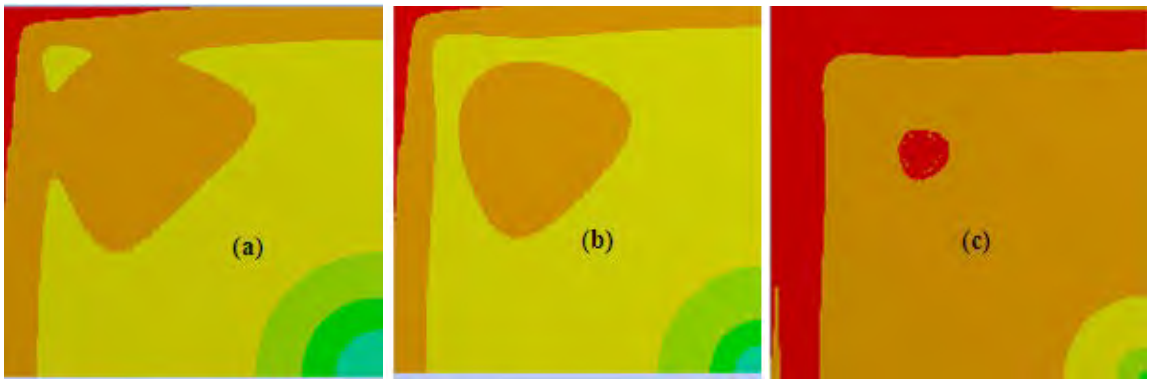



Figure 5.3-6: Red colour indicates area of maximum stress in SAC305under (a) thermal load case A (b) thermal load case B (c) thermal load case C

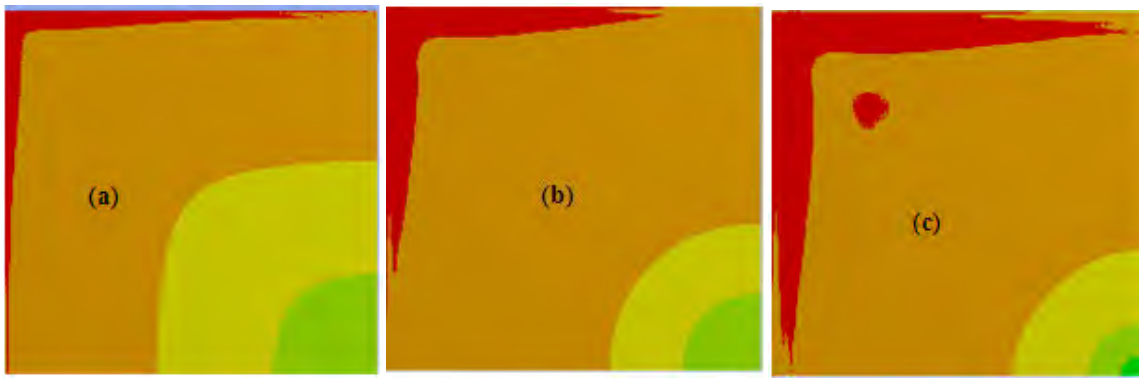



Figure 5.3-7: Red colour indicates area of maximum stress in SAC405under (a) thermal load case A (b) thermal load case B (c) thermal load case C

### 5.3.2 Study on strain energy

The work done by external loads in producing damage in a body is stored within the body as strain energy. Figure 5.3-8 and Figure 5.3-9 depict that strain energy accumulates in the studied SAC305 and SAC405 solder joints as thermal cycle progresses. For each SAC solder alloy, higher rate of strain energy accumulation is predicted for higher temperature cycle range as shown in Figure 5.3-8 and Figure 5.3-9 for SAC305 and SAC405 solder die-attach, respectively. Damage is expected to initiate in the solder when the accumulated strain energy reaches a critical value.

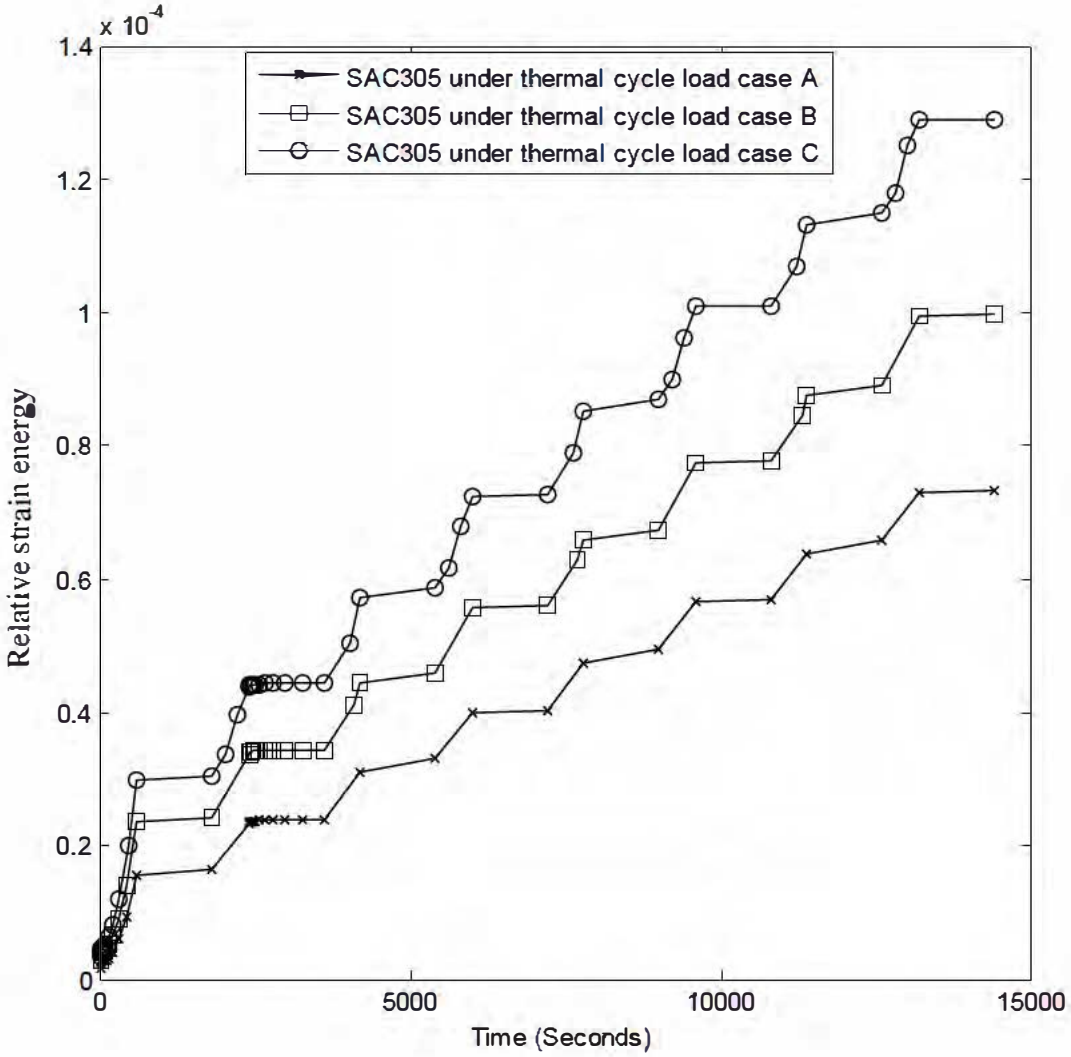



Figure 5.3-8: Strain energy in SAC305 under the different thermal cycle load cases

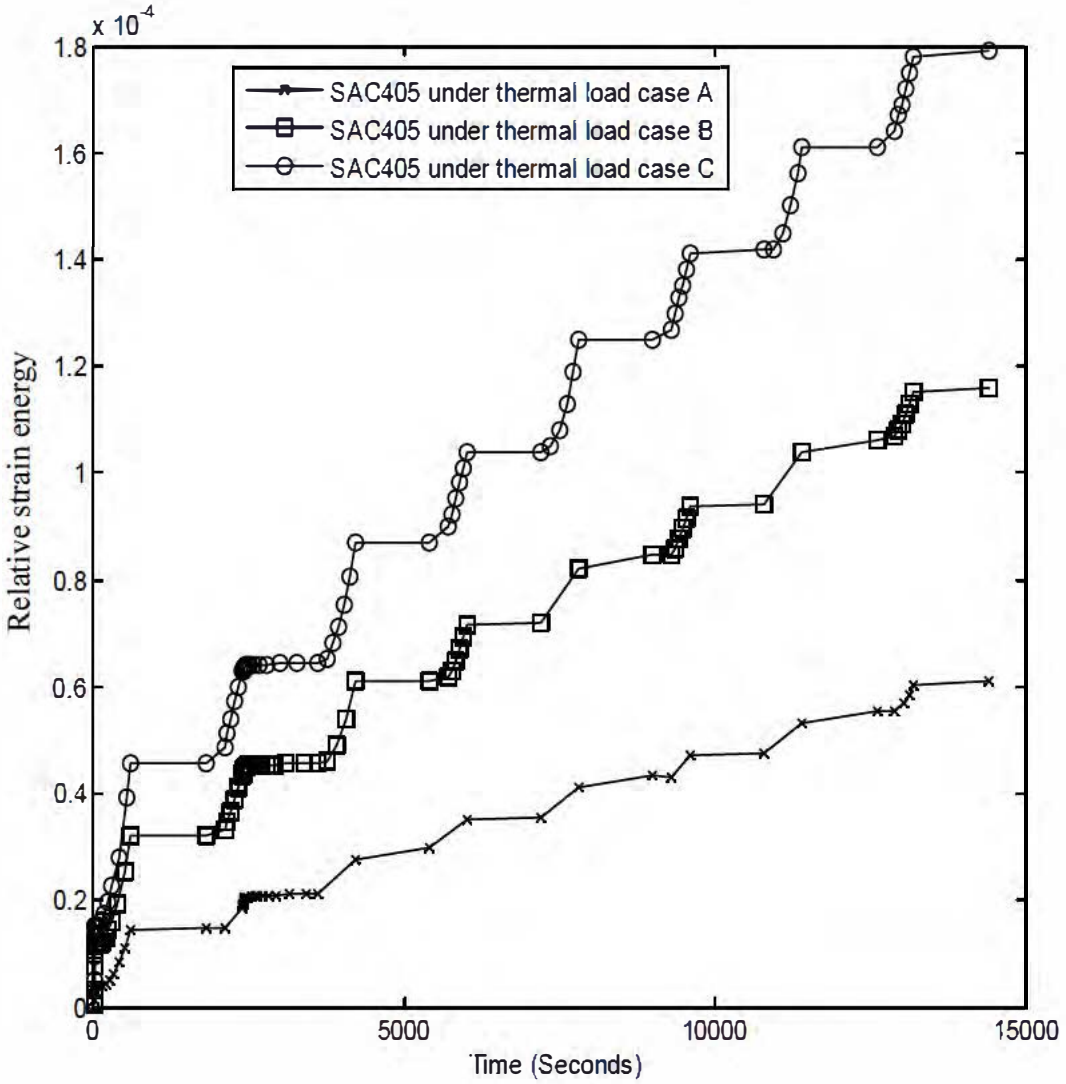



Figure 5.3-9: Strain energy in SAC405 under the different thermal cycle load cases

### 5.3.2.1 Effect of Ag content on the location of maximum strain energy in the SAC alloys

Visual inspection (Figure 5.3-10(a-c) and Figure 5.3-11(a-c)) show that the location of the maximum strain energy is similar for both SAC305 and SAC405 solder joints under all thermal cycle load cases regardless of the Ag content though with different strain magnitude. This suggests that concentration region of maximum strain energy in the studied solder joints is independent of the Ag content of the SAC solder alloys. The maximum strain energy concentrates in a small region at the edge of the solder joint and occupies a shallow depth from the surface of the solder joint region near the silicon die. This concentration region for maximum strain energy is referred to as the "critical region" in this study. Fatigue damage

often initiates and propagates from the critical region when the accumulated cyclic strain energy reaches a certain level for crack initiation [234-235]. The damage initiation site as observed from the FEA of the SAC solder joints is analogous to that observed in the experimental work of Stinson-Bagby [236] that showed crack initiation and propagation from the edge of the solder near the silicon die as shown in Figure 5.3-12. This result may have been influenced by the significant mismatch between the CTE of silicon and solder.

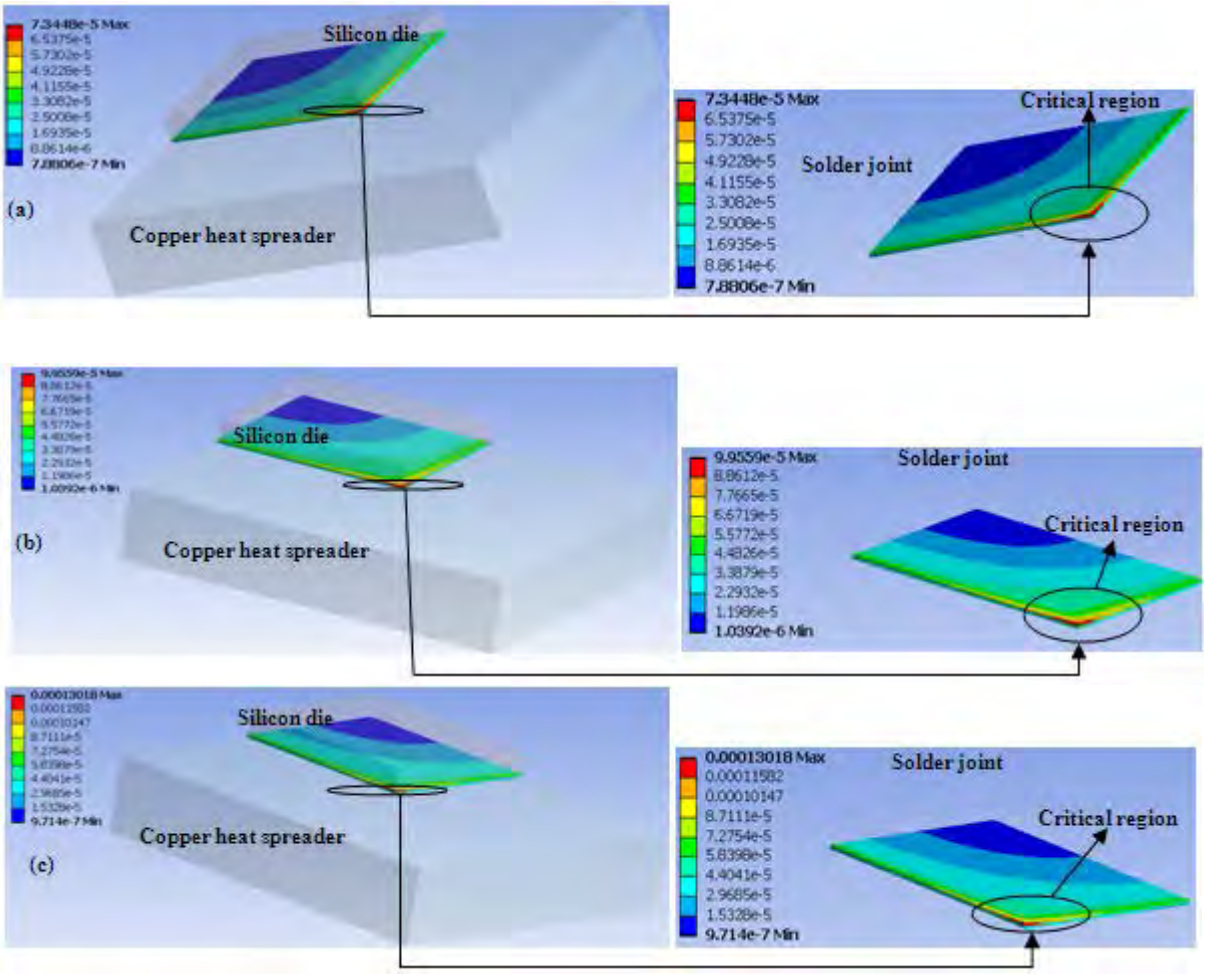



Figure 5.3-10: Location of critical region in SAC305under (a) thermal load case A (b) thermal load case B (c) thermal load case C

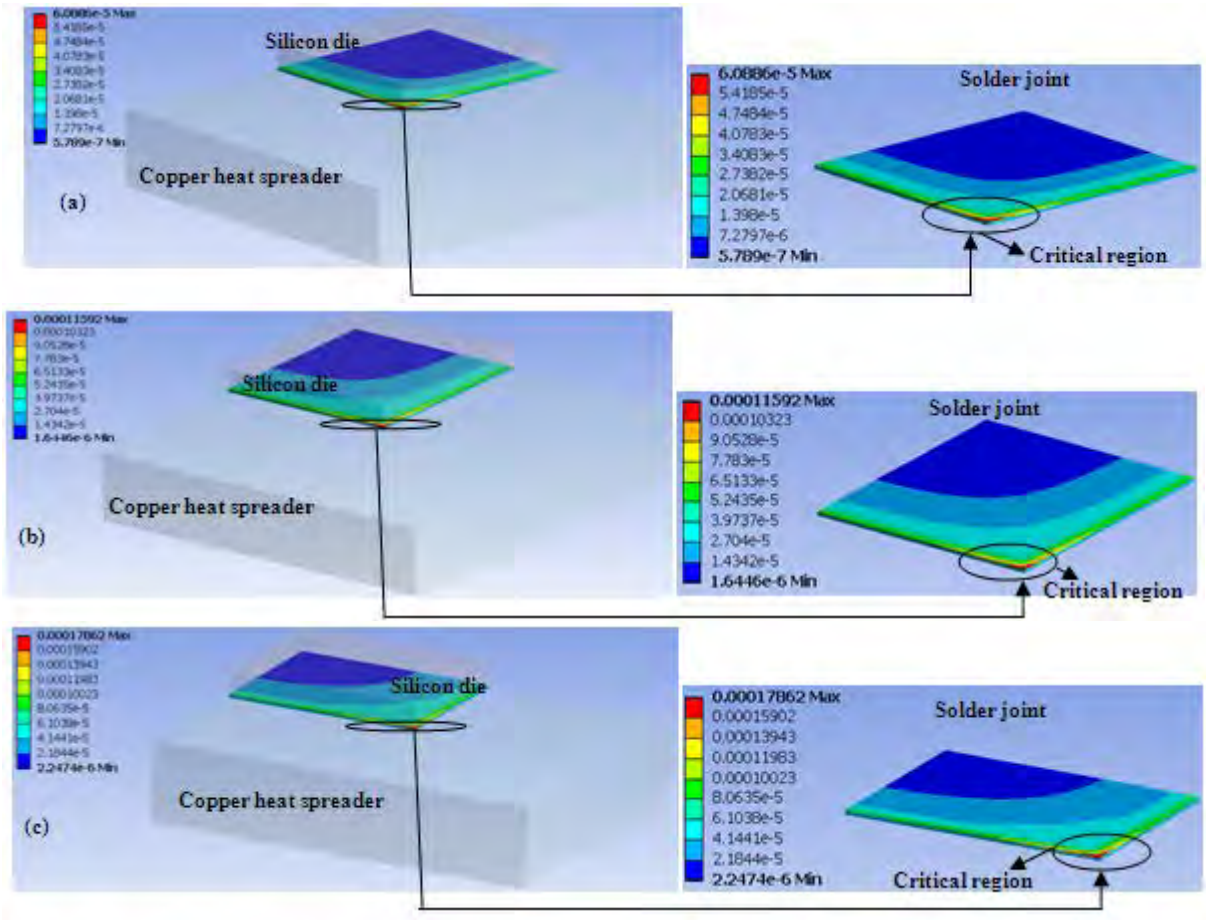



Figure 5.3-11: Location of critical region in SAC405under (a) thermal load case A (b) thermal load case B (c) thermal load case C

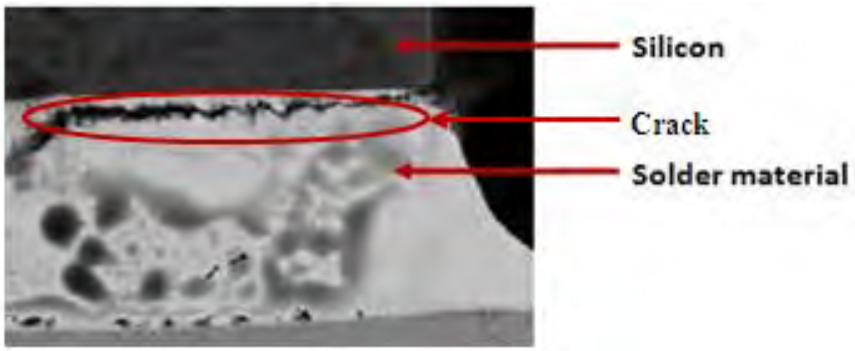



Figure 5.3-12: Image of crack that developed from the solder side near the silicon die at the point of highest calculated strain [236]

The location of the damage initiation in the studied SAC solder joints appears to be governed only by the nature of the materials and loads as the point of the highest strain energy is similar for both SAC alloys under all cases of thermal cycling independent of the Ag content.

### 5.3.3 Study on plastic work density

A body accumulates plastic work (Wpl) when external loads imposed on the body induce inelastic strain in the body. The plastic work per unit volume is referred to as the plastic work density. Thermal load on the chip-scale package induces plastic work on the solder die-attach used to couple the heat spreader to the silicon die. The plastic work for each element of the solder volume was extracted from ANSYS post-processing using the Element Table (ETABLE) command. ETABLE is a "spreadsheet" of element information within ANSYS. In order to minimise the mesh dependency of plastic work values, the plastic work value of each element is normalised by the volume of the element [237]. The volume averaged plastic work (plastic work density) $\Delta W_{pl,avg}$ can be numerically expressed as:

$$\Delta W_{pl,avg} = \frac{\sum_{i=1}^{n} W_{pl,i} . v_i}{\sum_{i=1}^{n} v_i} \qquad (5.3\text{-}2)$$

Where $\Delta W_{pl,avg}$ is the volume averaged plastic work in the solder volume made up of n elements ($i$=1- $n$), $W_{pl,i}$ is the plastic work in the $i$th element, and $v_i$ is the volume of the ith element.

Figure 5.3-13 shows that the relative trend of plastic work density plots for both SAC alloys under all cases of thermal loads is similar. The plastic work values are seen to increase with the thermal cycle numbers. As expected, the larger the temperature range, the larger the plastic work.

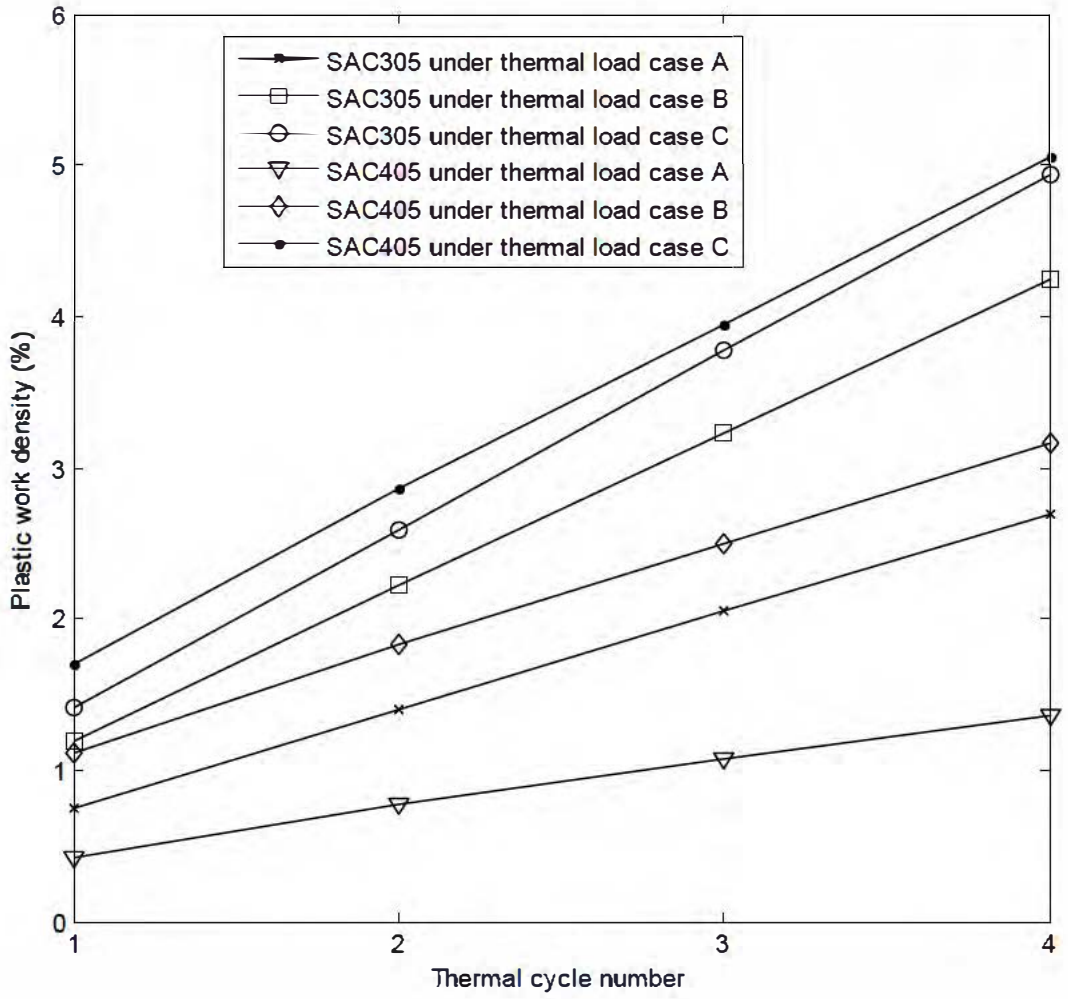



Figure 5.3-13: Plastic work density per thermal cycle under the three thermal load cases for SAC305 and SAC405

### 5.3.3.1 Accumulated plastic work

The change in the value of plastic work density over load step results in accumulated plastic work which is employed as a damage parameter for solder fatigue lifetime prediction [238]. The accumulated plastic work ($\Delta W_{pl}$) in one cycle for a given element can be written as equation (5.3.3):

$$\Delta W_{pl} = W_n - W_1 \qquad (5.3\text{-}3)$$

Where $W_n$ is the plastic work during the last load step of the cycle and $W_1$ is the plastic work during the first load of the cycle. This is further illustrated in Figure 5.3-14 with cycle 3 of the temperature cycle profiles.

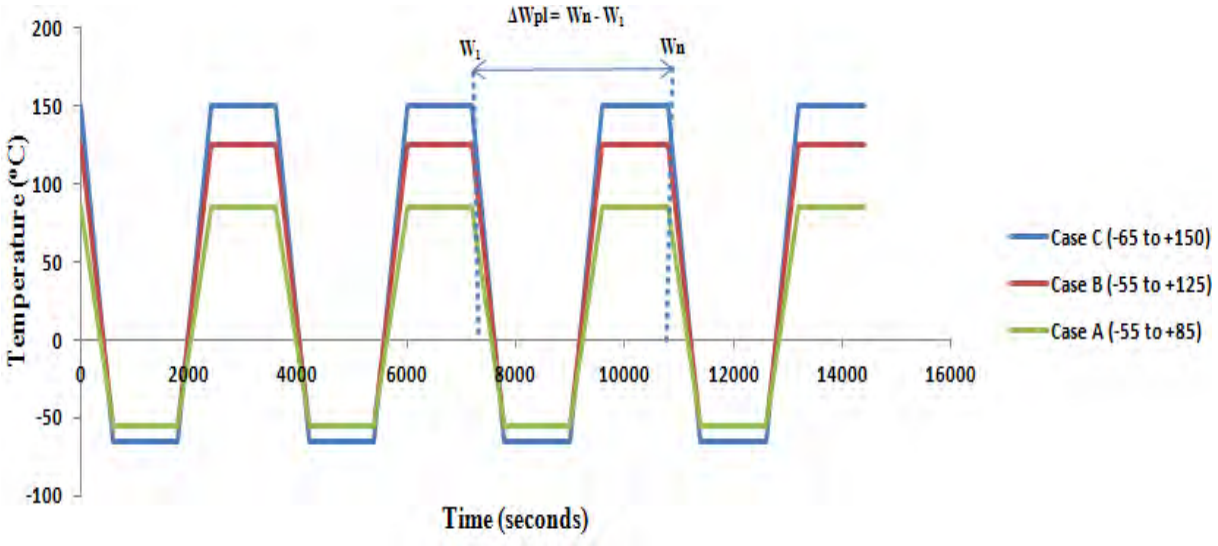



Figure 5.3-14: $W_1$ and $W_n$ respectively indicate the location of first and last load of cycle 3of the temperature cycle profiles.

Plots of accumulated plastic work values for both SAC solder alloys under the thermal load cases are shown in Figure 5.3-15 and Figure 5.3-16. It is observed from the plots that the magnitude of the accumulated plastic work generally varies with the number of cycles but tend to stabilise after the second cycle; the difference between the accumulated plastic work values for the third and fourth cycle is not significant. SAC405 showed slower stabilisation compared to SAC305 perhaps due to its reportedly higher stiffness (strength). Accordingly, the result from the stabilised cycle or the average of the extracted values of the damage parameter is used for further analysis. These values are shown in Table 5.3-1 for both SAC alloys for all cases of thermal loads. Unsurprisingly, the magnitude of accumulated plastic work rises as the thermal load increases for each of the SAC alloys. Based on the standard deviation of the set of values obtained for the accumulated plastic work for each SAC solder alloy under the three different thermal load cases as listed in Table 5.3-1, the accumulated plastic work for SAC405 appears to be more sensitive to the different thermal cycle ranges as its standard deviation value (0.0040) is relatively larger.

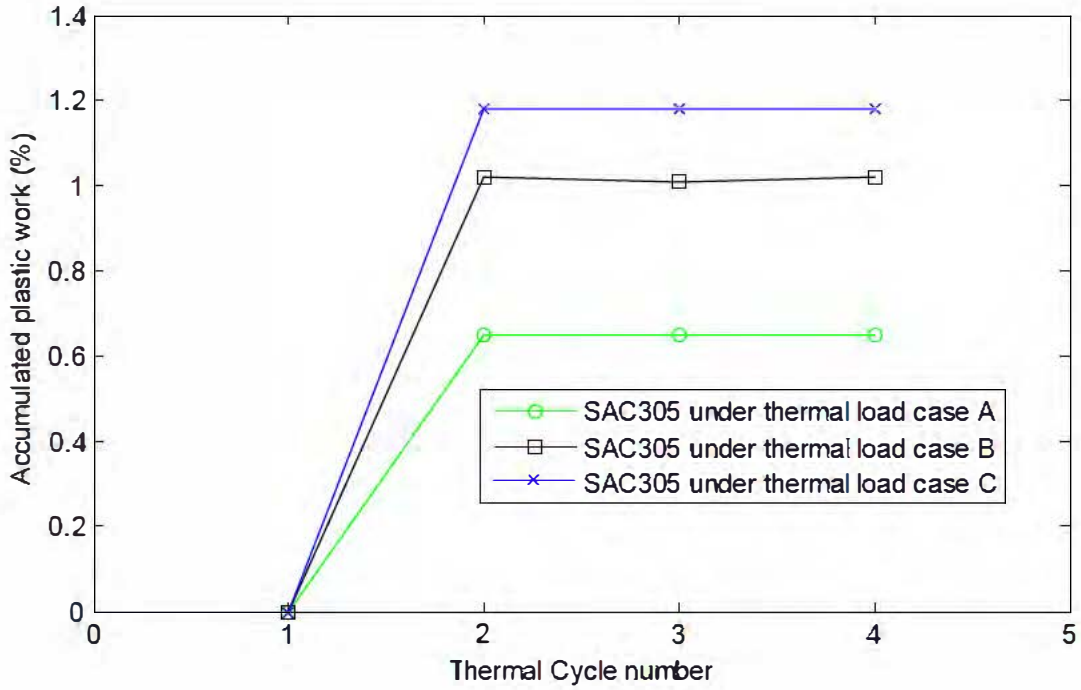



Figure 5.3-15: Accumulated plastic work for SAC305 under the three thermal load cases

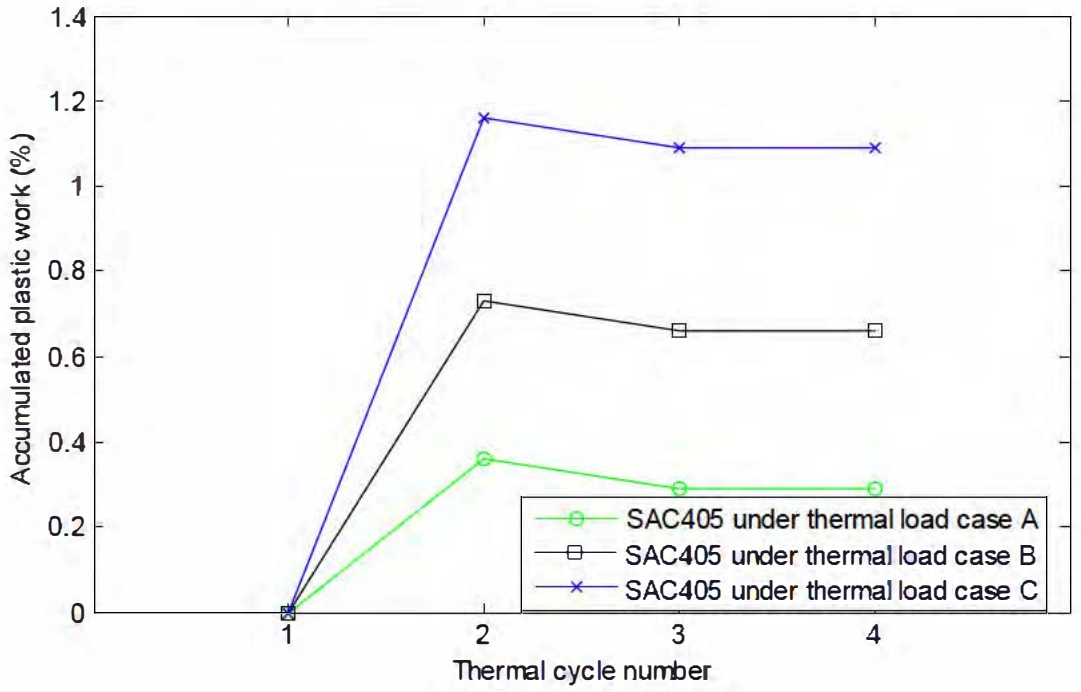



Figure 5.3-16: Accumulated plastic work for SAC405 under the three thermal load cases

Table 5.3-1: Volume averaged accumulated plastic work values obtained for the solder alloys under the different thermal load cases

| Solder alloy | Case A (-55°C to 85°C) (mJ/mm$^3$) | Case B (-55°C to 125°C) (mJ/mm$^3$) | Case C (-65°C to 150°C) (mJ/mm$^3$) | Standard deviation of the $\Delta W_{pl}$ values |
|---|---|---|---|---|
| **SAC305** | 0.0065 | 0.0102 | 0.0118 | **0.0027** |
| **SAC405** | 0.0029 | 0.0066 | 0.0109 | **0.0040** |

#### 5.3.3.1.1 Effect of Ag content on solder fatigue life

A higher accumulated plastic work indicates lower fatigue life and vice versa [238]. Figure 5.3-17 shows the comparison of the effect of Ag content on $\Delta W_{pl}$ for the different SAC alloy compositions solder die-attach under the thermal load cases. The results show that SAC305 consistently manifested higher magnitude of $\Delta W_{pl}$ compared to SAC405 under the same temperature cycle load. This suggests that an increase in the Ag content of the SAC alloys leads to relatively lower value of accumulated plastic work and subsequently enhances the thermal fatigue life of the solder die-attach. Hence, the thermal fatigue characteristic of SAC alloys as die-attach depends on the Ag content of the solders. This is attributed firstly to strengthening by an increase in the volume fraction of $Ag_3Sn$ dispersions in the higher Ag content alloy [210]. Secondly, the inter-particle space and grain size apparently decrease with increasing the Ag content in the SAC alloys [212]. This decrease in inter-particle space and grain size appears to increase the strength of the SAC alloy and results in less plastic deformation for higher Ag content SAC alloys compared to lower Ag content alloys. Thirdly, as observed in literature, the Young's modulus and CTE respectively increases and decreases with an increase in the Ag content of the SAC alloys; this implies that mismatches among the CTE of copper heat spreader, solder die-attach and the silicon die under thermal cyclic loading would be relatively less for SAC405 with higher Ag content in comparison to SAC305.

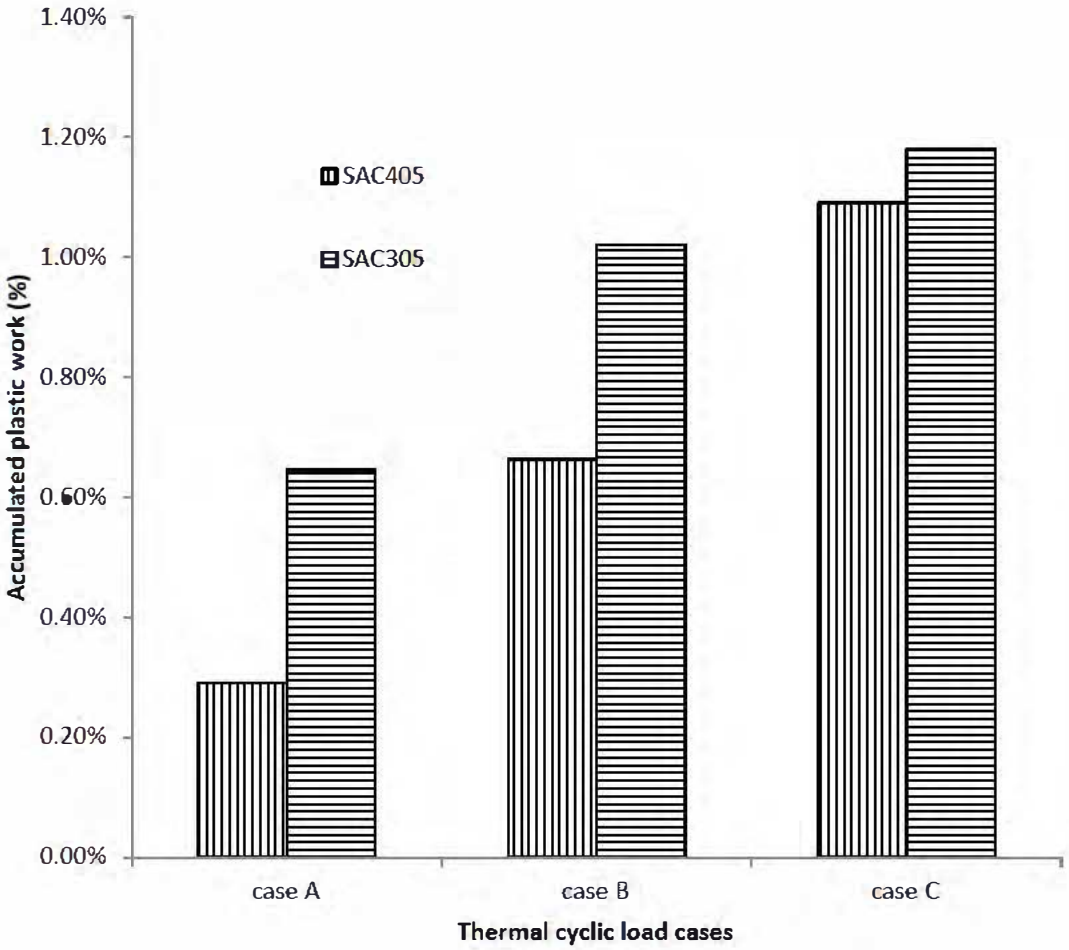



Figure 5.3-17: Effect of Ag content on accumulated plastic work for the SAC alloys under the three thermal cyclic load cases

The variations in the accumulated plastic work values obtained for both SAC alloys under the three thermal load cases were evaluated for comparison. The accumulated plastic work in SAC305 is about 124% more than that in SAC405, under thermal load case A; the damage parameters obtained for SAC405 are about 55% and 8% less than those for SAC305 when exposed to cyclic thermal load case B and case C, respectively. The difference in the accumulated plastic work values between SAC305 and SAC405 is seen to decrease as the thermal cycle range increases. In the authors' opinion, this could be attributed to the temperature dependent elastic modulus property of SAC405 (as shown in Table 5.2-3), the elastic modulus of SAC405 is seen to decrease as the reference temperature (highest temperature extreme in the thermal cycle) increases.

## 5.4 Application of conventional fatigue lifetime prediction model to large area solder joint

Fatigue lifetime models are used to determine the number of thermal cycles that a package can survive before failure. Extensive work has been done on the development of thermal fatigue life prediction models for solder joints leading to quite a fair number of models available in literature [230]. The fatigue models fall into the following categories –

- Stress based
- Energy based
- Inelastic strain amplitude (Coffin-Manson-type)
- Damage-mechanics-based
- Creep strain based

The different models depend on many factors like mode of cyclic loading, material type, deformation type and regime. Energy based approach is proposed for this study because it has the largest group of fatigue models and it is the most widely used model available for SAC lead-free solder [230]. In many of the work that has employed energy based approach, empirical data that validates the accuracy of the methodology is presented within +/-2x, which is considered state of the art for such complex analysis [190]. Several researchers have reported different energy based models for solder material. Most of the established fatigue models require a constant/parameter which is a measure of the damage accumulation per cycle. Many researchers [239-242] have generated different damage constants for these life prediction models for SAC alloys. Nonetheless, these model constants have been obtained and tested for small area solder joints like flip-chip solder bumps or BGAs. The model parameters are yet to be verified for large area solder joints to the authors' knowledge. Although it is claimed that the model constants can be used as long as 3-dimensional modelling and volume averaging techniques are employed [239], these model parameters could be dependent on solder joint geometry/shape [224] in as much as they rely on stress-strain history.

The method of employing damaged parameters averaged over certain thickness of element layers for fatigue lifetime prediction is questionable when the geometry/shape of the solder joint is different from flip-chip solder bumps or BGA solder joints (small area solder joints). For instance, the damage model parameters are averaged over 10% circular slice of volume around the critical region where the damage concentration is maximum for energy

partitioning model [243]. The model constants obtained through this method appeared to accurately predict the life of solder ball joints in BGA packages [244]. Ladani [245] has attempted using the same technique for large area solder joint where the damage constant was averaged over 10% of volume slice around the critical region but reported that the predicted life for the large area solder joint was significantly larger than the experimental results. This is because damage constants are for specific reference geometry of solder balls. In cases where the studied joint is different from the reference case like in large area solder joint, these constants cannot be used to correctly predict joint life time. Similar concern is perhaps applicable to other fatigue prediction models that employ damage constants averaged over certain volume of elements including Syed's creep strain based fatigue model [39] where a thickness of 25μm of the solder ball joint taken around the critical region was used. As these damaged parameters are conventionally extracted from a certain volume taken around a critical region in the height direction of the solder bump or solder ball, it is unclear the pattern of the chosen volume of elements in large area solder joints (such as the ones studied in this work). This is because the location of the maximum damage in large area solder joint is often at the corner region which has a different shape and orientation (Figure 5.4-1a) compared to the critical region in small area solder joint (Figure 5.4-1b).

Addressing the foregoing through rigorous experiments and FE modelling would form a basis for future work. It is good to know that Darveaux [237] has dealt with this concern of damage parameter sensitivity to element thickness in the solder height direction by suggesting different life correlation constants for various thickness of element layers selected for the damage parameter extraction. Nevertheless, Darveaux [237] has only implemented this technique for a small area Pb-based solder joint. Since the work reported in this study is a comparative study, the thermal fatigue reliability of the two studied SAC alloy compositions for die-attach application were evaluated using the critical values of the stabilised damage parameters extracted from the entire solder joint volume as reported in Section 5.3.3.1.

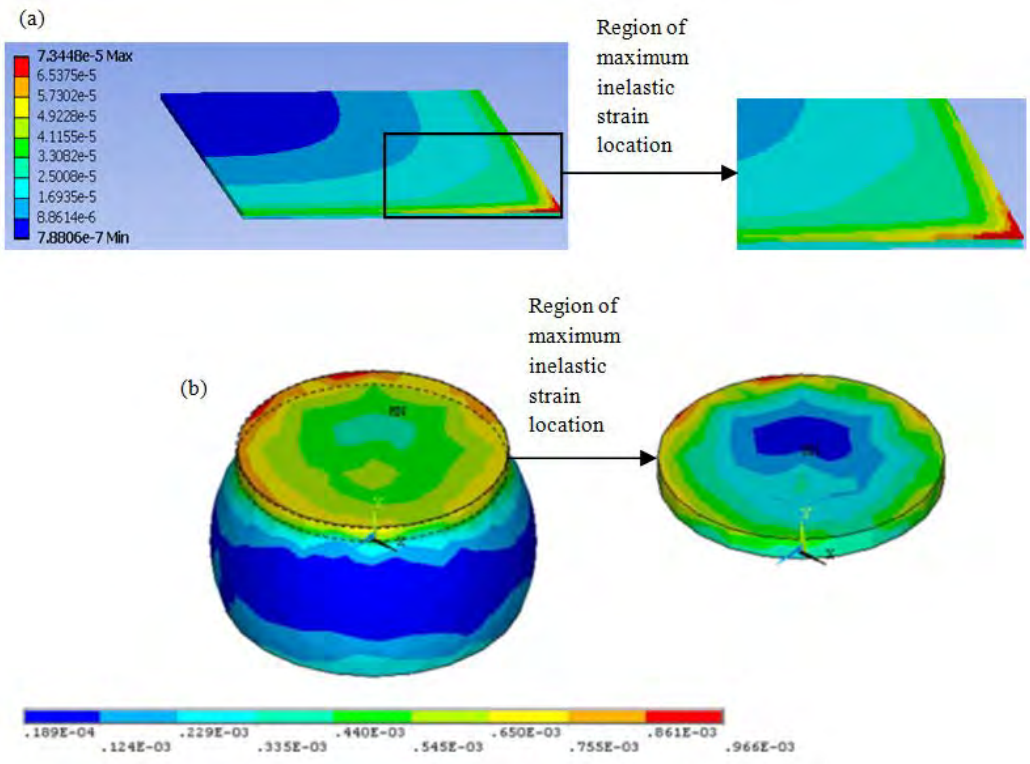



Figure 5.4-1: Critical region for (a) studied large area solder joint (b) BGA solder joint[246]

## 5.5 Summary

Research show that the optimal silver (Ag) content in the Sn-Ag-Cu alloys is crucial in fabricating a STIM that relatively has an improved thermal fatigue performance. Since SAC305 and SAC405 are the two standard SAC alloys and are both recommended by JEIDA and NEMI, respectively, finite element modelling was used to comparatively analyse the influence of Ag content for these two standard SAC alloy compositions on the thermal cycling reliability of solder die-attach, under three various cases of temperature cyclic loading conditions. The different temperature cycle profile investigation on the influence of Ag content for the SAC alloys has provided a deeper insight on the performance of SAC305 and SAC405 under different temperature applications. The key findings of the study are:

- The Von-Mises stresses and inelastic strains in each of the SAC solder die-attach were strong function of the thermal cycle profile, increasing in the order -55$^{o}$C to 80$^{o}$C < -55$^{o}$C to 125$^{o}$C < -65$^{o}$C to 150$^{o}$C.
- Under the same thermal cyclic loading condition, the range of stress was relatively greater for the SAC alloy solder die-attach with higher Ag content (SAC405) while the lower Ag content SAC solder (SAC305) experienced a comparatively larger

accumulated plastic work. This implies that SAC405 can sustain much higher stress before inelastic strain occurs.

- For all cases of cyclic thermal loading considered in this study, the maximum values of induced strain energy are all located in the corner regions of the studied solder joints at the side next to the silicon die, independent of the Ag content of the solder alloys. This is identified as the critical region and analogous to the crack path as observed in an experimental work elsewhere [236].
- Based on the extracted damage parameter, the thermal fatigue lifetime of the studied SAC alloy compositions for die-attach application increases as the Ag content of the solder rises. Hence, SAC405 has a better thermal fatigue resistance compared to SAC305.
- Based on the obtained standard deviation for the set of accumulated plastic work values, the accumulated plastic work in SAC405 is more sensitive to the studied thermal cycle ranges (-55$^{o}$C to 80$^{o}$C and -55$^{o}$C to 125$^{o}$C) compared to SAC305.
- The difference in accumulated plastic work values between SAC305 and SAC405 decreases as the thermal cycle range increases and is lowest (8%) under thermal load case C (-65$^{o}$C to +150$^{o}$C) compared to other studied cases of thermal cyclic loading (-55$^{o}$C to 80$^{o}$C and -55$^{o}$C to 125$^{o}$C).
- Considering that firstly, the difference between the accumulated damage for SAC305 and SAC405 decreases as thermal cycle range increases and lowest at thermal cycle load case C which is analogous to the harsh automotive ambient (between 125$^{o}$C to 150$^{o}$C); Secondly, the relatively lower flow stress of SAC305 could play a key role in the absorption of shock/vibration on electronic components for automotive application; thirdly, SAC305 is relatively less expensive compared to SAC405 which could be beneficial to the extreme cost constraints being undergone by the automotive industry - SAC305 is preferred especially for automotive applications and will be employed in subsequent parametric studies covering the effects of voids on the reliability of STIM.
- The method of employing damaged parameters averaged over certain thickness of element layers for fatigue lifetime prediction is questionable when the geometry of the solder joint is different from flip-chip solder bumps or BGA solder joints. As these damaged parameters are conventionally extracted from a certain volume taken around

a critical region in the height direction of the solder bump or solder ball, it is unclear the pattern of the chosen volume of elements in the studied solder die-attach.

# Chapter 6: Parametric study of solder voids: Numerical modeling – Part II

## 6.1 Introduction

In order to better understand the complex structural behaviour of solder die-attach with voids, an in-depth comprehension of the redistribution of strain and stress in the solder joint structure as a function of the voids size, voids distribution and voids location is required. These void features can be elucidated by a finite element modelling (FEM) approach. Hence, studies employing numerical method are proposed for an in-depth understanding of the precise contribution of different sizes, locations and configurations of lead-free solder voids to the performance of solder as TIMs. As recommended in the previous chapter, SAC305 will be employed for the finite element study on solder voids.

Owing to the different aspects of solder voids, they can be classified into groups or types. Hence, the solder void patterns under investigation include randomly distributed small voids and large voids; shallow voids and deep voids; corner/edge voids and centre voids. These various void types could have different level of impact on the reliability of solder die-attach and thus, the evaluation of the precise thermo-mechanical effects of these different void patterns is essential. The purpose of this chapter is to apply three dimensional (3D) finite element modelling (FEM) to a comparative study of the thermo-mechanical effect of different numerically controlled solder voids percentage, configurations and locations on SAC305 solder die-attachment layer of a chip-level packaged power device.

The chapter initially presents an FE model incorporating the STIM layer and other package layers including the chip and heat spreader. The FE model would include the material properties, dimensions of the different model layers and appropriate boundary conditions. To justify the finite element prediction, validation study is carried out and compared against an experimental work elsewhere. Finally, FEA parametric studies are carried out to investigate the effect of the different numerically generated random void configurations, sizes, volume fraction and locations on the thermo-mechanical performance of SAC305 alloy as STIM layer.

## 6.2 Finite Element Model

The 3D geometric model consists of different layers of materials as seen in Figure 6.2-1. Full models would be used for analysis considering that the finite element models with random voids (in the solder layer) generated via *MCRVEGen* algorithm are non-symmetrical. The dimensions of the layers that constitute the model assembly are listed in Table 6.2-1. The

dimension of the chip and corresponding solder die-attach layer is chosen to be 2.5mm x 2.5mm representative of one of the standard sizes of a real test die [247].

The finite element program subdivides the package into finite elements (mesh) as shown in Figure 6.2-2. The mesh for the model without solder void consists of 606,219 nodes and 120,564 elements. The same mesh distribution/concentration is used across all the cases investigated in a particular study to ensure correct comparison of the results.

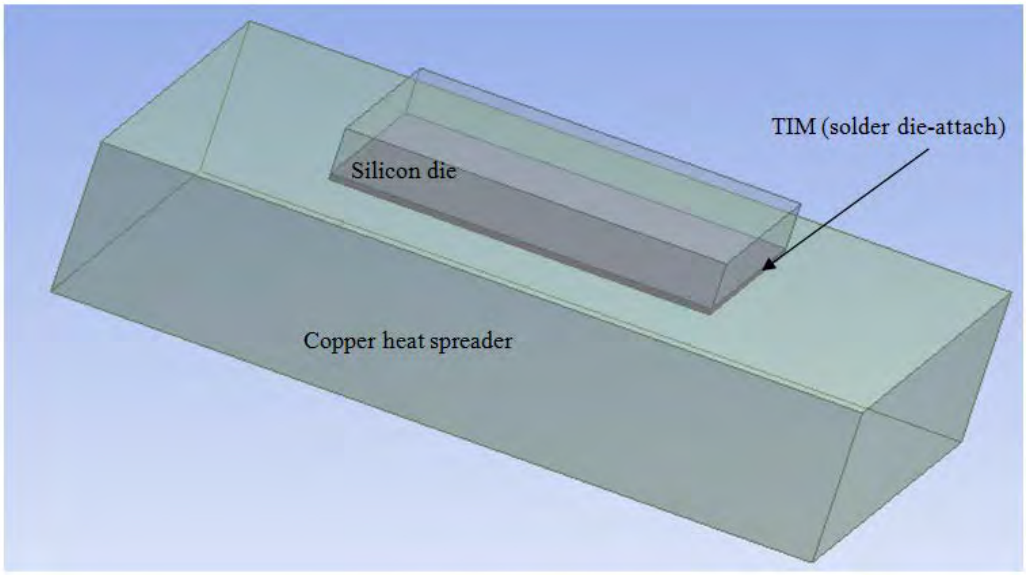



Figure 6.2-1: Model structure

Table 6.2-1: Dimensions of package assembly constituents for assemblies with voids generated via Monte Carlo approach

| **Parameter** | **Silicon die** | **Solder** | **Copper heat spreader** |
|---|---|---|---|
| Length | 2.5 | 2.5 | 5 |
| Width | 2.5 | 2.5 | 5 |
| Thickness | 0.3 | 0.04 | 1 |

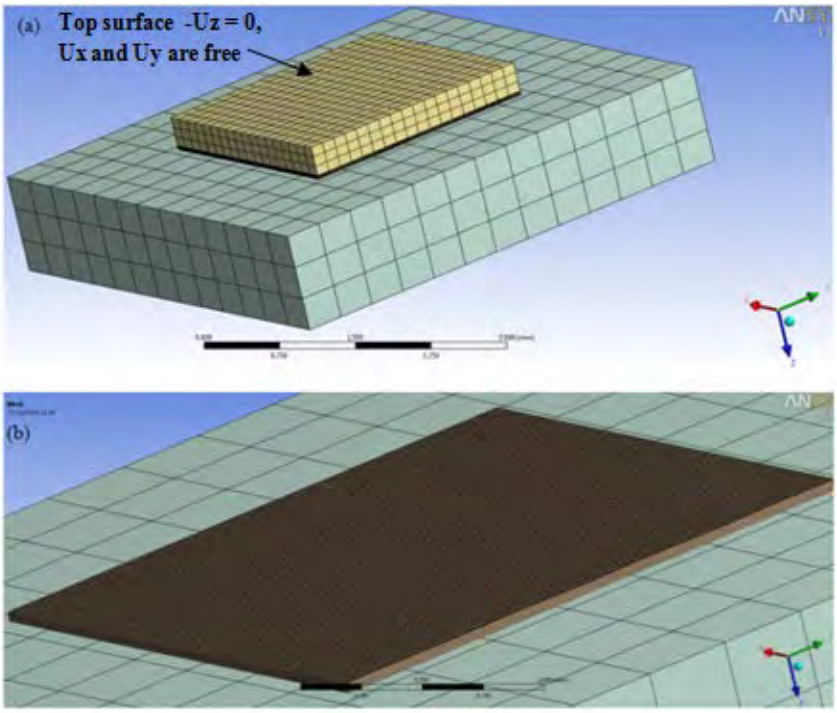



Figure 6.2-2: Example of a (a) 3-D meshed model showing the silicon die, solder layer without void and copper heat spreader. The top surface of the silicon die was fixed in z direction and displaced in the x and y directions (b) cross section view of the meshed model showing refined mesh around the solder layer and a relatively coarser mesh in the copper heat spreader

### 6.2.1 Material properties

The silicon die and copper heat spreader are assumed to be linear elastic with temperature dependent properties as shown in Table 6.2-2. The solder joints are modelled with linear elastic coupled with visco-plastic material properties. The linear elastic properties of the solder joints are shown in Table 6.2-2. A unified inelastic strain theory precisely the Anand's [205] visco-plastic material model is employed to accurately model the plastic behaviour of the SAC305 under temperature and strain-varying load. The Anand model parameters are shown in Table 6.2-3.

Table 6.2-2: Linear material properties

| **Properties** | **Silicon die[226]** | **SAC305[227]** |
|---|---|---|
| $E$(GPa) | 132.46-0.00954 $T$(K) | 38.7 |
| $a$ (ppm/$^{o}$C) | 2.113 + 0.00235 $T$(K) | 21 x $10^{-6}$ |
| $v$ | 0.28 | 0.35 |
| $\rho$ (x$10^{-6}$kg/mm$^{3}$) | 2.32 | 8.41 |

Table 6.2-3: Anand model constants for SAC305 alloy

| **Parameter** | **SAC305[75]** |
|---|---|
| $s_o$ (MPa) | 45.9 |
| $Q/R$ (1/Kelvin) | 7460 |
| $A$(1/s) | 5.87 x $10^{6}$ |
| $\xi$ (dimensionless) | 2 |
| $m$(dimensionless) | 0.0942 |
| $h_o$ (MPa) | 9350 |
| $\hat{s}$ (MPa) | 58.3 |
| $n$(dimensionless) | 0.015 |
| $a$(dimensionless) | 1.5 |

### 6.2.2 Loading condition

The FE study was carried out using harsh thermal cyclic loading (Case C in Chapter 5) in the range of -65$^{o}$C to +150$^{o}$C (JEDEC Standard [225]) as shown in Figure 6.2-3, with 20 minutes dwell at the peak and lowest temperature, the ramp rate is 10$^{o}$C/min. This profile is chosen particularly for testing devices mounted on-engine of an automotive.

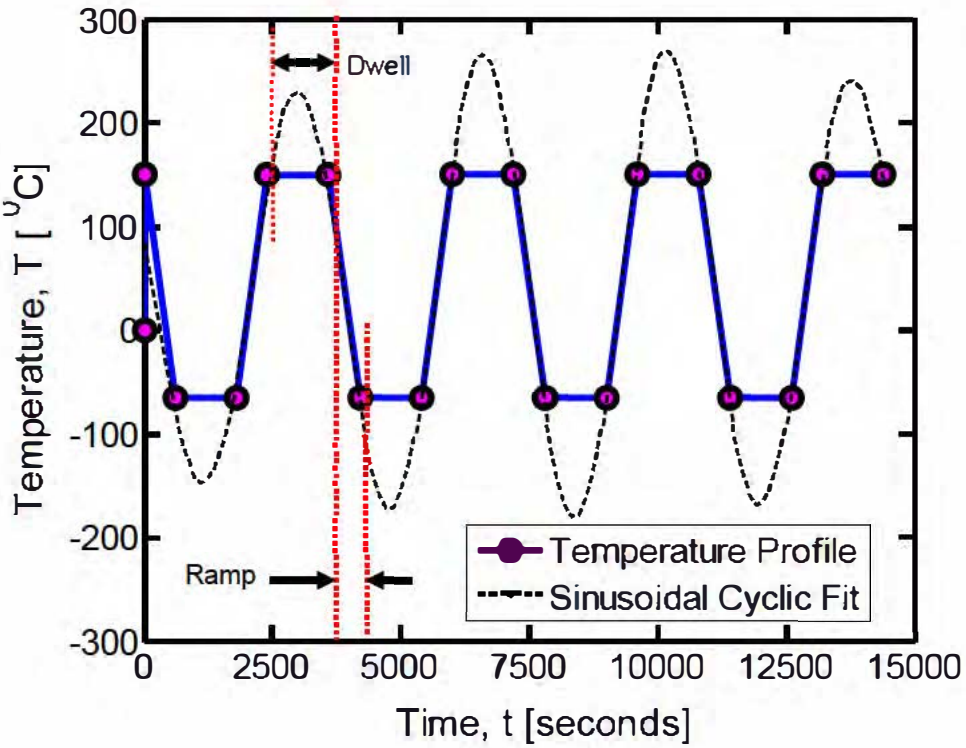



Figure 6.2-3: Temperature cycle profile used in the simulation (based on a sinusoidal cyclic fit)

### 6.3 Finite element results

Firstly, a case of joint without void is modelled and used as a base line. Figure 6.3-1 shows the region of the maximum localised strain energy concentration in the solder die-attach layer without void. FEA predicts the critical region (maximum damage site) to be a small region at the edge of the solder joint. This critical area occupies a shallow depth from the surface of the solder joint region near the silicon die and it is a potential damage initiation site. The critical site as observed in this study is comparable to that observed in the simulation (Figure 6.3-2a) and experimental work (Figure 6.3-2b) of Chang and McCluskey [248] that showed damage initiation and propagation from the edge of the solder near the silicon die. This result may have been influenced by the significant mismatch between the CTE of silicon and solder coupled with the fact that load significantly increases with 'distance-to-neutral-point (DNP)' in a chip-scale packaged component [75, 249]. The qualitative agreement between the result of this study and that of Chang [248] provides a level of confidence on the modelling technique adopted in this study. It should be noted that the study by Chang [248] is based on Indium solder die-attach layer.

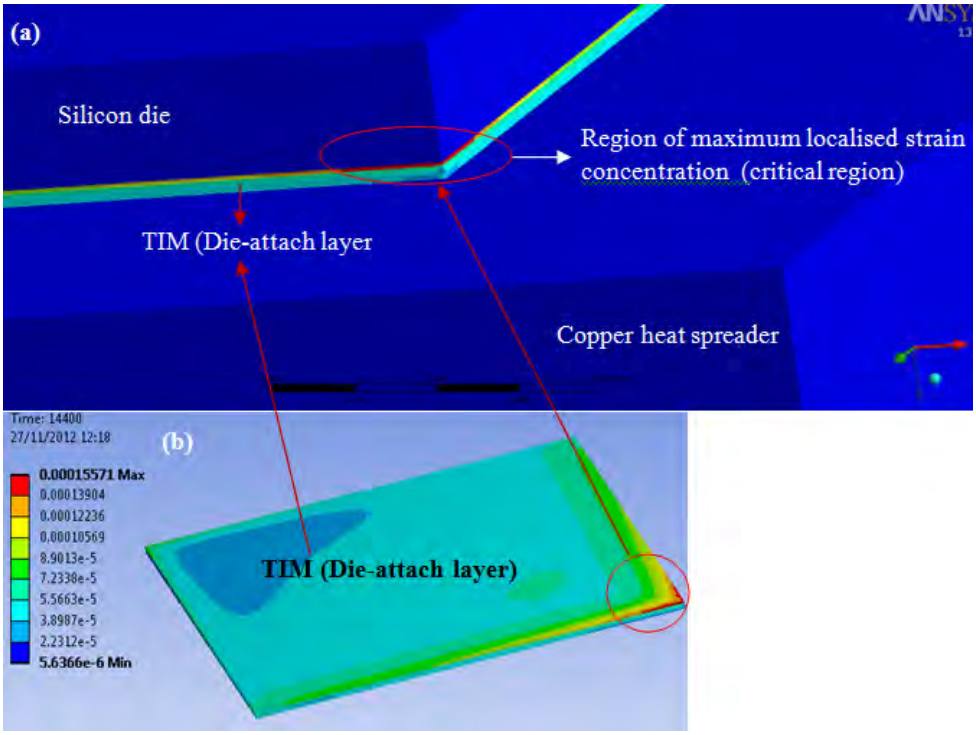



Figure 6.3-1: Contour plot of strain energy distribution showing (a) critical region in the corner of the SAC305 die-attach layer (b) only the die-attach layer with the critical region

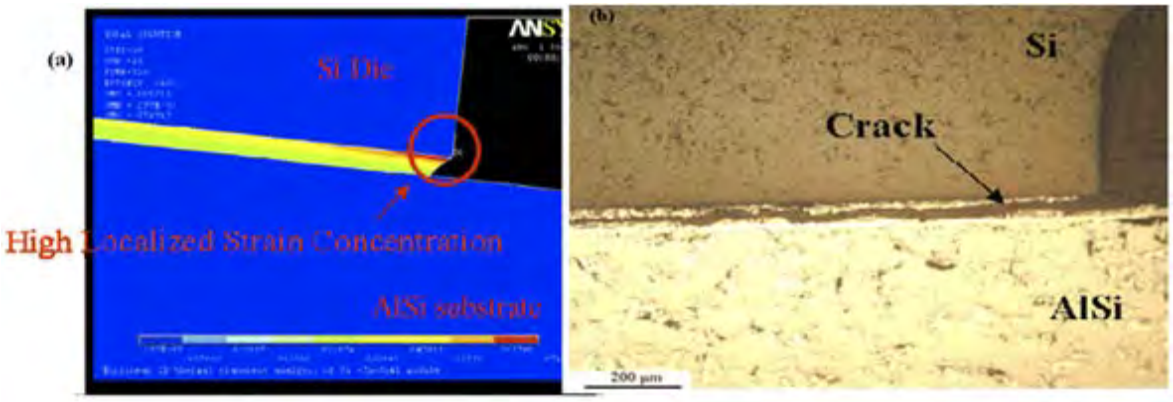



Figure 6.3-2: (a) contour plot of inelastic strain in FEA (b) fatigue failure of solder joint[248]

### 6.3.1 Study on void configuration (Small vs. Large voids)

With regards to void configuration, the formation of distributed small voids and large single coalesced voids is feasible. Large voids can be formed through the coalescence of smaller voids especially when the solder is in a molten state for long time [250]. Hence, in this study, the term "large coalesced void" is at times used for the numerically generated large voids.

The fatigue life of solder joints are functions of many factors such as the magnitudes of strain, stress and accumulated plastic work.

Figure 6.3-3 and Figure 6.3-4 depict the results of the strain energy of the solder joints due to the different void configurations (small and large voids, respectively). The strain energy accumulates in the SAC305 STIM layer as thermal cycle progresses. Damage is expected to initiate in the solder when the accumulated strain energy reaches a critical value. Figure 6.3-3 and Figure 6.3-4 show that the magnitude of strain energy increases as the void percentage increases. This behaviour can be explained in terms of physical parameters including load bearing area and stress concentration factor [175]. It should be noted that the less discrepancies among the strain energy values obtained for the 5% - 20% large voids volume could be as a result of the similarities in the locations of those voids. Detailed study on the location of voids will be covered in the next section.

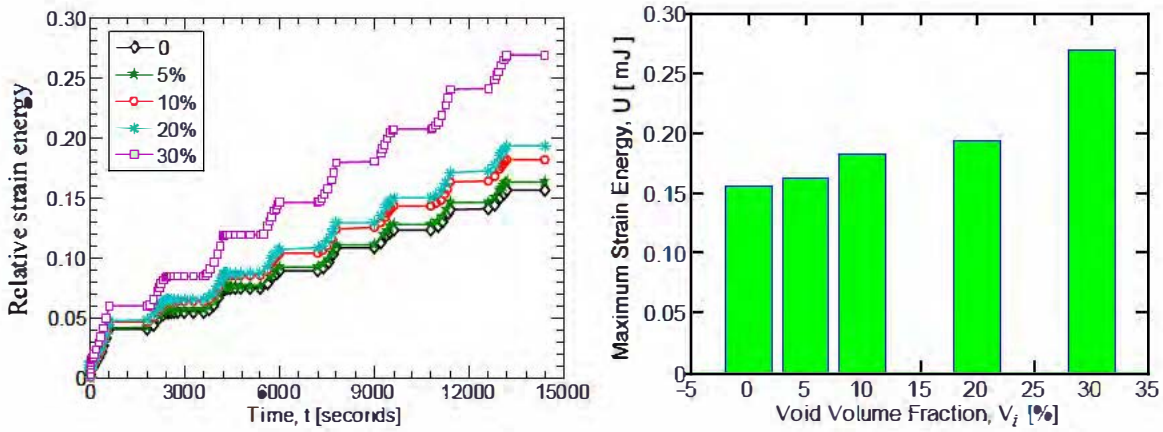



Figure 6.3-3: Effect of void volume fraction for small voids: (a) time histories of strain energy (b) maximum strain energy histogram

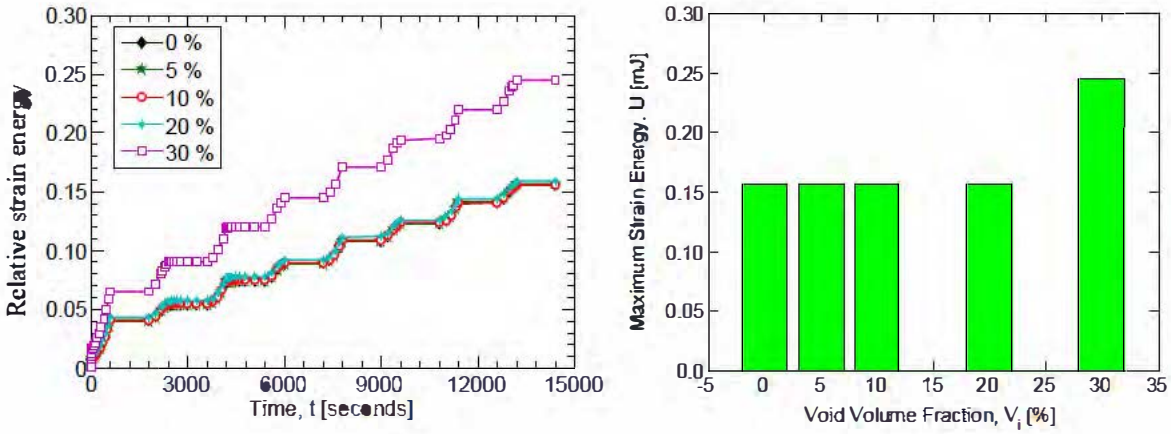



Figure 6.3-4: Effect of void volume fraction for large voids: (a) time histories of strain energy (b) maximum strain energy histogram

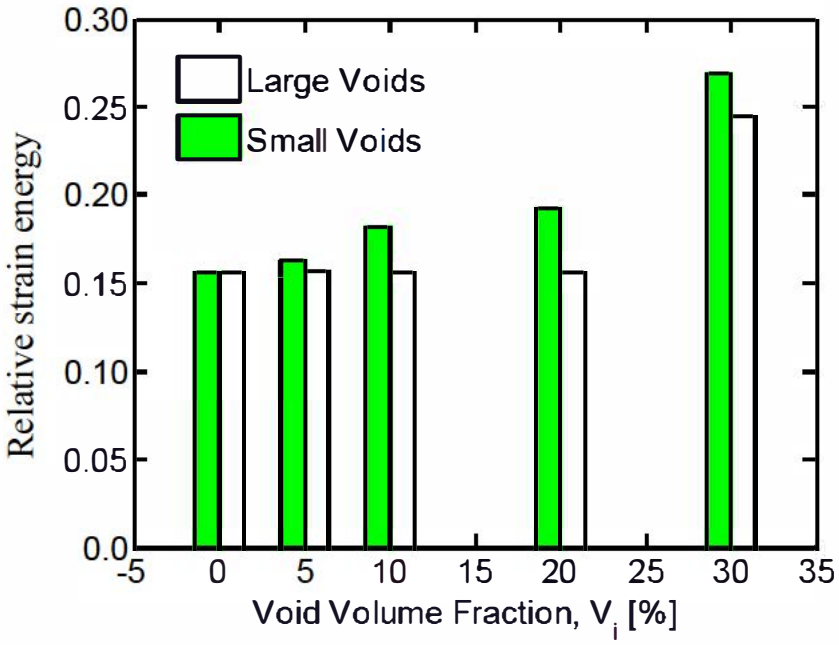



Figure 6.3-5: Comparison histogram of maximum strain energy for small and large voids

The primary factor that obviously changes as the percentage of void increases is the load bearing area of the solder joint. An increase in solder void percentage decrease the load bearing area of the solder joint (to support the thermal expansion mismatch) and lead to an increase in stress/strain in the solder joint, which could in turn accelerate damage initiation. This considers the fact that the original area of the solder joint remains constant while the void area/volume increases.

In Figure 6.3-6, the thermal cycle profile is superimposed on the plots with ordinate axis as the secondary axis to aid explanation for 5% void volume fraction configuration. As seen in Figure 6.3-6, the cyclic stresses in the solder joints due to the different void configurations (small and large) were similar though with variations in magnitude. The thermally induced stresses follow acyclic pattern where the maximum stress is experienced at the beginning of the low temperature dwell and the minimum stress at the end of the high temperature dwell because of the viscous behaviour of the solder joints. Minimum stress occurs during the high temperature phase of the thermal cycling load, while maximum stress is associated with the low temperature phase. Stress relaxation takes place both at the high and low temperature dwell phase due to creep effect. The comparison of the time histories of Von-Mises stress in the solder joints due to the different void configurations are shown in Figure 6.3-7. Evidence from Figure 6.3-7 suggests that the stress in the solder joints with small voids appears to be slightly more than that in the joints with large voids for equivalent voids percentage. This

could be as a result of stress concentration factor. The stress concentration around a circular cavity inside an infinite body increases around the cavity as the cavity becomes smaller [251]. In other words, stress concentration is an inverse function of cavity or void radius (in this case). This is why visual inspection of the contour plots (Figure 6.3-8 and Figure 6.3-9) of distribution of stresses around the different configurations of voided solder joints suggest an increase in the stresses acting around the small voids that are close to the critical region (solder/silicon interface) and stresses on the other side (180 degrees away – solder/copper interface) from the damage site. Accordingly, this increase in stress concentration around the small voids results in an enhancement in strain localisation around the joints with clustering small voids compared to those with large void configurations [177]. The enhancement in strain localisation leads to an increase in the strain energy of the solder joints with small voids relative to the joints with large void, for equivalent void percentage, as shown in Figure 6.3-5. The increase in strain energy of the joints with clustering small voids could facilitate damage initiation in the bearing solder joints when the accumulated strain energy reaches a critical value.

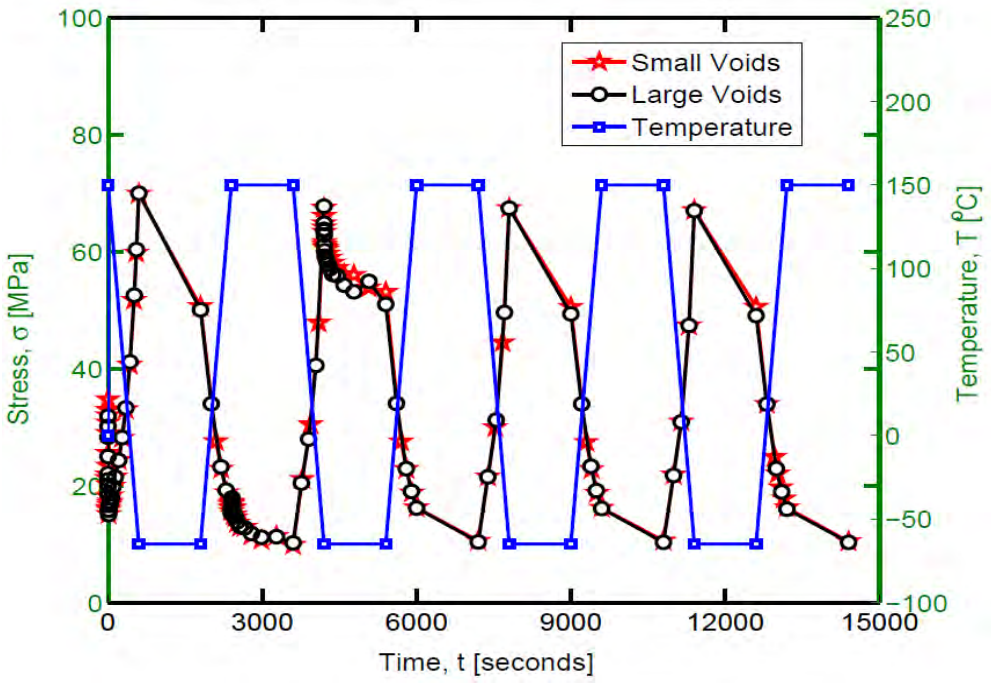



Figure 6.3-6**:** Thermal cycle profile superimposed on plot of von-Mises stress versus time for a 5% void volume fraction (of small and large configurations).

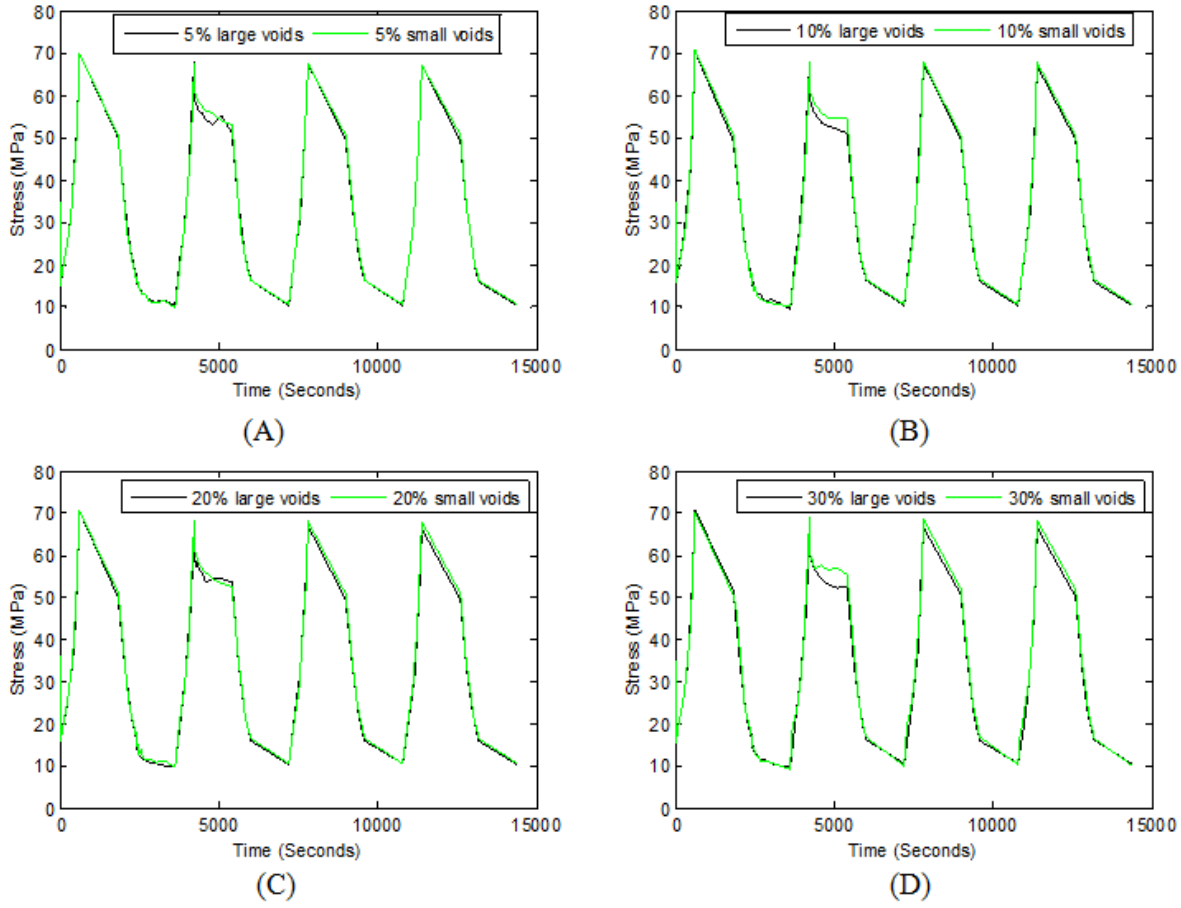



Figure 6.3-7: Stress plot for small and large voids configurations for (a) $V_i$ = 5% (b) $V_i$= 10% volume fraction (C)$V_i$= 20% volume fraction (D) $V_i$= 30% volume fraction

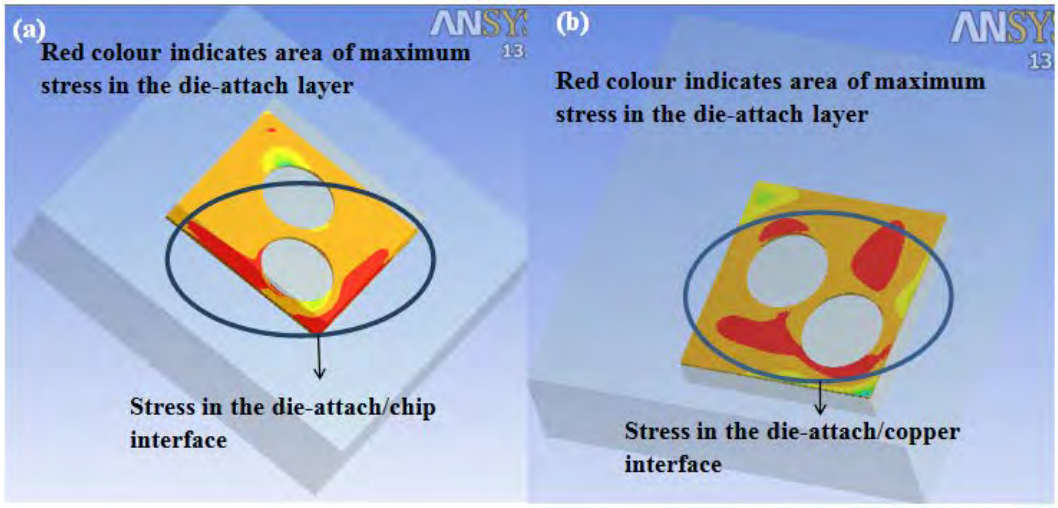



Figure 6.3-8: Stress distribution in the die attach layer for 30% large voids(a) die-attach/chip interface (b) die-attach/copper interface

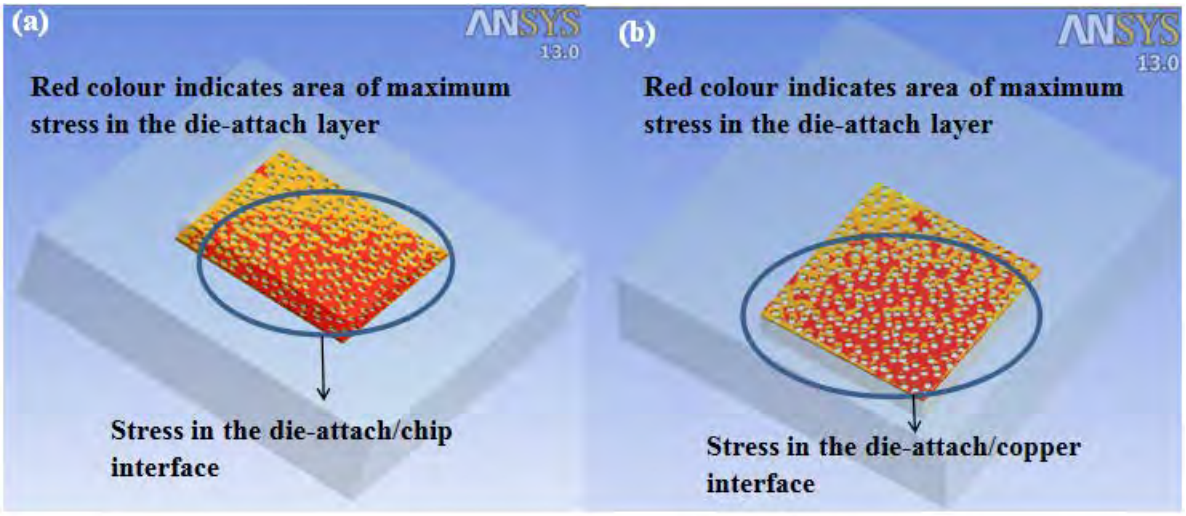



Figure 6.3-9: Stress distribution in the die attach layer for 30% small voids(a) die-attach/chip interface (b) die-attach/copper interface

#### *6.3.1.1 Accumulated plastic work*

A comparison between the obtained damage parameter (accumulated plastic work) for the small randomly distributed voids and large voids are shown in Figure 6.3-10. Evidence from the figure suggests that obtained damage parameter appears to be more for solder joint with large voids compared to the joints with small randomly distributed voids, for equivalent void percentage. However there is need for further study to assess conclusively which of either the large or small void configurations lead to higher accumulated plastic work. Visual inspection of the contour plots of the damage distribution in the solder joints with different void configurations reveals that the studied large void cases does not have much effect on the distribution/location of the maximum damage site compared to the small randomly distributed voids as shown in Figure 6.3-11 for 20% void volume percentage. In cases where one or a few of the small randomly distributed small void(s) is/are around the critical region, the region of maximum damage appears to drift away from the corner as the small random voids around the site increases. In other words, the contour plots show a decrease in the damage propagation rate in critical area around the small voids. This suggests that small voids arrest the damage propagation. This damage arrest mechanism could be as a result of blunting of the tip size of the damage region by the void [157, 174].

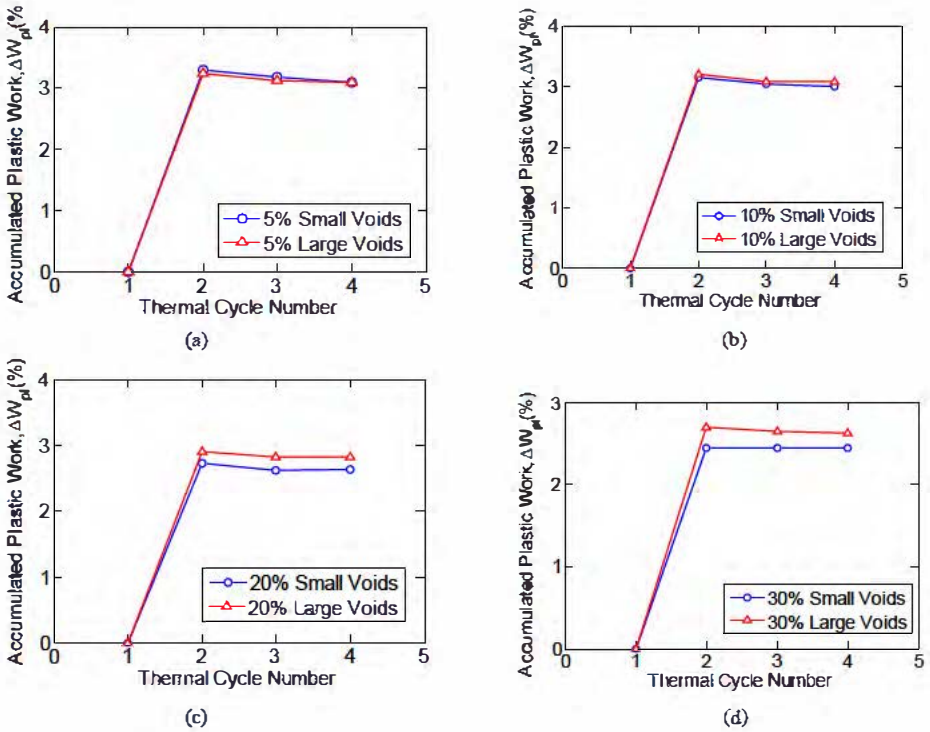



Figure 6.3-10: Accumulated damage plot for small and large voids configurationsfor (a) $V_i$ = 5% (b) $V_i$= 10% volume fraction (C)$V_i$= 20% volume fraction (D) $V_i$= 30% volume fraction

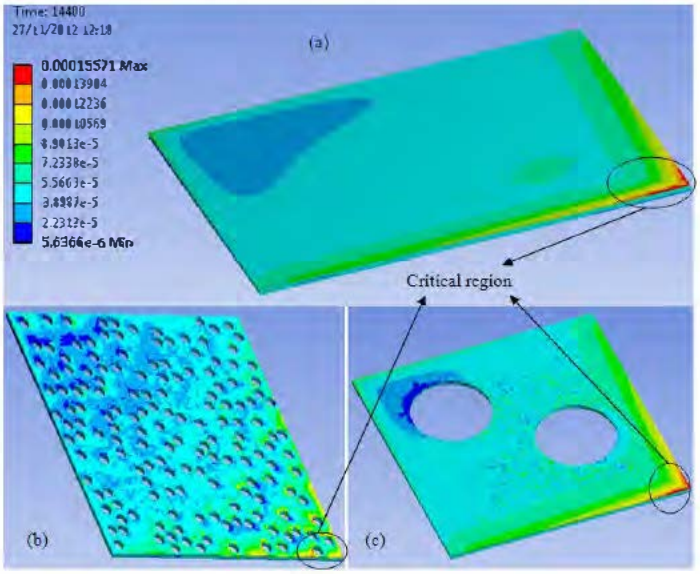



Figure 6.3-11: Contour plots of damage distribution in (a) solder joint with no void (b) 20% small random voids configuration showing less damage concentration in the critical region (c) 20% large voids configuration showing damage concentration that is similar to the joint without void

Figure 6.3-12 shows the interaction between void percentage and void configuration, the difference between obtained damage parameter for the two void configurations increases as voids percentage increases. The percentage difference increases from 4% - 25% as the void percentage increases from 5% to 30%. Therefore, as voids increases, the effect of configuration dominates over the effect of percentage. In other words, the sensitivity of solder joint fatigue life to the configuration of the voids increases as the void percentage increases.

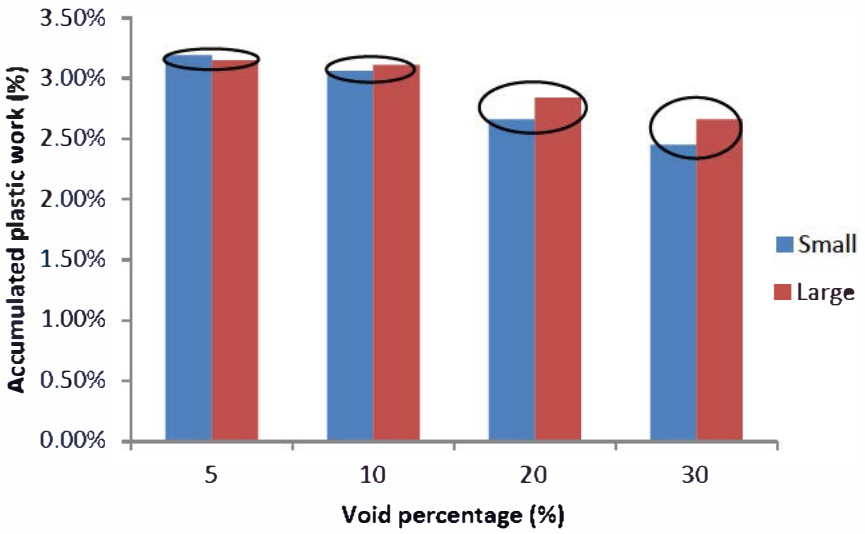



Figure 6.3-12: Interaction effect between void configuration and area

As observed in Figure 6.3-12, the decrease in accumulated plastic work as the void volume fraction increases is because the solder joint volume decreases as void percentage increases. In other words, voids were introduced by taking portion of material out of the solder joint volume. Since the work reported in this study is a comparative study, the accumulated plastic work values were evaluated using the critical values of the average damage parameters extracted from the entire solder joint volume remaining after the introduction of void percentages. Previous studies on small area solder joints (flip-chip solder bumps or BGA solder joints) have conventionally extracted these damaged parameters from a certain volume taken around a critical region in the height direction of the solder bump or solder ball. However, it has been reported in previous chapter [252] that this method of employing damaged parameters averaged over certain thickness of element layers is questionable when the geometry/shape of the solder joint is different from flip-chip solder bumps or BGA solder joints. It is unclear the pattern of the chosen volume of elements in large area solder joints

(such as the ones studied in this work). This is because the location of the maximum damage in large area solder joint is often at the corner region which has a different shape and orientation compared to the critical region in small area solder joint.

### 6.3.2 Study on void location

There is no generally accepted standard on distribution (vertical/spatial location) of die-attach voids for commercial/consumer industries, to the authors' knowledge. In the absence of specific test standard, the industry often subjects test vehicles to military standard qualification tests without much consideration for the application of the product [253]. MIL-STD-883D, method 2030 [28], for the ultrasonic inspection of die attach requires that a corner void should not be bigger than 10% of the total void area. Hence, 10% large coalesced void area was chosen for this study as a level of interest.

Voids can be formed at the corner/edge or centre of the STIM layer. In order to examine the precise effect of void location on the reliability of solder joint and potential crack arresting, 10% void area was selected to be modelled at different locations on the solder joint. 10% void was arbitrary located at different locations (void location A,B,C and E) of the solder die-attach layer as depicted in Figure 6.3-13a-c,e representing corner voids. Additionally, 10% void area was positioned in the centre (void location D) of the die-attach (Figure 6.3-13d) representing centre void (void location A). A depiction of solder layer without void is presented in Figure 6.3-13f to serve as a reference. The solder voids are of diameter 0.45mm and 0.04mm deep in a solder layer of 0.04mm thickness. Other dimensions remained as previously listed in Table 6.2-1.

As expected, Figure 6.3-14 shows that among the corner voids, the void located on the critical region (location B) resulted in the highest strain energy. This void decreases the cross-sectional area and load bearing area around the critical site. Subsequently, strain energy increases around the void which could accelerate damage initiation. The centre void resulted in the lowest strain energy that is akin to the strain energy of the solder joint without any void. This could be because of the near-neutral location of the centre void considering that load increases with DNP.

An interesting point for this study is that the obtained damage parameter (accumulated plastic work) is lowest for void located on the critical site as shown in Figure 6.3-15. Following our investigation, this could be attributed to damage arrest mechanism; in the contour plots of damage distribution (Figure 6.3-16a – f), this was depicted as a drop in the damage

propagation rate (after damage initiation) in the vicinity of the void close to the critical region. The damage propagation rate appears to decrease around the void. The centre void and voids located further from the critical region do not seem to assist in damage arresting, the solder joints with such voids resulted in almost the same damage distribution and critical region as the solder joint without any void (Figure 6.3-16f).

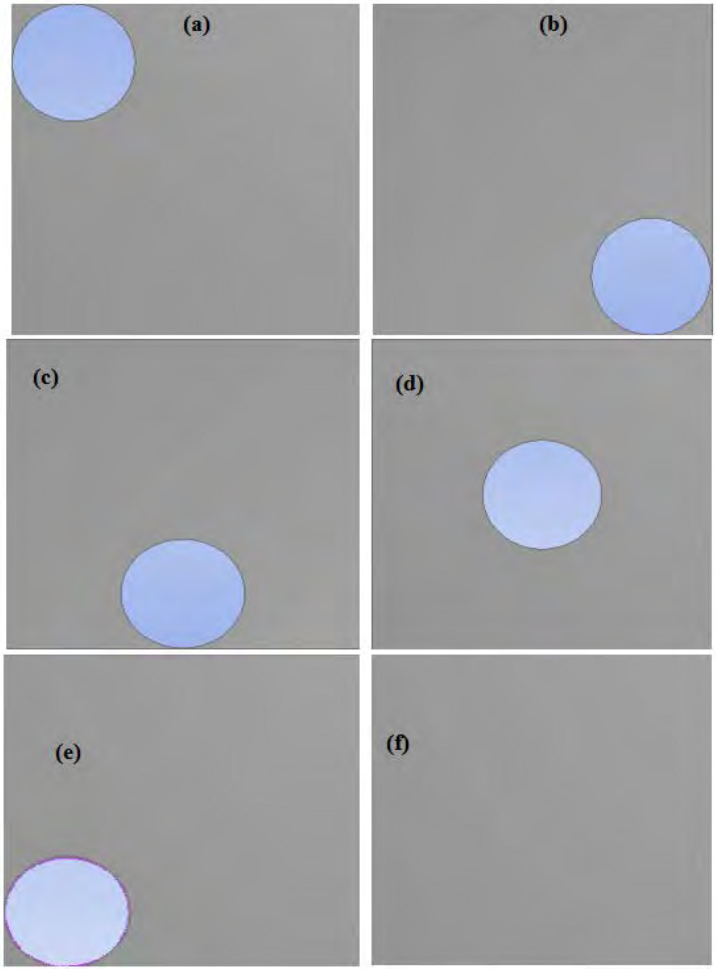



Figure 6.3-13: (a) Void location A (b) void location B (c) void location C (d) void location D (e) void location E (f) when there is no void. (Not drawn to scale).

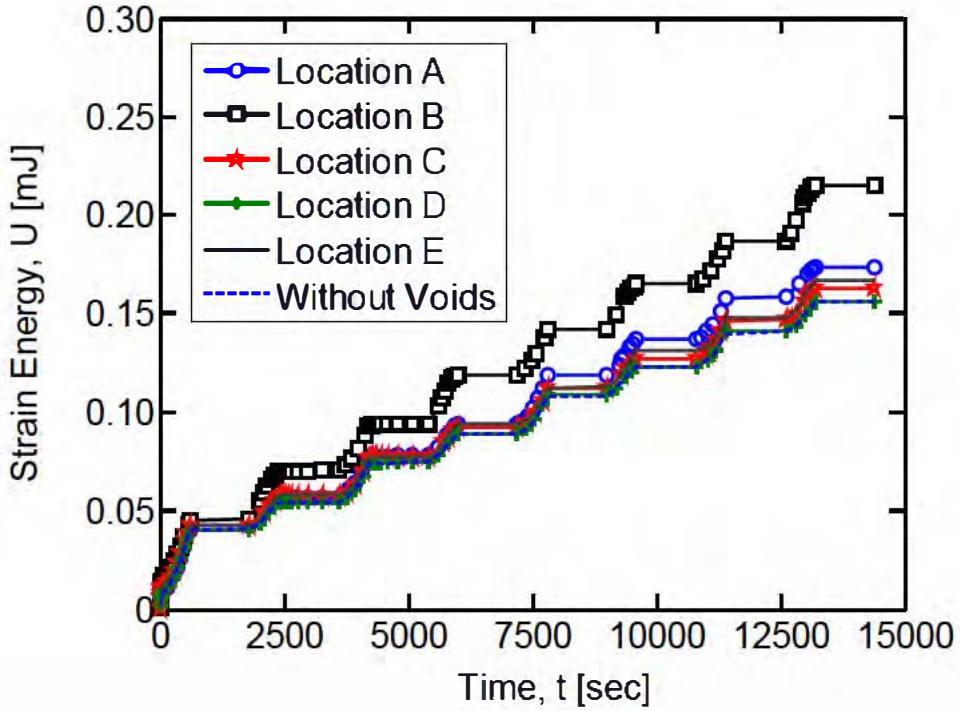



Figure 6.3-14: Strain energy in the solder joint due to the void location

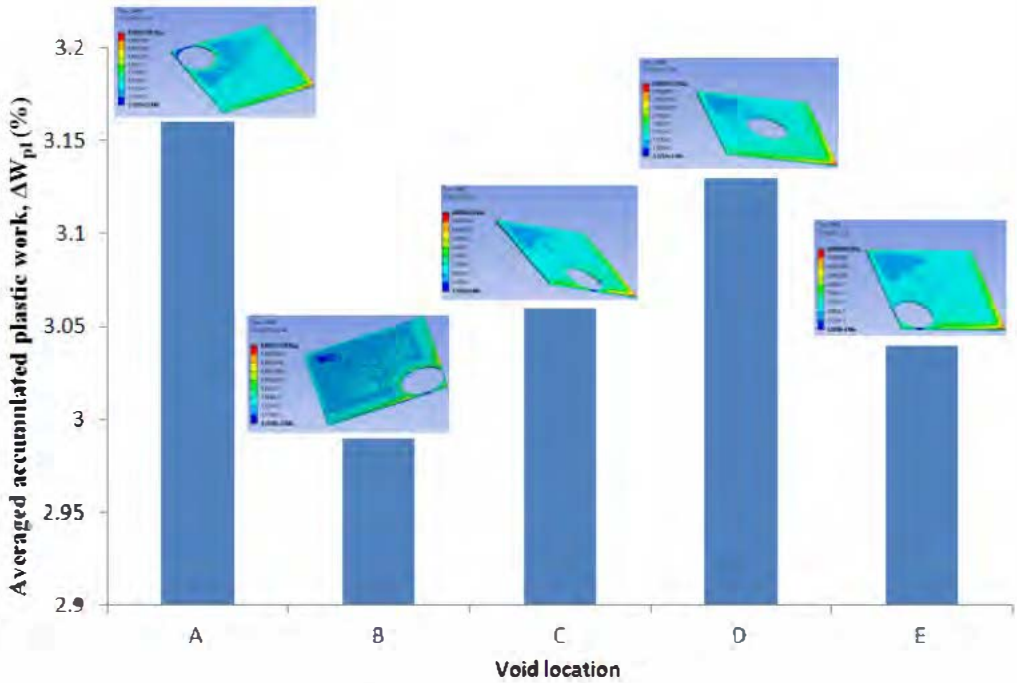



Figure 6.3-15: Effect of void location on accumulated plastic work

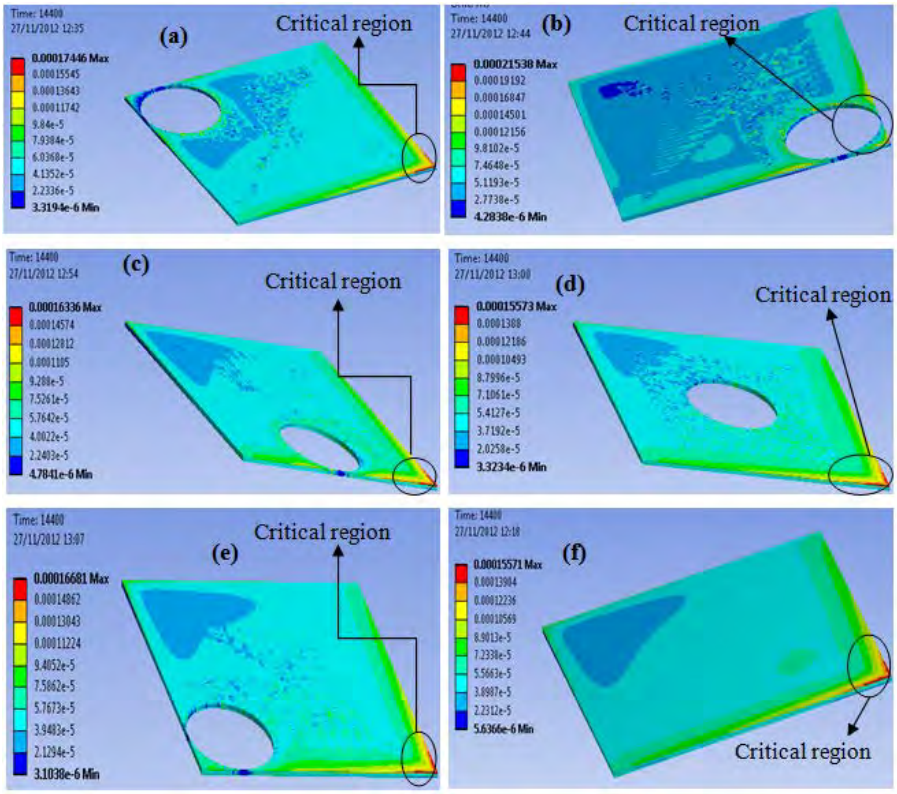



Figure 6.3-16: Damage distribution on the die-attach layer(a) as a result of void location A (b) as a result of void location B (c) as a result of void location C (d) as a result of void location D (e) as a result of void location E (f) when there is no void (Not drawn to scale).

### 6.3.3 Study on void depth

A through-thickness distribution of voids is a feature of real voided solder materials. To investigate the effect of through-thickness voids, an ideal model setup will involve 3D RVEs with randomly distributed voids (spherical voids) through the thickness. As the current implementation of the void-generating algorithm does not incorporate such volumetric void-generation feature, this study developed simplified through-thickness void arrangements as tool for assessing the effect of void depth.

Shallow voids can be formed at different vertical positions in the solder layer. This is because voids can be encapsulated in the middle of solder layer due to entrapment of gas bubbles formed by flux and other reactants during reflow soldering process. Furthermore, there is a potential for voids to occur at the surface between the solder layer and metallised silicon die or heat spreader as a result of poor solder wetting due to defective backside metallisation or backside contamination during manufacturing. Hence, representative shallow voids are situated at different vertical positions in the solder layer as shown in Figure 6.3-17a-c. Through void (Figure 6.3-17d) can occur as a result of degradation of shallow

voids during device service and also due to completely non-wetting of solder during manufacturing.

Four cases of voids depth were simulated; the cases are referred to as top void (case 1), middle void (case 2), bottom void (case 3) and through void (case 4). As in Section 6.3.2, 10% void is used in the study of these different void cases. Considering that FEA predicted the critical region (maximum damage site) in a die-attach to be a small region at the edge of the solder joint (Figure 6.3-1); the void cases are situated at the critical region (edge of the solder joint). Top void is 0.02mm deep located at the edge (critical region) of the solder joint in the upper part of the solder layer (0.04mm thick) next to the silicon die as illustrated in Figure 6.3-17a. Middle void is 0.02mm deep located at the edge (critical region) of the solder joint and situated in the middle of 0.04mm thick solder layer as shown in Figure 6.3-17b, leaving 0.01mm thick of solder layer on top and below the void. Bottom void is 0.02mm deep located at the edge of the solder joint in the lower part of the solder layer (0.04mm thick) next to the copper heat spreader as delineated in Figure 6.3-17c. Through void is 0.04mm deep in a solder layer of 0.04mm thickness, creating a through solder void and located at the edge of the solder joint as shown in Figure 6.3-17d.

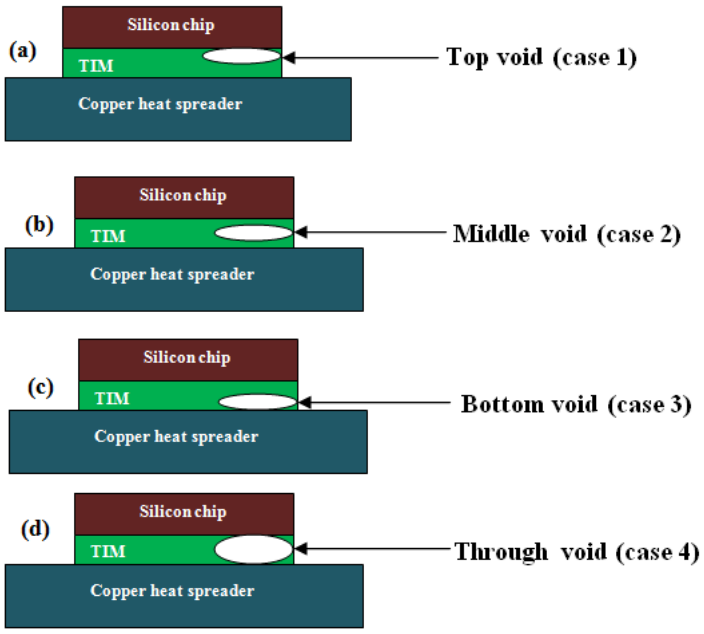



Figure 6.3-17: Schematic showing (a-c) shallow void cases and (d) through void(Not drawn to scale)

As shown in Figure 6.3-18, for the four void cases, as expected, “through void (case 4)” resulted in the most accumulated damage. “Through void” occupies the most region in the

solder joint compared to the shallow voids and could significantly weaken the stiffness of the solder joint around the void. A comparison among the shallow void cases shows that "void case 1" located at the interface of the solder joint and silicon chip (where the maximum damage is) resulted in the most obtained damage parameter. This void appears to greatly increase the extent and severity of strain localisation at the interface. The void embedded in the solder layer (case 2) does not have much impact on the reliability of the joint compared to void located at the solder/copper heat spreader interface (case 3). The decrease in the accumulated plastic work as compared to the solder joint with "through void" (case 4) is 3.3% when the void is at the solder/chip interface (case 1), 8.4% when at the solder/copper interface (case 3) and 9.7% when the void is embedded in the middle of the solder layer. In other words, with regards to shallow void cases, the voids at the interface are more detrimental to the reliability of the solder joint. This is in agreement with the IPC (IPC-A-610, IPC-7095) standard [170-171] that regards voids at the interface as higher risk voids relative to the voids embedded in the solder joint.

Stress concentration increases at the interfaces when the void interfaces with the silicon die or copper heat spreader which could facilitate damage initiation. This is coupled with the fact that voids potentially reduce the damage propagation path by taking out a large region from potential damage path. The combination of these two factors (increase in stress and decrease in damage propagation path) results in decrease in reliability of solder joint due to voids at interfaces compared to void embedded in the solder joint.

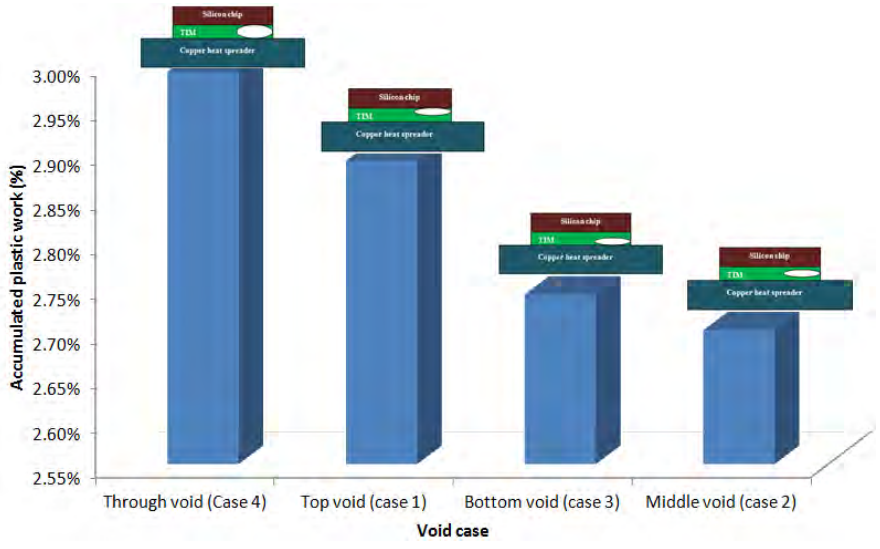



Figure 6.3-18: Accumulated damage due to the different void depth cases

## 6.4 Summary

In this chapter, the STIM layer with numerically generated random voids was incorporated into other package layers including the chip and heat spreader to complete the geometric model. The FEM result of the geometric model incorporating the SAC305 STIM layer has been validated against other experimental result (based on Indium STIM layer). The good qualitative agreement between the observations in the two results provided a level of confidence on the adopted modelling technique. Further parametric studies were carried out employing FEM to investigate the impacts of the different numerically generated random void configurations, sizes, volume fraction and locations on the thermo-mechanical performance of SAC305 STIM layer. Results suggest that:

- The sensitivity of solder joint fatigue life to the configuration of voids increases as the void percentage increases.
- The effect of large voids on obtained damage parameters in the studied solder joints was more profound compared to small randomly distributed voids. It was observed that the small voids around the critical region of the solder joints appeared to enhance stress and strain localisation around the maximum damage site thus facilitating damage initiation. However, the small voids also showed potentials of arresting the damage propagation by blunting the crack tip and thus increase the overall fatigue life of the solder joint.
- Strain energy in the solder joint increases as void gets closer to the critical site which may enhance damage initiation. Void further away from the critical region did not alter/influence damage distribution in the solder joint.
- Voids located in the surface of the solder joint were more detrimental compared to void embedded in the middle of the solder layer. Precisely, void situated in the surface between the solder joint and silicon die (where the critical site is located) was more detrimental to the solder joint reliability compared to void located in the solder/copper interface. Through void (void extending through the entire solder thickness) resulted in the most damaging parameter compared to the shallow void cases.

These conclusions may translate to strict void inspection criteria for joints with large voids, through voids, joints with voids close to the critical site and void located at the surface between the solder joint and the chip or copper heat spreader. Further studies have been carried out to investigate the effect of the different solder void patterns on the thermal

performance of a chip scale packaged power device. These will be presented in the next chapter.

# Chapter 7: Parametric Study of voids: Numerical modeling – Part III

## 7.1 Introduction

Besides the thermo-mechanical effects of voids on solder joints as covered in the previous chapter (chapter 6), voids also reduce the effective solder cross-section area available for heat transfer [254]. This subsequently results in an increase in thermal resistance and chip peak temperature which can lead to temperature activated failure mechanisms.

The purpose of the present chapter is to apply FEA to a systematic investigation of the effects of different numerically controlled Pb-free solder void patterns on the thermal performance of chip-level packaged power device. As in chapter 6, SAC305 will be used for the investigation. The solder void patterns under investigation include distributed small voids and large single coalesced voids; shallow voids and deep voids; corner/edge voids and centre voids. Thermal characterisation of the impacts of these voids is crucial in assessing the role of different void patterns in package thermal performance and improving the overall reliability of semiconductor power devices.

This chapter firstly gives a theoretical background on the thermal implications of solder voids. Subsequently, finite element modelling is carried out on to evaluate the effects of different void percentages and configurations on the overall thermal performance of a chip-scale packaged power device. New voided STIM models are numerically generated for a study on the effect of different heat generating area of the chip on thermal resistance values. Further parametric studies are then carried out on the effect of different void depth and locations on the thermal behaviour of a chip-scale assembly.

### 7.1.1 Thermal implication of solder voids

The heat generated by the power dissipated above the void has to flow laterally around the void and hence obstruct thermal flow as shown in Figure 7.1-1. This impediment in heat flow could result in overheating or other temperature activated failure mechanisms. A practical example of voids induced failure case is shown in Figure 7.1-2; the occurrence of voids in the STIM have resulted in high thermal resistance and subsequent melting of gold (Au) bonding wires found in another piece of experimental work.

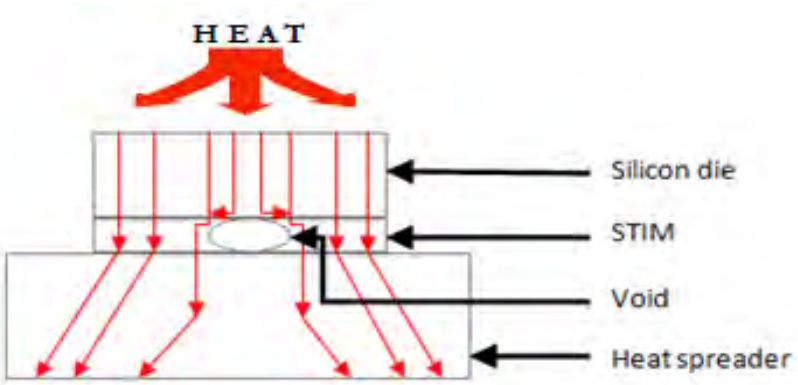



Figure 7.1-1: Schematic of heat flow with void present in the die attach

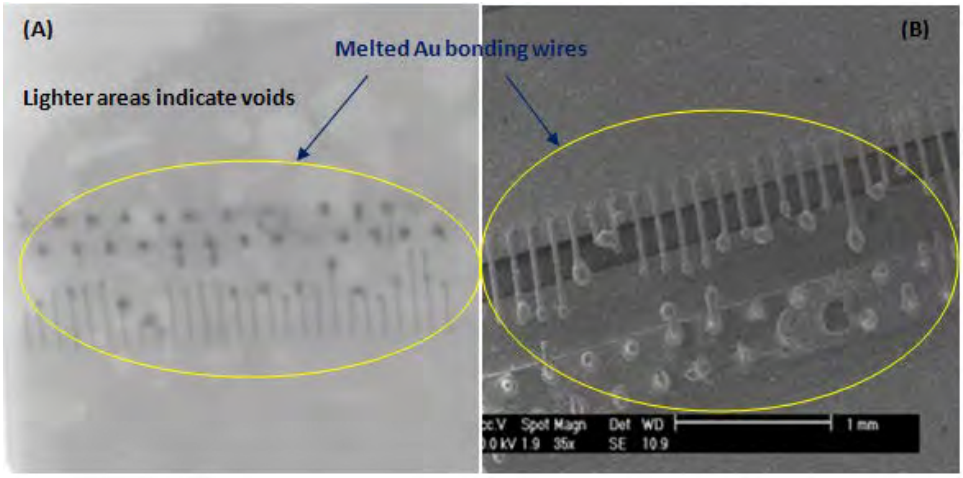



Figure 7.1-2: Images of melted Au bonding wires due to overheating caused by voids in the STIM layer(A) X-ray image (B) SEM image

The rate of conductive heat transfer through a solder joint based on Fourier's law is given as:

$$Q = -kA\frac{dT}{dx} = kA\frac{T_1 - T_2}{L} \qquad (7.1\text{-}1)$$

Where Q is the heat transferred; k is the thermal conductivity; A is the cross sectional area of the solder joint; dT/dx is the temperature gradient; L is the thickness of the solder; and $T_1$-$T_2$ is the temperature difference. It can be inferred from equation (7.1.1-1) that the heat transferred is directly proportional to the cross sectional area of the solder layer. Defining resistance as the ratio of a driving potential to the corresponding transfer rate, it follows from equation (7.1-1) that the heat spreading resistance for conduction in the solder joint can be expressed as:

$$\theta = \frac{T_1 - T_2}{Q} = \frac{L}{kA} \qquad (7.1\text{-}2)$$

As a result of voids detrimental impact on heat conduction, process conditions are usually controlled carefully during manufacturing stage in order to keep void percentage at an acceptable level. This acceptable level is defined by the impact of voids on critical thermal parameters of an electronic package. A convenient parameter used in characterising and comparing the thermal effects of different cases of solder voids investigated in this paper is referred to as θ-JC (thermal resistance), defined as the ratio of the device temperature increase over ambient to the average power dissipated in the device [255] (which is a measure of the ability of a package to dissipate heat via conduction from the surface of the die to the heat spreader surface) [28, 38]. This is expressed as:

$$\theta\text{-JC} = \frac{T_{max} - T_{min}}{P} \qquad (7.1\text{-}3)$$

Where $T_{max}$ is the maximum temperature at the chip junction; $T_{min}$ is the minimum temperature at the top surface of the heat spreader; P is the power dissipation of the silicon chip. θ-JC is an important thermal design parameter which can be used to determine the maximum allowable power or the chip peak temperature under a given power for infinite heat sink [256].

### 7.2 Finite element model

The local (simplified) model consists of a silicon die of the packaged semiconductor power device mounted upon a stack of supporting layers of STIM and copper heat spreader (IHS) as depicted in Figure 6.2-1. The properties and dimensions of the different components of the simplified model are listed in Table 7.2-1.

Table 7.2-1: Properties and dimensions of package assembly constituents

| **Parameter** | **Silicon die** | **Solder (Sn3.0Ag0.5Cu)** | **Copper heat spreader** | **Void** |
|---|---|---|---|---|
| Length (mm) | 2.5 | 2.5 | 5 | - |
| Width (mm) | 2.5 | 2.5 | 5 | - |
| Thickness (mm) | 0.3 | 0.04 | 1 | - |
| Radius (mm) | - | - | - | Varies as in Section 4.2.2. |
| Conductivity (W/mK) | 120 | *50 | 386 | 0.0261 |

** Ref. [15]*

### 7.2.1 Boundary conditions

Overall boundary conditions for the simplified model like the global model in Section 5.2 include a uniform heat flux Q ($W/mm^2$) at the top centre surface of the die. The heat (1W) generating area (active area) is applied as a heat flux on the top surface of the silicon chip. A fixed temperature ($25^oC$) is applied at the backside of the copper heat spreader, representing an infinite heat sink. The other surfaces are assumed to be adiabatic, i.e. no heat transfer by convection or radiation is considered. The heat is dissipated from the chip primarily by conduction through the supporting layers. Thus, only conduction mode of heat transfer is considered for all the void cases (models) investigated in this study.

## 7.3 Results and discussions

The voids are firstly modelled as vacuum with no material property and then with the material property of air (0.0261 W/mK thermal conductivity). There was no significant variation noticed in the results obtained from the two different approaches. Thus, in order to reduce computational time, all cases of void models considered in this study are modelled as vacuum unless otherwise stated. It is important to know that even though the values obtained through the approach employed in this study can be used to predict and compare thermal response of a package due to the effects of different solder die-attach void patterns; they may not represent real quantitative values of thermal resistances due to the limitations of the approach. Factors, such as defects of materials, thermal contact/interfacial resistances and non-linearity in the materials including solder voids are not considered in the modelling. These factors are traded off for an in-depth comprehension of the impacts of different numerically controlled solder die-attach void patterns on package thermal performance. In line with the method the simulations were carried out, this section will be presented in four main parts:

### 7.3.1 Effect of void configurations – Large vs. small

The voids are 0.04mm deep in a 0.04mm thick solder layer. The results as presented in Figure 7.3-1 show that for both void configurations, θ-JC rises as void percentage increases. Furthermore, as illustrated in Figure 7.3-2 and Figure 7.3-3, the chip junction temperature also rises as θ-JC increase. The increase in chip junction temperature due to 30% large coalesced void configuration is 1.68%, which is more than the 0.26% observed for equivalent percentage (30%) of small distributed voids.

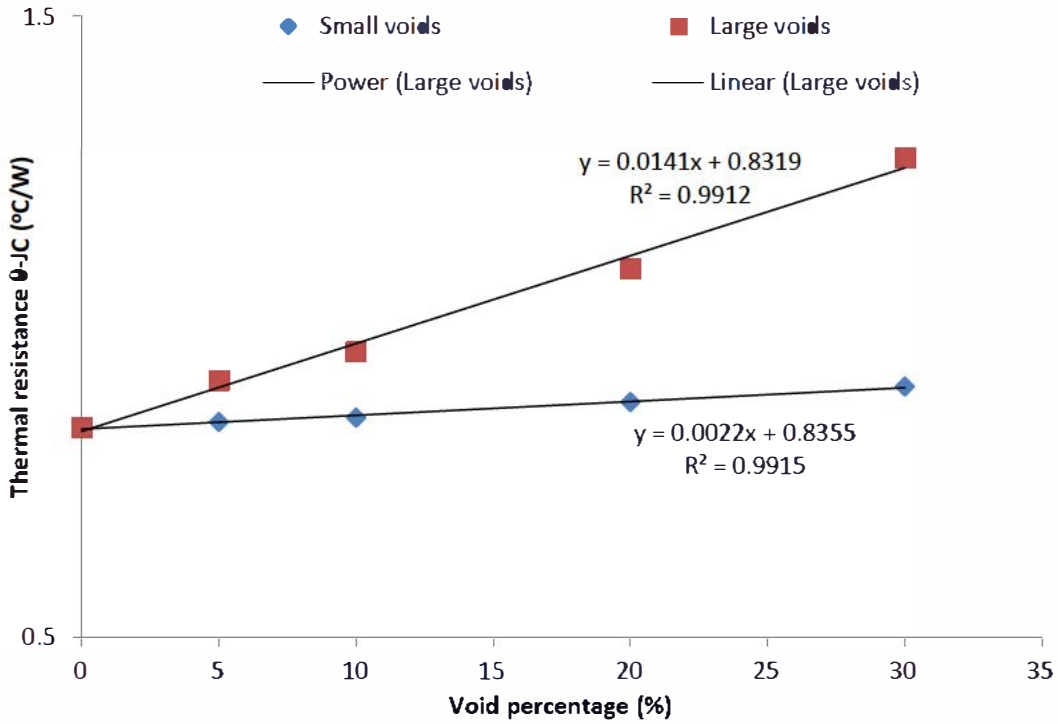



Figure 7.3-1: Variation of θ-JC with different void configurations

There is a distinct difference in the thermal impact of large and distributed voids as void percentage increases. The thermal resistance due to small voids configurations ($\theta$-$JC_S$) increases to a maximum of 0.90°C/W with 30% voids. As regards large void pattern, equivalent void percentage to that of distributed voids results in a much higher increase in thermal resistance ($\theta$-$JC_L$) of 1.27°C/W for 30% voiding.

The results suggest that:

- θ-JC increases as void percentage increases.
- Void configuration has a significant impact on the thermal performance of a package.
- Large single void can greatly increase the thermal resistance of a package compared to distributed voids of equivalent void percentage.

More attention should therefore be given to large coalesced voids when setting criteria for solder die-attach inspection. The difference in the thermal spreading resistance behaviour of large coalesced and small distributed void configurations can be qualitatively explained through the effects of heat flow. Three-dimensional heat spreading comprises of both vertical flow and lateral flow [257]. Therefore, there could be vertical heat flow resistance from the heat generating source above the void, and a lateral heat flow resistance from the region

above the void to the surrounding non-voided areas [62]. Void in solder die attach area results in a thermal spreading resistance as heat is forced to flow laterally around the void region. Additionally, heat flow in the vertical direction is restricted by the high thermal resistance through the void itself. For the same void percentage, lateral heat flow resistance is higher for large coalesced void configurations since heat flows laterally for a much shorter distance for the small distributed voids. Thus, large coalesced voids result in a much more increase in the overall thermal resistance.

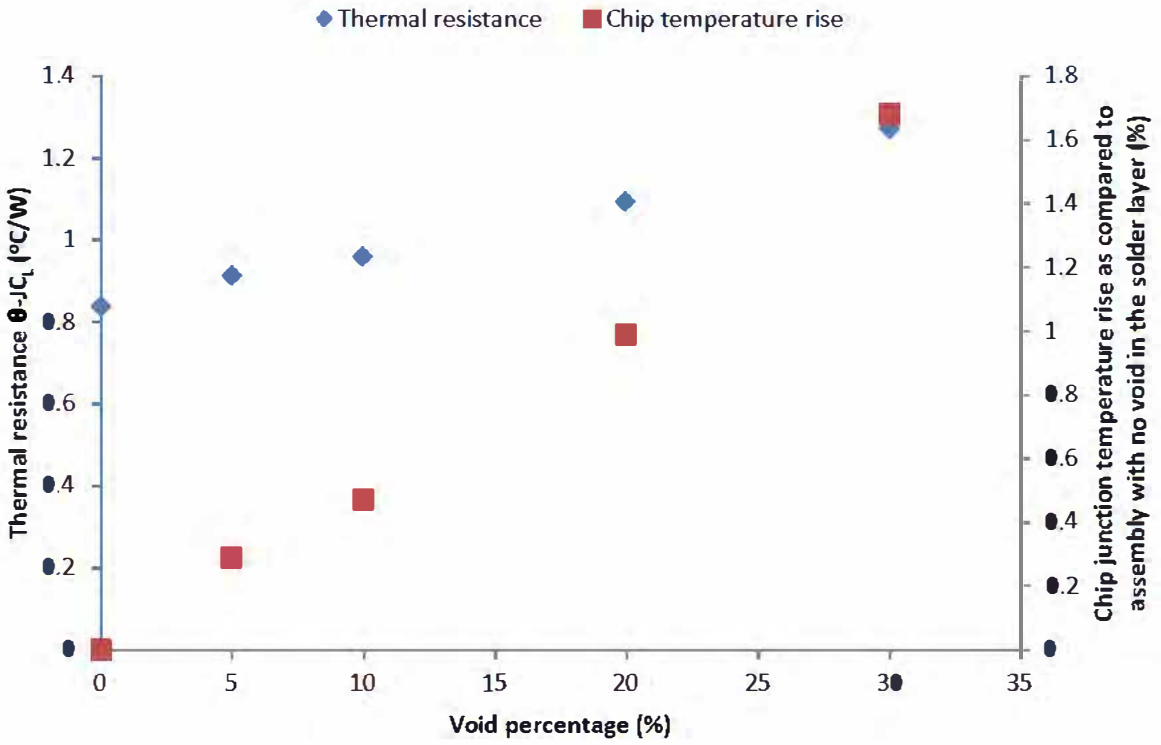



Figure 7.3-2: Thermal performance of assembly due to large voids

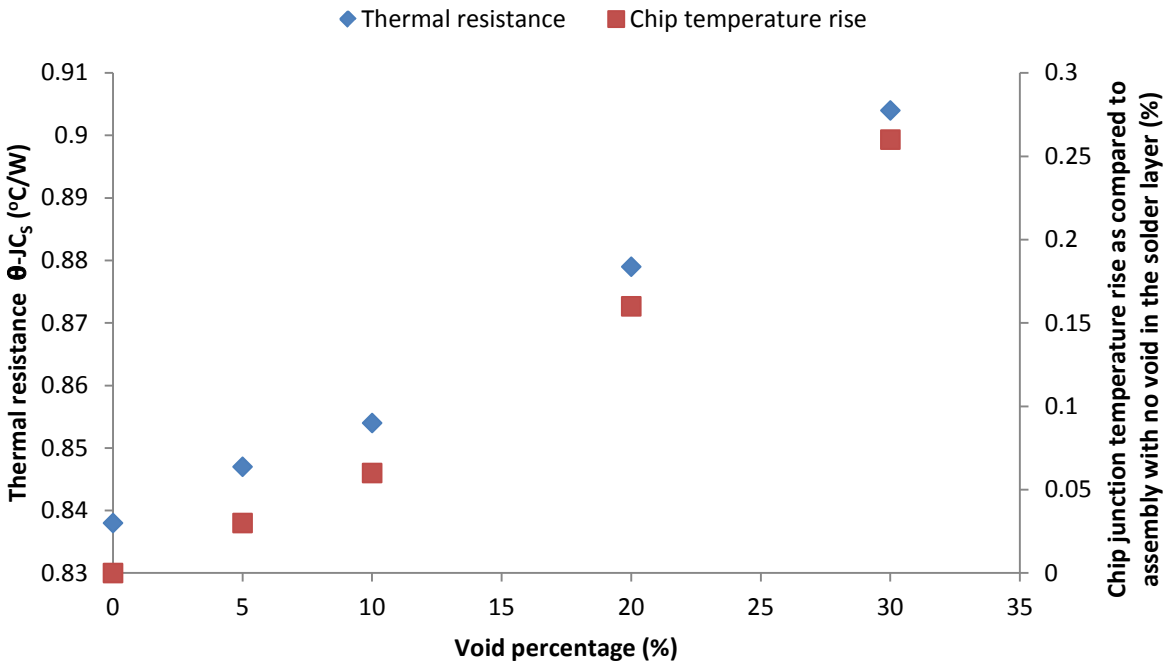



Figure 7.3-3: Thermal performance of assembly due to small voids

#### 7.3.1.1 Comparison with available experimental data

Experimental work on void configuration is scarcely available in literature; this could be as a result of the complexities and interactions associated with the many factors that affect void formation during manufacturing and operating stages [165]. Hence, practically controlling exact void configurations in a solder layer of about 0.04mm thickness would be too complicated. No wonder, finite element thermal analysis is often employed to isolate and characterise the precise effects of the different void configurations as even a mixture of these voids can form in one given solder joint in reality. To the authors' knowledge, the only previous experimental work which allows the exact control of void configuration is that of Fleischer et al. [62]. They studied the effect of large void and distributed void experimentally by precisely etching square void patterns directly onto the backside of the chip. They also carried out a numerical study to show that the thermal effect of voids located in the chip backside is equivalent to voids located in the die bond layer. Their results as depicted in Figure 7.3-4 showed that large contiguous void results in a much higher thermal resistance compared to small distributed voids of equivalent voiding percentage. This validates the finding of this study which suggests that small distributed voids account for less thermal resistance compared to large coalesced void of the same voiding percentage. Nonetheless, considering that in reality, solder voids do not follow a simple regular pattern square-like

shape but appear to progress roundly and chaotically, this study employ a randomly distributed circular void approach precisely embedded in the solder die-attach layer as shown in Figure 4.2-9 and Figure 4.2-10. This approach is different from the square void patterns precisely etched onto the backside of the chip in Reference [62]. The strong qualitative agreement in the results from the two different approaches suggests that void geometry may not have an effect on thermal resistance. The quantitative discrepancies between the simulation results reported in this study and the experimental results in Fleischer et al. work [62] are expected because the experimental parameters including the material properties of lead-based solder attach layer studied by Fleischer et al. [62] were different from the parameters used in the present numerical study.

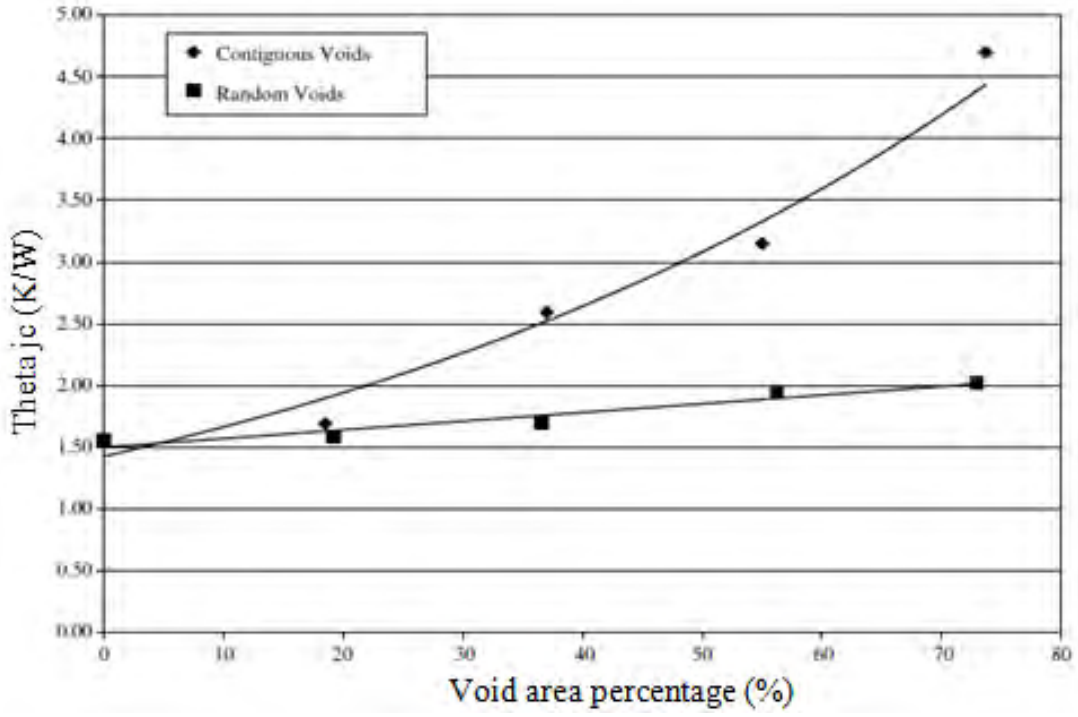



Figure 7.3-4: Variation of thermal resistance with contiguous and distributed void percentage (Fleischer et al. [62]).

### 7.3.2 Effect of heat generating source area on thermal resistance values

Considering that the active (heat source) area in a chip is often smaller than the total chip area as shown in Figure 7.3-5, the chip heat source area (active area) in the chip is varied from 10 – 100% to study its effect on thermal resistance values due to different void configurations.

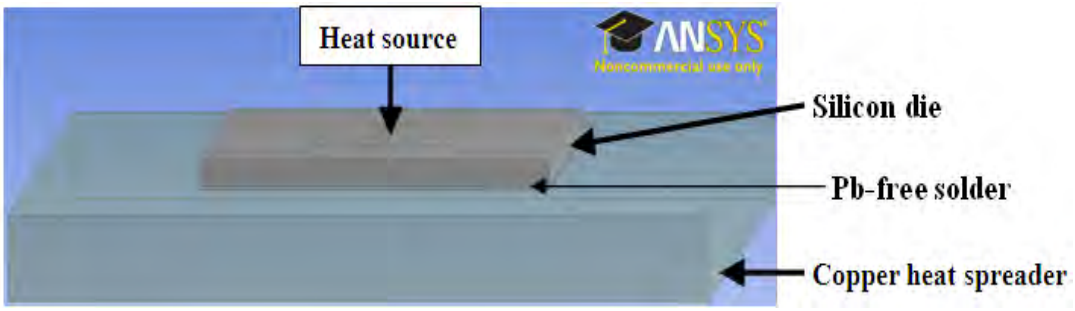



Figure 7.3-5: Model structure showing 40% chip heat source area

#### *7.3.2.1 Void model generation for study on heat source area of chip*

For this study on the effect of heat source area on thermal resistance values, considering the highly unsymmetrical (non-uniformity) nature of the random voids generated using the *MCRVGen* algorithm which would affect the result of variation in heat generation area; a new mathematical model was developed for the creation of evenly distributed small voids and large void. Large coalesced void takes the form of a single, large centrally located, circular void while small distributed voids are modelled as evenly spaced circular voids with equivalent total void area as the large coalesced void. The voiding area was calculated in such a way that one single coalesced circular void would be equivalent to 25 small evenly distributed circular voids as follows:

$$A_{large} = a_{small} \qquad (7.3\text{-}1)$$

$$\pi(R_{large})^2 = \pi(r_{small})^2 \qquad (7.3\text{-}2)$$

$$\left(\frac{(R_{large}}{5}\right)^2 = (r_{small})^2 \qquad (7.3\text{-}3)$$

$$\frac{(R_{large})^2}{25} = (r_{small})^2 \qquad (7.3\text{-}4)$$

$$A_{large} = 25a_{small} \qquad (7.3\text{-}5)$$

Where $A_{large}$is the area of large single coalesced void; $a_{small}$ is the area of small distributed voids; $R_{large}$ is the radius of large single coalesced void; $r_{small}$ is the radius of small distributed voids.

Figure 7.3-6 shows example of void configuration for 10% void area concentration and the complete void configurations are shown in Table 7.3-1.

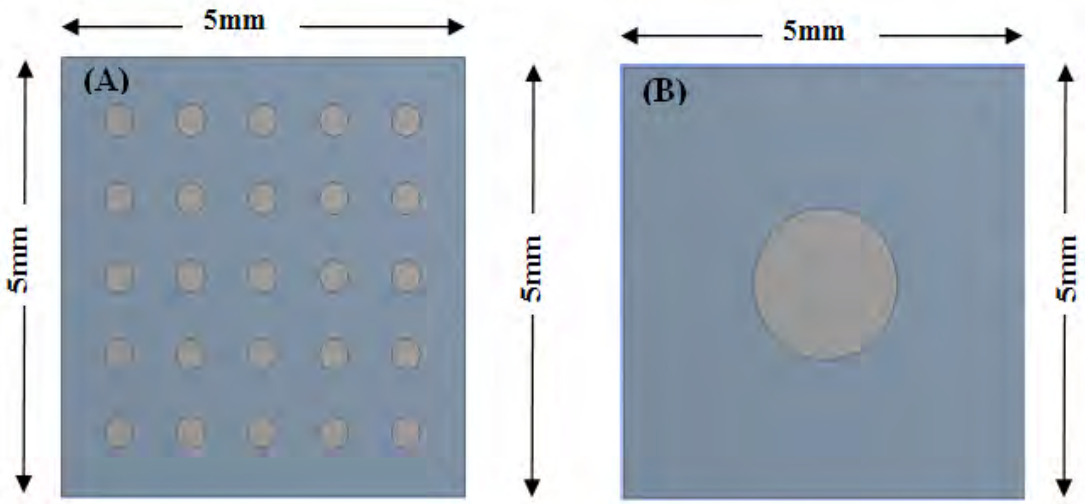



Figure 7.3-6: Examples of void configuration for 10% void area concentration with (A) showing evenly distributed small voids and (B) showing large single void

Considering that the MIL-STD-883D, method 2030 [172], for the ultrasonic inspection of die attach requires that the overall solder void area should not exceed 50% of the total joint area, the void area percentages (total area of voids/foot print of solder) 5, 10, 20, 30, 40, 50% are chosen as levels of interests, and a 75% void selected as a worst case reference for this study. Area percentage is defined as the ratio of the void area to the solder joint area when viewed from the top (as indicated by IPC-7095 [171] and also the same way X-ray machines measure the area percentage of voids). The voids are simulated as trapped air pockets. The void approach presented in this study differs from the void model proposed by Fleischer et al. [62] which consider voids as square patterns precisely etched onto the silicon chip backside. The method presented in this study allows the numerical and spatial control of different circular void patterns embedded in the solder layer. Thus, it enables the investigation of the thermal performance of chip-scale packaged power device due to the impact of different heat source generating area. Of course, in reality solder voids do not follow a simple exact orientation but progress chaotically.

Table 7.3-1: Large and distributed void configurations

| Model | Configuration type | Void *radius (mm) | Number of voids | Void **area ($mm^2$) | Percentage of void area (V%) |
|---|---|---|---|---|---|
|  | No void | 0 | 0 | 0 | 0 |
|  | Large | 0.631 | 1 | 1.25 | 5 |
|  | Distributed | 0.126 | 25 | 1.25 | 5 |
|  | Large | 0.892 | 1 | 2.49 | 10 |
|  | Distributed | 0.178 | 25 | 2.49 | 10 |
|  | Large | 1.261 | 1 | 4.99 | 20 |
|  | Distributed | 0.252 | 25 | 4.99 | 20 |
|  | Large | 1.544 | 1 | 7.49 | 30 |
|  | Distributed | 0.309 | 25 | 7.49 | 30 |
|  | Large | 1.784 | 1 | 10.00 | 40 |
|  | Distributed | 0.357 | 25 | 10.00 | 40 |
|  | Large | 1.995 | 1 | 12.50 | 50 |
|  | Distributed | 0.399 | 25 | 12.50 | 50 |
|  | Large | 2.442 | 1 | 18.74 | 75 |
|  | Distributed | 0.488 | 25 | 18.74 | 75 |

**Approximated to3 decimal places*

*** Approximated to 2 decimal places*

The properties and dimensions of the different components of the generated mathematical model are listed in Table 7.3-2. Nonetheless, owing to the symmetry of the models generated

with the theoretical calculated voids, only ½ geometric symmetry of the package (die and die-attach: 2.5mm x 2.5mm; copper: 5mmx5mm) is used in the analysis in order to reduce computational time and storage space.

Table 7.3-2: Properties and dimensions of package assembly constituents

| **Parameter** | **Silicon die** | **Solder (Sn3.0Ag0.5Cu)** | **Copper heat spreader** | **Void** |
|---|---|---|---|---|
| Length (mm) | 5 | 5 | 10 | - |
| Width (mm) | 5 | 5 | 10 | - |
| Thickness (mm) | 0.3 | 0.04 | 1 | - |
| Radius (mm) | - | - | - | Varies as in Table 7.3-1 |
| Conductivity (W/mK) | 120 | *50 | 386 | 0.0261 |

** Ref. [15]*

The overall boundary condition for the model is the same as in Section 7.2.1 for the models generated using the *MCRVGen* algorithm.

The FEA program (ANSYS) subdivides the assembly into finite elements (mesh) as shown in Figure 7.3-7. The mesh for assembly without solder void consists of 606,219 nodes and 120,564 elements, the results are checked for mesh independence by comparison to models with 355,971 nodes and 2,909,666 nodes.

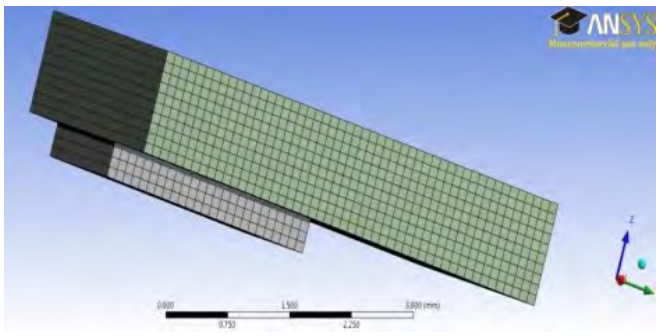


Figure 7.3-7: An example of a meshed model

***Small voids Vs large voids:***

For the new mathematically generated small voids and large coalesced void, the effect of small voids and large void of equivalent void area percentage on thermal performance is firstly evaluated. The voids are 0.04mm deep in a 0.04mm thick solder layer. The results as presented in Figure 7.3-8 show that there is a distinct difference in the thermal impact of large and small voids as void percentage increases. The thermal resistance due to small distributed void configurations ($\theta$-$JC_D$) increases to a maximum of 2.105°C/W with 75% voids. As regards large void pattern, equivalent void percentage to that of distributed voids results in a much higher increase in thermal resistance ($\theta$-$JC_L$) of 6.367°C/W for 75% voiding. The qualitative agreement between this study and the previous study on effect of different void configurations provides confidence on modelling technique. Hence, this void generation approach would be used for a comparative study of the effect of different area of chip heat source on thermal behaviour of chip-scale packaged power device.

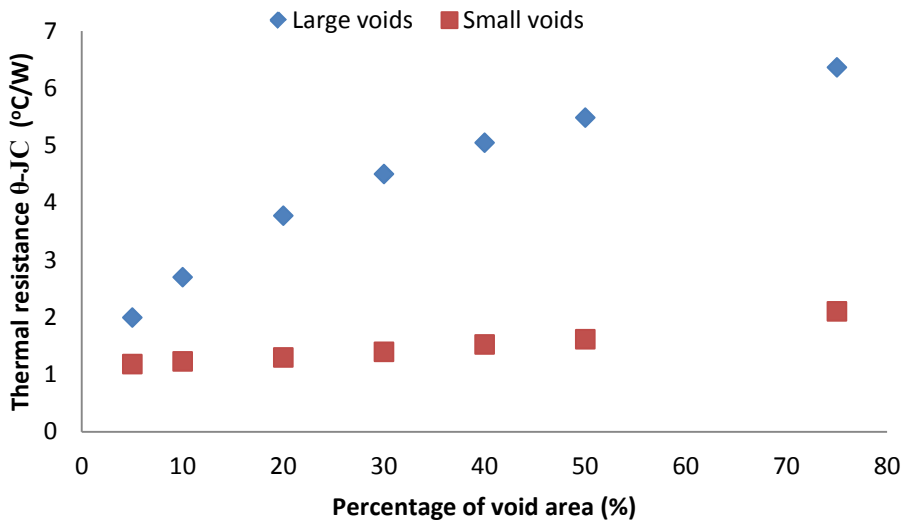



Figure 7.3-8: Variation of θ-JC with different void configurations

#### 7.3.2.1.1 Study on Heat Source Area

The influence of the heat (1W) generating area on thermal resistance is examined by varying the active area in the chip from 10 – 100% for the two different void configurations (10% large and small voids area). The results are shown in Figure 7.3-9. It is clear from the results that θ-JC decrease as the heat generating area increases. This is perhaps because larger heat source area has a more heat transfer area and thus smaller heat flux which can subsequently

improve thermal performance, for the same amount of chip power generation.At each heat generating area, θ-JC is higher for large coalesced void configuration than distributed voids. As the heat generating area increases from 10–100%, θ-JC variation for the distributed voids configuration is 338% which is higher than the 284% observed for large coalesced void configuration. Thus, this study suggests that θ-JC values may strongly depend on the heat (power) generating area of the chip. It is of immense consequence to thermal engineers creating accurate thermal models to understand that the effect of the chip power on thermal resistance depends on the area of the chip generating the power. Considering that the heat generating area of the chip is much smaller than the total chip area in reality, a fixed heat generating area of 2mm x 2mm (40%) at the top centre surface of the chip as shown in Figure 7.3-5 is employed as a level of interest for subsequent studies on effect of different void patterns on package thermal resistance.

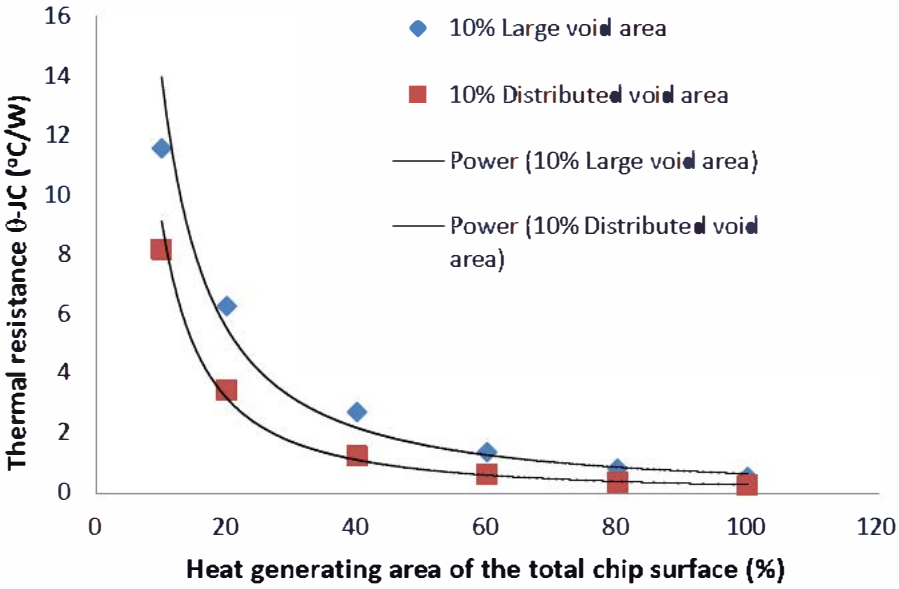



Figure 7.3-9: Effect of heat generating area on θ-JC

### 7.3.3 Effect of voids depth (shallow vs. deep voids)

Previous analysis in section x suggests that large coalesced voids have more adverse impact on the thermal resistance of package than distributed voids for equivalent voiding percentage. Hence, large coalesced void was chosen for this study.

From the solder wetting point of view, there could be shallow voids (partially wetted) and deep voids (completely non-wetted voids).Hence, representative shallow voids are situated at different vertical positions in the solder layer as shown in Figure 7.3-10a-c. Through void

(Figure 7.3-10d) can occur as a result of degradation of shallow voids during device service and also due to completely non-wetting of solder during manufacturing.

Four cases of voids depth were simulated; the cases are referred to as top voids (case 1), middle voids (case 2), bottom voids (case 3) and through voids (case 4). Top voids are 0.02mm deep located centrally in the upper part of the solder layer (0.04mm thick) next to the silicon die as illustrated in Figure 7.3-10a. Middle voids are 0.02mm deep located centrally in the middle of 0.04mm thick solder layer as shown in Figure 7.3-10b, leaving 0.01mm thick of solder layer on top and below the voids. Bottom voids are 0.02mm deep located centrally in the lower part of the solder layer (0.04mm thick) next to the copper heat spreader as delineated in Figure 7.3-10c. Through voids are 0.04mm deep in a solder layer of 0.04mm thickness, creating a through solder void as shown in Figure 7.3-10d. The solder void models used for this study are modelled by filling the void depths with material that has the thermal conductivity of air (0.0261W/mK). Other dimensions including the void area percentages are as earlier listed in Section 7.3.2.1 for large coalesced voids.

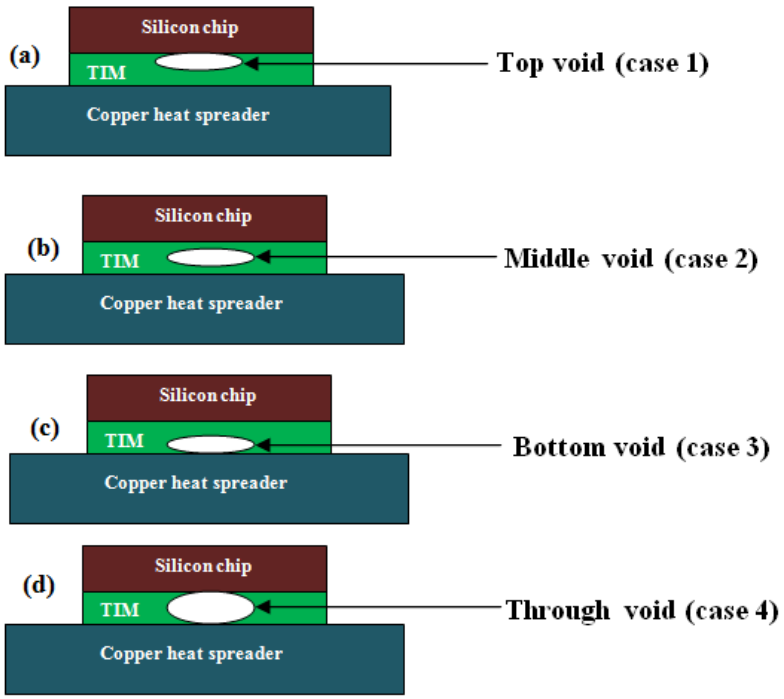



Figure 7.3-10: Schematic showing (a-c) shallow void cases and (d) through void(Not drawn to scale)

Figure 7.3-11 shows θ-JC rises as the void percentage increases for the different void cases. The thermal performance predictions for the different void cases are observed to be similar as the result data for each case is correlated with a power fit. Figure 7.3-12 depicts the

comparison of thermal resistance due to the different void cases. Among the shallow void cases, top voids (closest to the heat source) relatively lead to the highest increase in θ-JC. Furthermore, bottom voids (next to the heat spreader) which occur in solder layer surface further from the heat generating chip result in less values of θ-JC compared to the middle voids. The variations in θ-JC due to the different shallow void cases with the same thickness result from the vertical proximity of the voids to the heat generating source. With regards to the four void cases, as expected, thermal resistance is highest for through voids. A through void in the solder layer replaces a relatively much higher thermal conductivity solder region with an extremely low thermal conductivity void. Overall, there is no significant variation in θ-JC as a result of the four different void cases as θ-JC only varies betweeen 1–5 % as the voids percentages increase from 5-75%. Similar result trend as regards the void cases was reported by Chen et al. [256]. However, the work of Chen was limited to 10% void area. In this study, the influence of void depth/position on thermal resistance can be observed in detail from 5 - 75% void area, greatly extending the current state of knowledge. This detailed information particularly may be of assistance to thermal engineers especially with works [160, 187] reporting the occurrence of voids in excess of 50% of solder joint volume in some Pb-free solders.

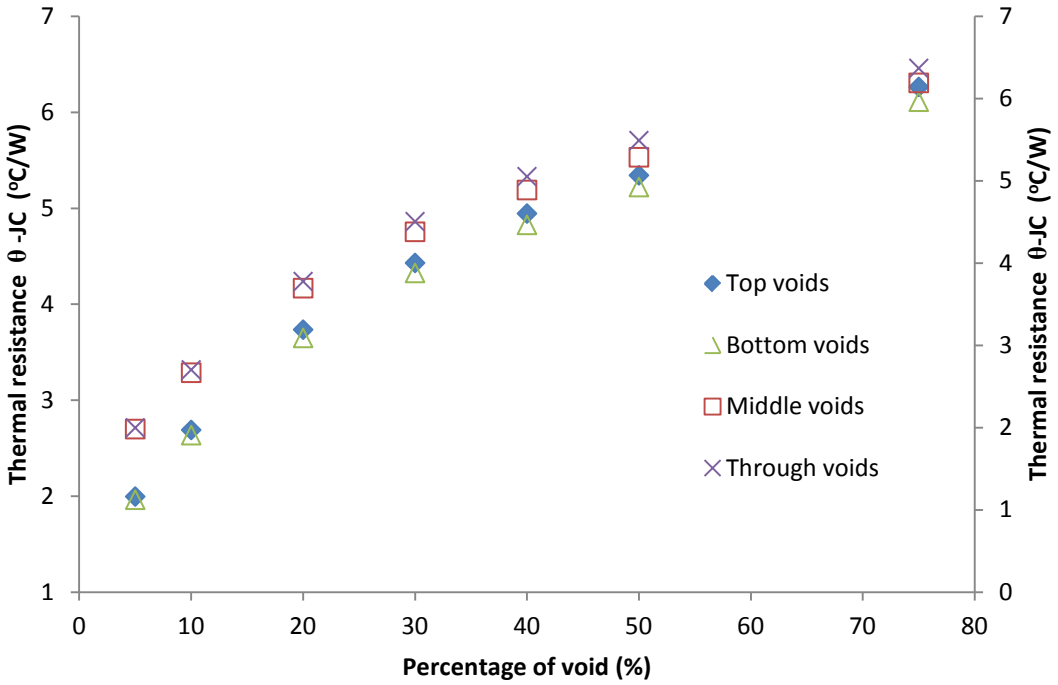



Figure 7.3-11: Thermal resistance performance for the different void cases

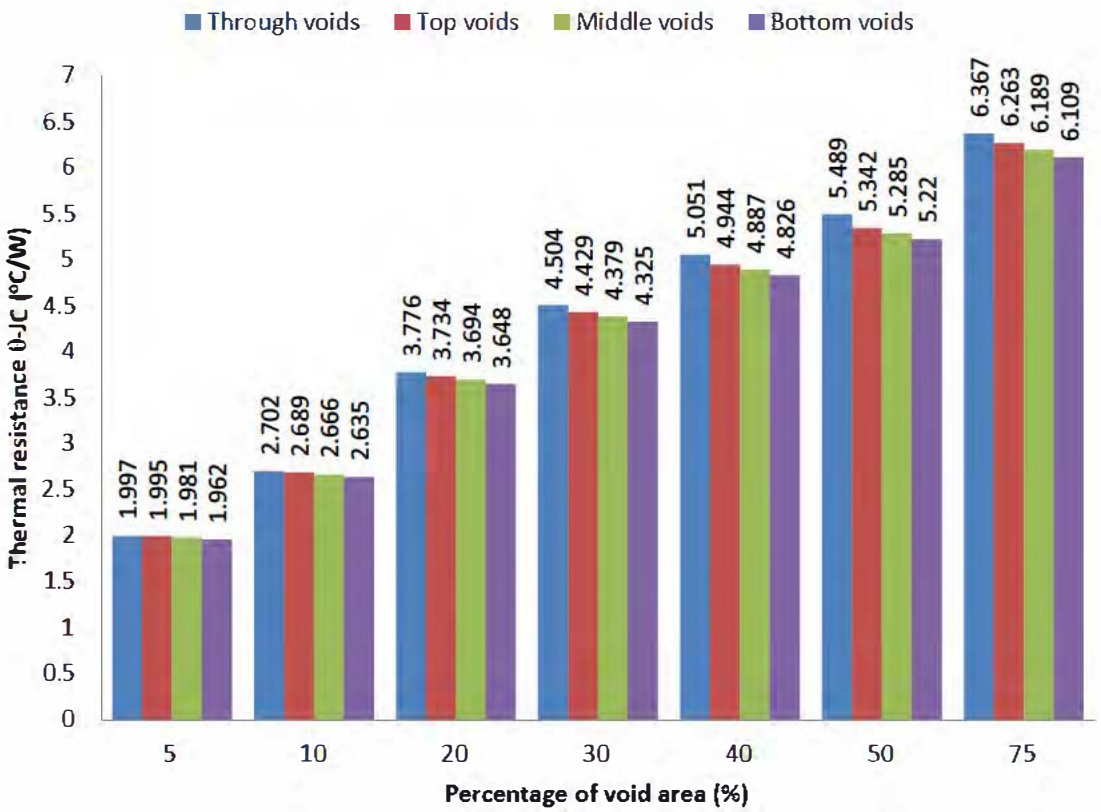



Figure 7.3-12: Variations of thermal resistance due to the different void cases

### 7.3.4 Effect of void location (corner voids vs. centre void)

10% large coalesced void area was chosen for this study as a level of interest. Furthermore, through voids were used for this investigation because they account for more profound effect on θ-JC compared to shallow voids as evident from the previous finding.

While the heat source is kept constant as shown in Figure 7.3-5, 10% void was arbitrary located at different proximities (void location A-C) to the heat generating source as depicted in Figs. Figure 7.3-13b-d representing corner voids. Additionally, 10% void area was positioned near the centre of the heat generating chip (Figure 7.3-13e) representing centre void (void location D). A depiction of solder layer without void is presented in Figure 7.3-13a to serve as a reference. The solder voids are 0.04mm deep in a solder layer of 0.04mm thickness. While the heat distribution effects of the four different void locations are as shown in Figure 7.3-14(b-e), Figure 7.3-14a delineates the temperature contour at the back surface of the chip when there is no void in the solder layer as a reference.

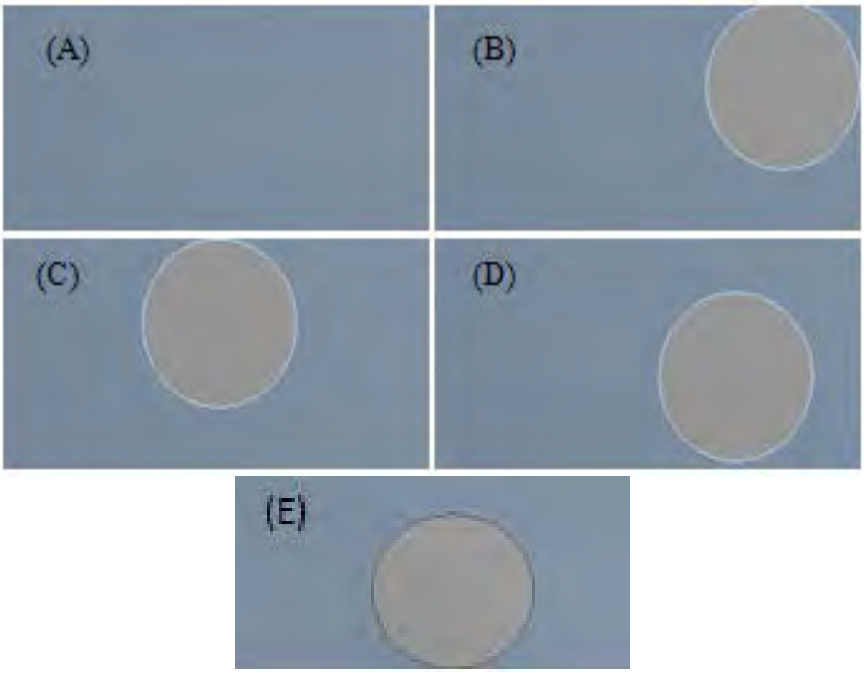



Figure 7.3-13:Void locations(A) shows solder layer without void (B) shows void location A (C) shows void location B (D) shows void location C. (E) shows void location D.(Not drawn to scale)

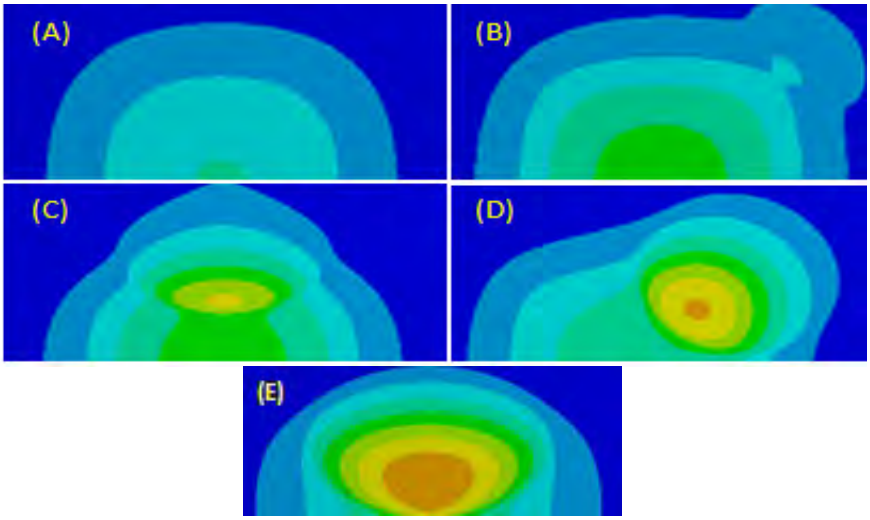



Figure 7.3-14: Heat distribution effects on the back surface of the silicon chip(A) when there is no void (B) as a result of void location A (C) shows hot spot as a result of void location B (D) shows hot spot as a result of void location C (E) shows hot spot as a result of void location D. (Not drawn to scale)

Visual inspection of the temperature contour at the back surface of the silicon die reveals that voids significantly impede thermal path as delineated in Figure 7.3-14b-e with reference to Figure 7.3-14a. A strong upshot of void location on die back surface temperature is evident.

One can easily differentiate the void location as it is qualitatively reproduced on the back surface temperature contour of the chip. At different locations, the void location results in a progression of high temperature points around the void. The result data as presented in Figure 7.3-15 shows that the closer the void is to the heat source, the higher the θ-JC. This is comparable to the result of the work by Ciampolini et al. [64] where corner-void was accountable for a peak temperature less than that of centred void effect. θ-JC rise (Figure 7.3-16) as compared to assembly with no void in the solder die attach layer is 0.1% when the void is furthest from the heat source (void location A), 2.9% when further (void location B) and 33.5% when the void is closer to the heat source (void location C). θ-JC significantly rises to 107.4% for centre void (void location D) positioned near the centre of the heat generating chip. The findings from the present study actually suggest that a void located at the edge of a solder layer may not result in hot spot (representing the hottest spot at the chip surface as suggested by the work of Fleischer et al. [62] and Biswal et al. [184]; this is because the active area in a real chip is smaller than the total chip area, and hence the void percentage under the un-active area does result in a relatively lower thermal resistance as evident from the less significant rise (0.1%) in θ-JC due to void location (A) (Figure 7.3-14b).

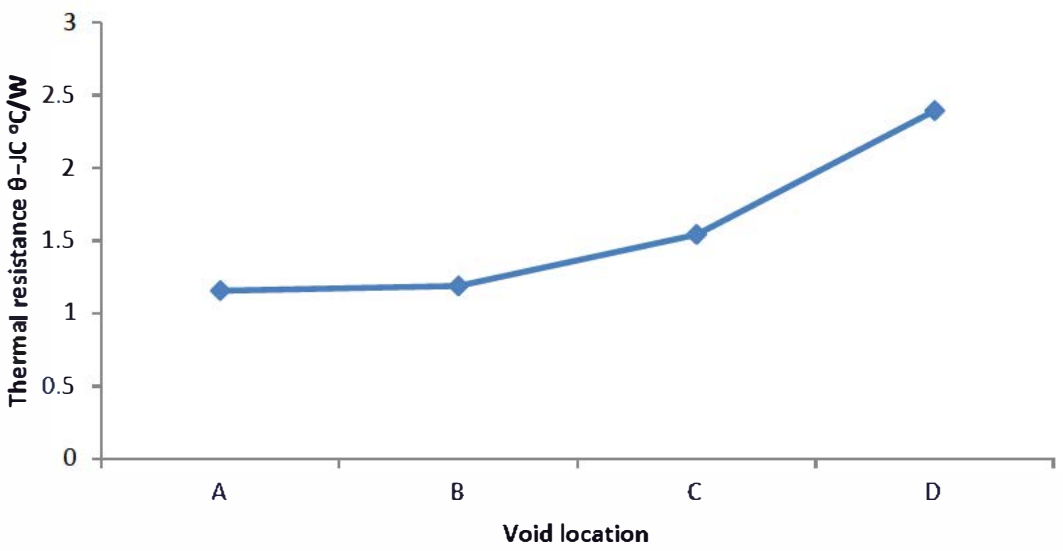



Figure 7.3-15: Thermal effects of the four different void locations

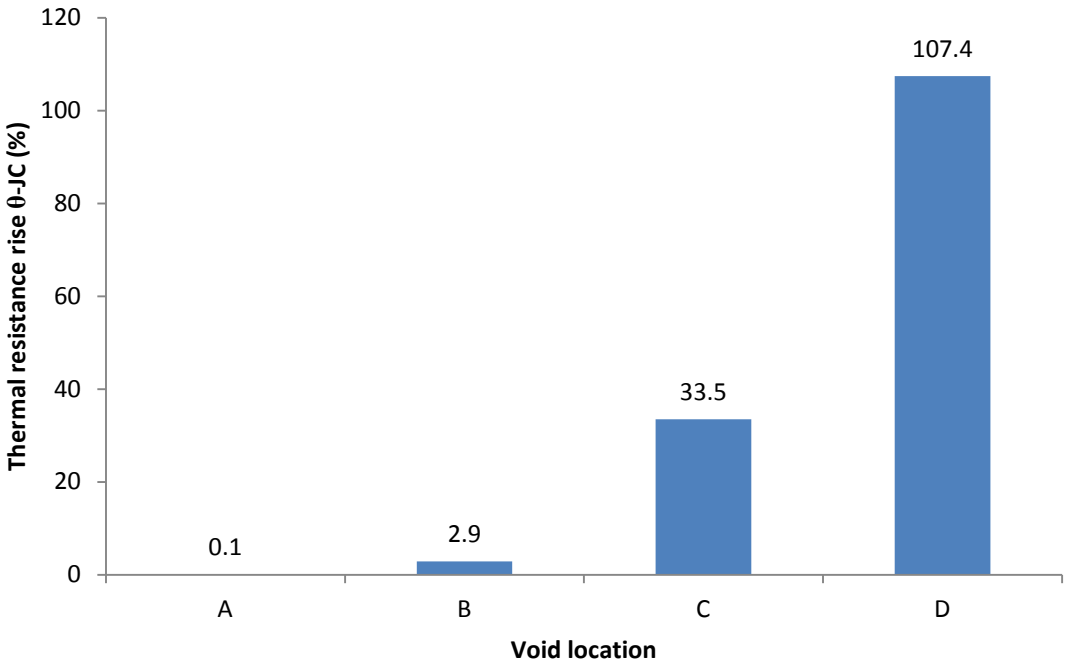



Figure 7.3-16: Comparison of θ-JC rise due to the different void locations

## 7.4 Summary

In this study, thermal simulations have been performed to characterise the thermal effects of different numerically controlled solder die attach void patterns on the performance of chip-level packaged power device. An analytical approach referred to as θ-JC (thermal resistance) was employed to understand and explain the findings. The following are findings of this study:

- θ-JC values are dependent on the heat generating area of the chip.
- Large single void has a more detrimental impact on θ-JC compared to small distributed voids of equivalent void percentage.
- Shallow voids formed in the solder die attach layer next to the surface of the heat generating chip result in a relatively higher θ-JC than equivalent shallow voids present at other vertical positions further from the heat generating chip. Nonetheless, through-thickness void (voids extending through the whole solder layer) in the same lateral position as the shallow voids is accountable for the highest θ-JC values.
- θ-JC is highest for voids present near the center of the heat source. A void at the edge (very far from the heat source) of the solder die attach layer may not result in hot spot (representing the hottest spot at the chip back surface).

# Chapter 8: Comparative study on voiding level and shear strength for Lead-free STIMs subjected to thermal ageing: Experimental study

## 8.1 Introduction

The European Union restriction of hazardous substances (RoHS) directive (2002/95/EC) [157] which became effective on July 1, 2006 requires the removal of lead (Pb) from solder interconnections. This requirement implies the testing and qualification of existing and new electronic packages using Pb-free solders. Thus, the reliability of Pb-free solders has remained a subject of research interest. Albeit compositions in the Sn-Ag-Cu (SAC) ternary system have been widely accepted and preferred as replacements for the traditional Sn-Pb solder alloys [214, 238, 258-259], other Pb-free solders are presently being considered or even used for electronic interconnections and packaging applications. For example, alloys containing bismuth or indium and other elements that exhibit high thermal conductivities are at times employed as TIMs to improve thermal transfer from the chip to the heat spreader.

While the focus as regards implementing these Pb-free solders as thermal interface materials (die-attach) has been on decreasing thermal resistance path [211], it is highly essential to evaluate and understand the mechanical reliability of these solders when employed as TIMs under exposure to high temperature. This is because the application of these solders often experience elevated temperature for a long period of time during service life. For example, in the automotive under-hood, components and interconnects can be subjected to temperature in the region of 125$^{o}$C or above for extended periods of time [231]. Hence, high temperature storage (thermal ageing) is one of the reliability tests employed to simulate the effects of such high temperature exposure over an extended period of time.

Considering that lead-free solders are comparatively more prone to voiding, an extensive examination of these alloys is necessary in order to understand their voiding potentials and reliability as TIMs especially under exposure to high temperature. This chapter provides a comparative study on the voiding level and mechanical durability (shear strength) of representative Pb-free STIMs under different thermal ageing durations, with emphasis on SAC305. This study would attempt to correlate the significance of void level with mechanical durability of the solder joints. Successful Pb-free solder alloys should manifest low voiding levels and relatively high and stable mechanical strength during temperature excursion of at least 125$^{o}$C.

This chapter is divided into four sections including the introduction. Section two presents the materials used for the experiment and the experimental procedures. The results of the experiment including study on voiding levels, study on shear strength and correlation of

voiding level and shear strength values are covered in section three. Finally, section four gives a summary of the details discussed in the chapter.

## 8.2 Materials and experimental procedure

The Pb-free solders under investigation are as shown in Table 8.2-1. Firstly, standard wetting tests (trial tests) were carried out using two copper substrates of dimensions 10x10x0.3mm (representing the die) and 20x20x0.3mm (representing the heat spreader) to find out the parameter limitations for the reflow profiles of the different solder performs. The reflows were done in a SM 500CX Batch forced convection type oven (Figure 8.2-1). The temperature and time of the four different zones were varied in accordance to the solder preforms manufacturer's guide to get the reflow parameters (shown in Table 8.2-2) that produced good bond and thus were used for the main experiment.

Table 8.2-1: Investigated solder preforms

| **Nomenclature** | **Solder composition (wt%)** | **Melting point/range ($^{o}$C)** | **Thermal conductivity (W/mK)** |
|---|---|---|---|
| SAC | 96.5Sn3Ag0.5Cu (SAC305) | 217-220 | 50* |
| Bi/Sn | 58Bi42Sn (eutectic) | 138 | 19 |
| In | 99.99In (eutectic) | 157 | 86 |
| In/Ag | 97In3Ag (eutectic) | 143 | 73 |

*[75]


Figure 8.2-1: SM500 CXE 'Batch' convection reflow oven

Table 8.2-2: Parameters used for the reflow profile

| Solder Type | Zone 1 (Preheat) Temperature ($^oC$) | Zone 2 (Soak) Temperature ($^oC$) | Zone 3 (Reflow) Temperature($^oC$) | Zone 4 (Peak) Temperature ($^oC$) |
|---|---|---|---|---|
| SAC | 180 | 180 | 220 | 240 |
| Bi/Sn | 150 | 150 | 160 | 180 |
| In | 150 | 170 | 180 | 197 |
| In/Ag | 150 | 163 | 170 | 190 |
| **Duration (s)** | 60 | 120 | 180 | 120 |

A total of sixteen (16) test vehicles were then used for the main experiment. A single test vehicle consists of a solder layer sandwiched between metallised silicon die and copper heat spreader. The backside of the die was metallised with Ti/Ni/Ag layers. The dimensions for the copper heat spreader were 20mmx20mmx0.3mm, eight of the metallised silicon die were of size 2.65mm x 3.15mm x 0.43mm and the other eight were of size 2.59mm x 3.73mm x 0.43mm, the different solder performs were 0.05mm thick and were cut according to the sizes of the silicon die. This is further illustrated in Table 8.2-3.

Table 8.2-3: Dimensions of package assembly constituents

| Parameter | Silicon die | | Solder preform | | Copper heat spreader |
|---|---|---|---|---|---|
| | **8** | **8** | **8** | **8** | |
| Length (mm) | 2.65 | 2.59 | 2.65 | 2.59 | 20 |
| Width (mm) | 3.15 | 3.73 | 3.15 | 3.73 | 20 |
| Thickness (mm) | 0.43 | 0.43 | 0.05 | 0.05 | 0.3 |

The assembly process as schematically shown in Figure 8.2-2 commenced with the cleaning of copper heat spreaders with isopropanol, distilled water and finally acetone. A commercially available flux operating at 125$^o$C - 350$^o$C temperature from Indium Corporation [260] was then applied on the heat spreader. Solder preforms from the different solder alloys were cut out according to the sizes of the different metallised die and manually placed on the copper

substrates, the metallised backside of the silicon die were then placed on top of the solder preforms. The soldering was carried out with SM500 CXE convection type reflow oven using the different reflow parameters shown in Table 8.2-2 for the different solder performs.

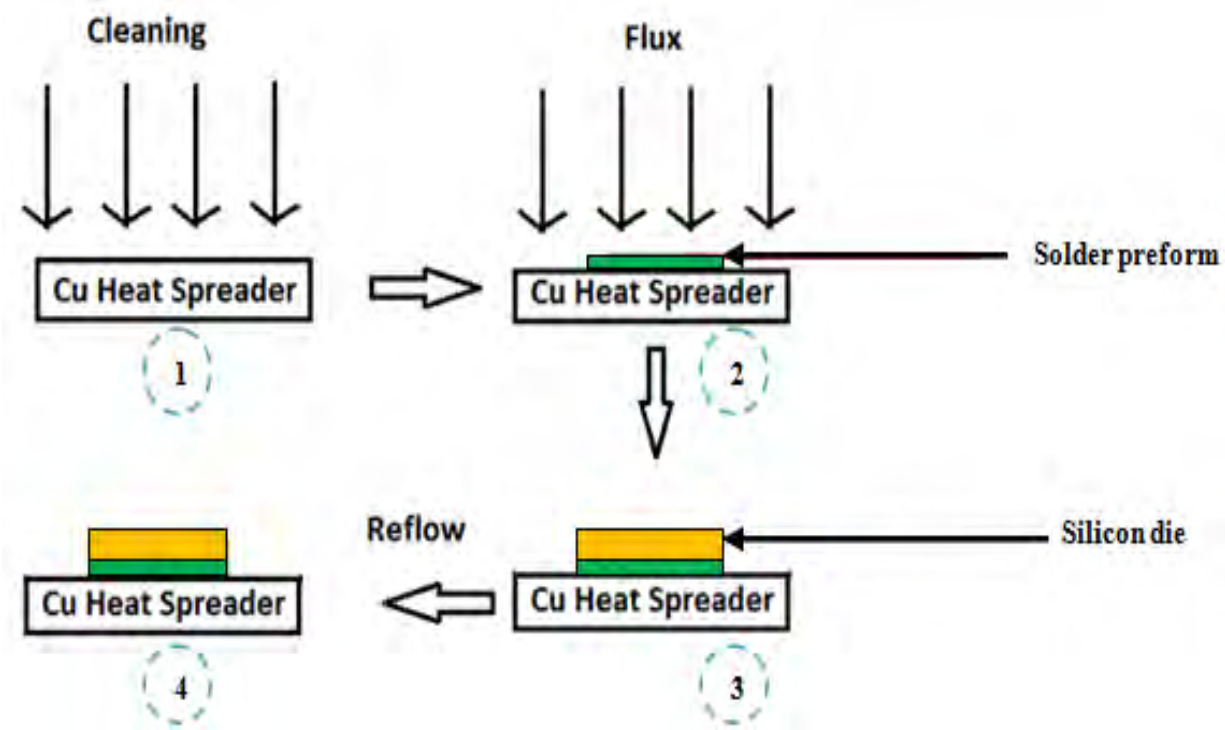



Figure 8.2-2: Schematic of the assembly process

The as-soldered samples were grouped into four batches. Each of the batches consisted the four different solder preforms sandwiched between the same size of die and copper heat spreader. Samples were subjected to thermal ageing at 125$^{o}$C (with a tolerance of ± 10$^{o}$C) for 50 hours, 100 hours, 200 hours and 300 hours. An example of the thermal ageing profile obtained from the chamber (Figure 8.2-3) for 50 hours of ageing is shown in Figure 8.2-4. It should be noted that the ageing temperature (125$^{o}$C) is one of the standard high temperatures in both JEDEC [261] and MIL-STD standards (MIL-STD-750C) [262-263]. Also, 125$^{o}$C is deemed suitable for all the Pb-free solders that are being evaluated in this study considering the low melting point of some of the alloys like Bi/Sn with a melting point of 138$^{o}$C. It is worth knowing that subjecting the samples to thermal ageing is likely to produce solder joints with different levels and distribution of voids. At the end of each thermal ageing time, one batch was taken out to check the percentage of void content of the Pb-free solder joints using the X-ray tool. The following procedures were employed in order to successfully calculate the solder voids percentage:

- The samples were placed inside the X-ray machine and the intensity of the X-ray beam adjusted to obtain a clear image of the test vehicles.
- When a clear image was displayed on the X-ray screen, the region of interest (ROI) was marked with a selection tool. Areas of the silicon die were selected as the region of interest.
- The closure and threshold were fixed for the entire samples. The threshold level is set in such a manner that the interior of the voided areas are covered with red colour as shown in Figure 8.3-1.
- The software then give the percentage voids in each solder layer for each sample.

Figure 8.2-3: The chamber used for Isothermal ageing

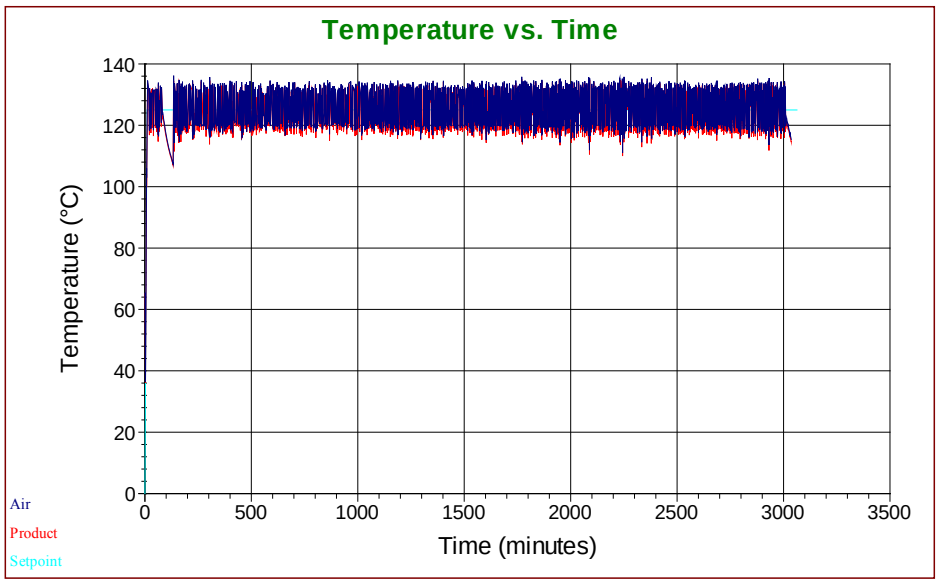



Figure 8.2-4: Temperature vs time graph obtained for 50 hours ageing

After the voiding inspection, shear tests were subsequently carried out on the four types of solder in a batch. A shear tester (Type Series 4000) from Dage Precision Industries was used. The parameters for the shear test were as listed in Table 8.2-4.

Table 8.2-4: Parameters for shear test

| | |
|---|---|
| **Test speed** | 700.0µm/s |
| **Test Load** | 75N |
| **Maximum Test Load** | 500.0N |
| **Land Speed** | 500.0 µm/s |
| **Shear height** | 100 µm |

## 8.3 Experimental results

Based on the manner the results were analysed, this section will be reported in three parts:

### 8.3.1 Study on voids

The void percentages after thermal ageing at 50 hours, 100 hours, 200 hours and 300 hours are accordingly depicted in Figure 8.3-1. The red spots in the images indicate the presence of voids.

Void occurrence reportedly [264] increases when the substrate area to be soldered is comparatively large (like soldering a heat spreader onto a die). The large flat silicon area that

is perpendicular to the substrate (heat spreader) impedes out-gassing during the soldering process. Hence, the slow out-gassing of the solder flux by-products (both liquid and gases) could result in some of the gases being entrapped within the solder joint and subsequently lead to an increase in the level of voiding.

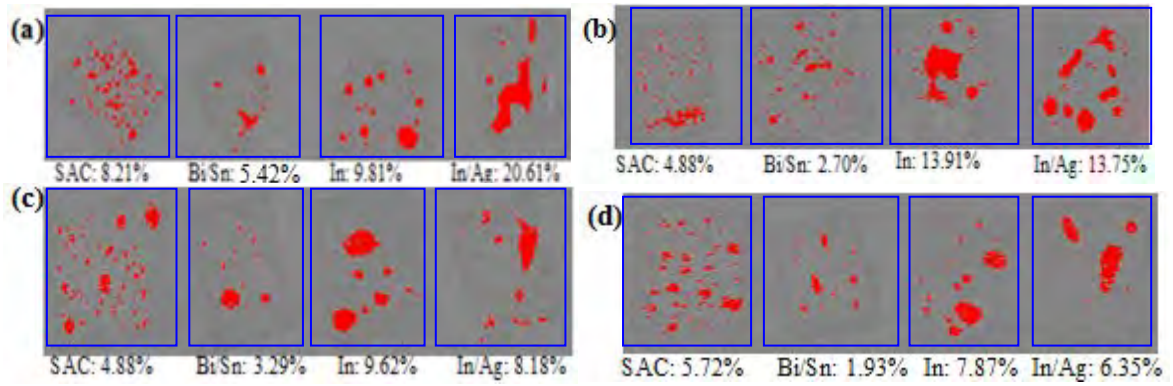



Figure 8.3-1: X-ray image showing solder voids after thermal ageing of the samplesfor (a) 50 hours (b) 100 hours (c) 200 hours (d) 300 hours. Void enclosures in the solder layer are visible as red spots. Theoritical preform sizes are 2.65mm x 3.15mm x 0.43mm and 2.59mm x 3.73mm x 0.43mm.

The high flux activity under exposure to elevated temperature could have resulted in the relatively low level of voiding. Xu et al. [265] suggested that the selection of a more highly activated flux is vital to the promotion of wetting in Pb-free soldering. The surface tension between the molten solder and substrates is decreased and wetting improves as fluxing reaction increases under exposure to high temperature for a long time [264].

Based on the average values of voiding across thermal ageing time as shown in Table 8.3-1, Bi/Sn and SAC alloys comparatively manifested lower voiding levels. As both alloys contain Sn unlike In and In/Ag, the low voiding level in SAC and Bi/Sn over the thermal ageing time could be attributed to the reportedly improved wetting ability of Sn [266]. The addition of Sn is suggested to improve the wetting ability of SAC and Bi/Sn alloys and thus allows the molten solder to more effectively fill up the air voids and the surface area available for soldering during temperature soak. The higher surface tension of In might have also contributed to a reduction in spreading out of In containing solder alloys which could impede the wetting ability of the studied In and In/Ag solder alloy and subsequently lead to the presence of more voids, comparatively. In addition, the higher surface tension of In and In containing solder alloys compared to the Sn-based alloys could also increase the potential of

trapping unwanted volatiles within the molten solder; as these volatiles cannot easily escape from the solder, voids are formed when these compounds remain in the body of the solidified solder joint.

Table 8.3-1: Void percentage for each solder across thermal ageing time

| Solder type | Void percentage (%) | | | | Average values of Voiding level across thermal ageing time |
|---|---|---|---|---|---|
| | 50 hours | 100 hours | 200 hours | 300 hours | |
| **SAC** | 8.10 | 4.88 | 4.88 | 5.72 | **5.89** |
| **Bi/Sn** | 5.42 | 2.70 | 3.29 | 1.93 | **3.33** |
| **In** | 9.81 | 13.91 | 9.62 | 7.87 | **10.30** |
| **In/Ag** | 20.61 | 13.75 | 8.18 | 6.35 | **12.22** |

### 8.3.2 Study on Shear strength

In the electronics industry, shear test is often carried out in order to obtain the force at which a component joint can be "sheared"; hence, shear strength depicts the joint strength. Usually, the harder the solder joint, the greater the shear force value required to shear the component and the more stronger and reliable the solder joint.

The shear force values (shown in Table 8.3-2) obtained from the Dage bond machine were used to calculate the shear strength of the solder joint using the equation:

$$\tau_{sj} = \frac{F}{A_{wj}} \qquad (8.3\text{-}1)$$

Where $\tau_{sj}$ is the solder joint shear strength, F is the shear force applied to the joint and $A_{wj}$ the wetting area of the solder joint [267]. It should be noted that each of the eight silicon die used for 50 and 100 hours ageing has an area of 8.35mm$^2$ and the other eight silicon die employed for 200 and 300 hours ageing has an area of 9.66mm$^2$.

Figure 8.3-4 show images of one of the samples subjected to shear test. The analysis would focus on SAC305 as the material of interest. Generally, as observed in Figure 8.3-5, the effect of thermal aging on solder joints can be divided into two categories based on the inherent features of intermetallics with regards to their strengthening or degradation effect on solder joint [268]:

- Strengthening stage: Strength of solder joint remains the same or increases to a small extent as a result of increased intermetallic strengthening and annealing
- Degradation stage: Strength of solder joint decreases because of the formation of relatively thicker, rougher, and more porous intermetallics

Shear strength results (Figure 8.3-5) show that the shear strengths of the studied SAC solder joint are relatively high and are in the region of 10MPa throughout the thermal ageing period. The standard deviation of the set of values obtained for the shear strength of SAC during thermal ageing was 0.34MPa which is less than 1MPa.The results show that the extended periods the SAC alloy was exposed to do not have a significant effect on its shear strength and thus suggest a greater ability of the alloy to maintain consistency under exposure to high temperature for a long time. The possible reason for the relative consistency in shear strength values for the SAC alloy was explained by Peng [269]; It was found that during thermal ageing, the contents of Cu and Ag in Sn matrix are reduced by precipitation of $Ag_3Sn$ and $Cu_6Sn_5$. Fouassier et al. [270] observed not only that $Ag_3Sn$ but also $Ag_4Sn$ formed in the Sn matrix, after annealing at 125ºC for 600 hours. As the precipitation of these compound phases is by solid state diffusion, they are very small and hence have great strengthening effect. These fine precipitates retain or even increase the shear strength of the solder joint by effectively locking dislocation movements and grain boundary sliding in the Sn matrix. It should be noted that with longer ageing time (~ 600-1000 hours) of SAC, coarsening of the IMC particles could occur. In other words, the precipitate particulates could merge into larger ones [271]. These could eventually reduce the strengthening effect of the precipitates. A typical scanning electron microscope (SEM) image of reflowed samples of SAC at various thermal ageing time is shown in Figure 8.3-2. It can be observed that the coarsening of the microstructure grows as the thermal ageing time increases.

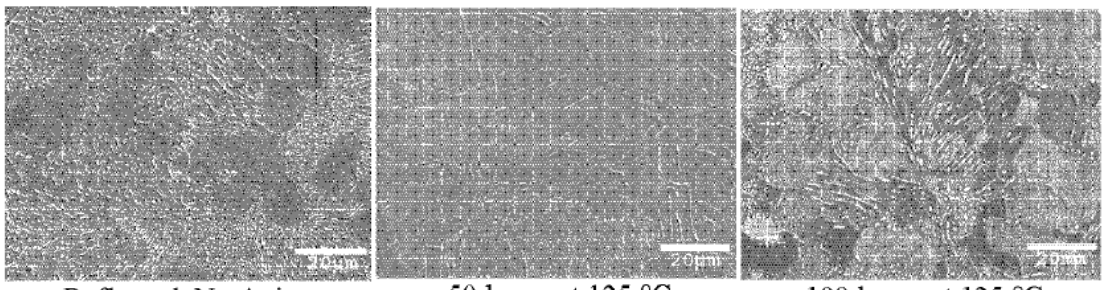



Figure 8.3-2: SAC microstructure as reflowed and after thermal ageing [272]

Even though the magnitude of the shear strength values obtained for In was less than those for the SAC alloy under the same thermal ageing time, similar to the SAC solder joint, there was no significant variation in the shear strength values (within 4MPa) of In as thermal ageing time increases. The standard deviation of the set of values obtained for the shear strength of In during thermal ageing was 0.52MPa which is equally less than 1MPa. Similar result trend as regards the less significant discrepancy in shear strength values of In as thermal ageing time increases was also reported by Ding [273]. The In/Ag alloy shows lower shear strength values and larger variation in the shear strength values compared to SAC alloy. The solder shear strength is seen to increase and decrease across the ageing period. The variation is between 1.5 – 2.5MPa between the test intervals. It can be seen that for the Bi/Sn, there was a rise in shear strength with increase in isothermal ageing time up to 300 hours. Oliver et al. [274] reported that Bismuth alloys manifested high strengths during lower ageing time which was seen to reverse after ageing for about 500 hours. Figure 8.3-3 shows the fracture surface of Bismuth alloy after ageing at 150$^{o}$C for 500 hours. As can be seen in Figure 8.3-3, the grain size significantly increased during thermal ageing and this is suggested to be the primary cause for the decrease in shear strength of the alloy. The brittleness associated with bismuth is suggested to be one reason why the shear strength significantly reduces under this ageing condition. This could be a concern especially considering the long period of time components could be subjected to harsh environment during operation like in the automotive under-hood applications. In this study, samples could only be evaluated up to 300 hours of thermal ageing at 125$^{o}$C due to limited resources.

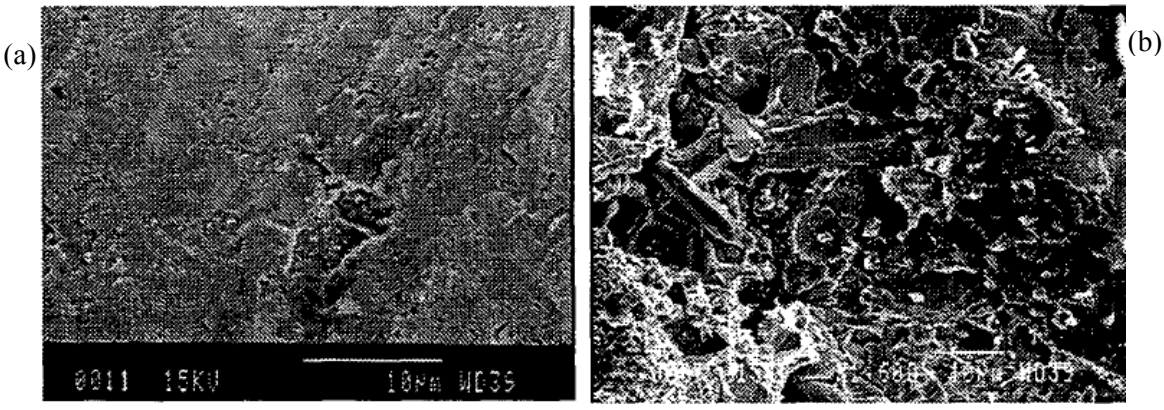



Figure 8.3-3: (a) Fracture surface of non-aged solder alloy (b) fracture surface of solder alloy after ageing at 150$^{o}$C for 500 hours [274]

Based on the aforementioned results, SAC and Bi/Sn appears promising for STIM applications in comparison to other tested Pb-free STIMs. SAC, however, appears a better

choice compared to Bi/Sn. This is because Bi/Sn has lower melting point and thermal conductivity compared to those of SAC and thus, may not withstand the high temperature excursion experienced by devices mounted on the engine of an automotive [231-232]. The brittleness that is associated with Bi/Sn is also a concern for the shock/vibration that could be experienced in the automotive under-hood applications.

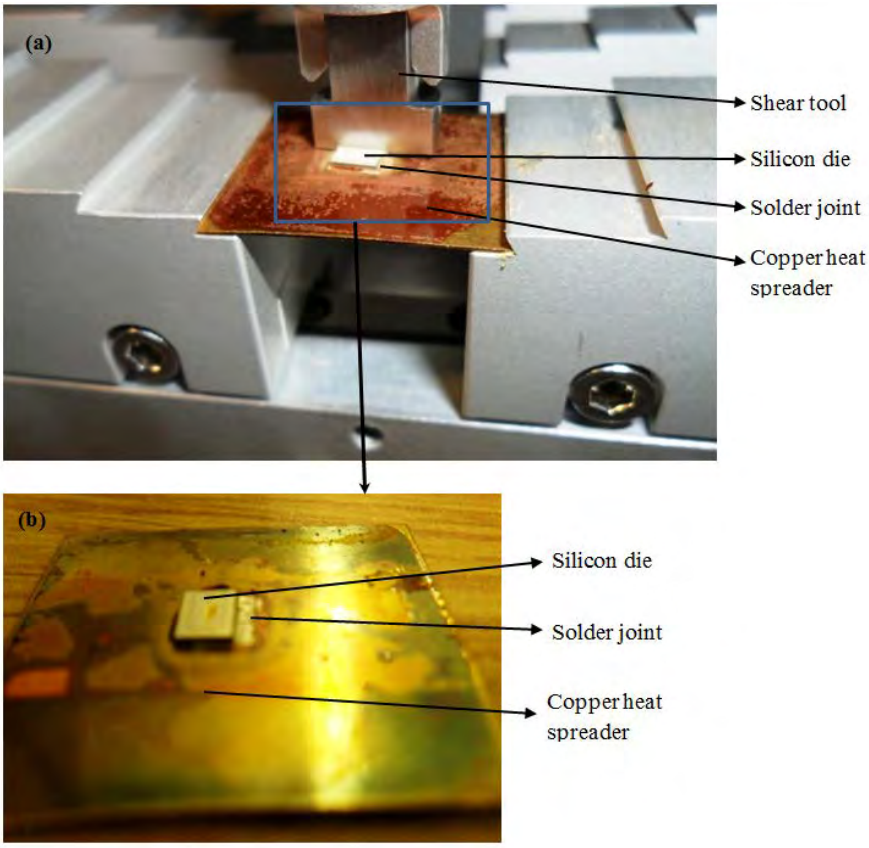



Figure 8.3-4: Images showing (a) sample fixed in the Dage shear machineready for shear testing (b) sample after undergoing shear test

Table 8.3-2: Shear force values

| Solder type | Shear force after each test point (N) | | | |
|---|---|---|---|---|
| | 50 hours | 100 hours | 200 hours | 300 hours |
| **SAC** | 84.65 | 86.48 | 97.48 | 104.80 |
| **Bi/Sn** | 43.21 | 51.00 | 79.81 | 124.96 |
| **In** | 32.10 | 37.69 | 49.43 | 44.41 |
| **In/Ag** | 31.09 | 52.44 | 42.77 | 62.93 |

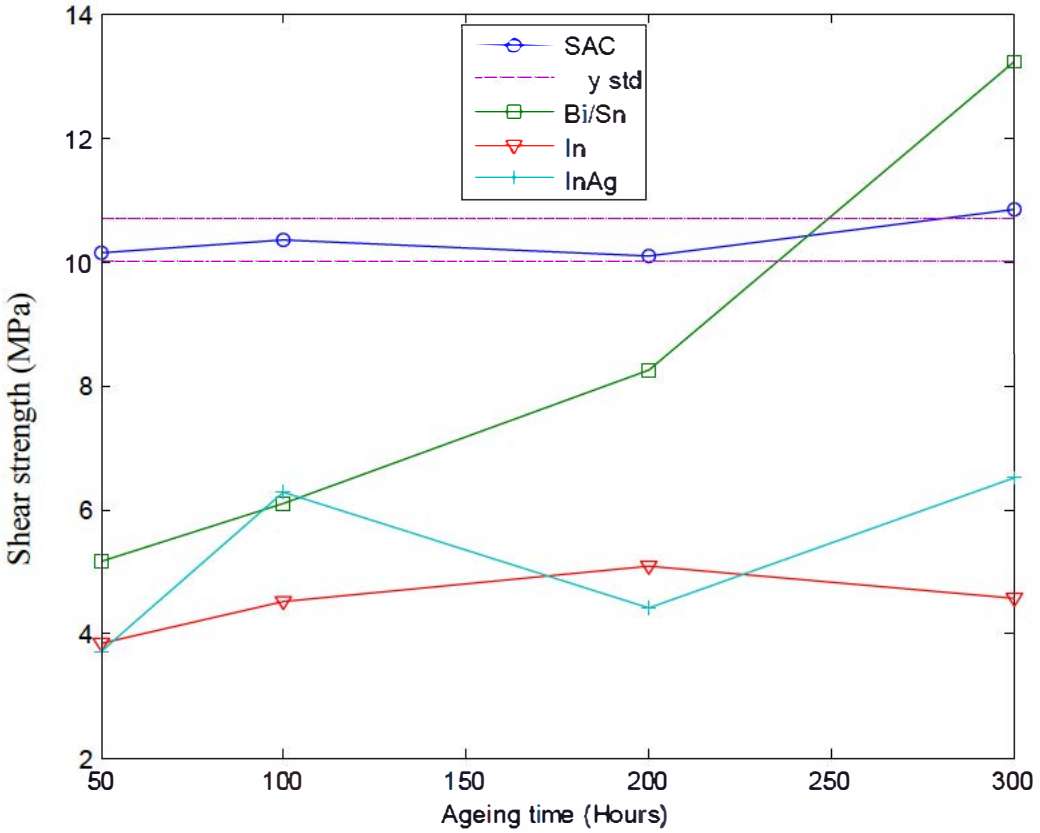



Figure 8.3-5: Shear strength for each thermal ageing time

### 8.3.3 Correlation of voiding level with shear strength

Figure 8.3-6 attempts to correlate voiding level with shear strength. It is difficult to establish a correlation because of the large scatter in the obtained values. The significant scatter as depicted in Figure 8.3-6 could be as a result of different void sizes, shapes and distributions of voids in the STIM layers as observed in the optical assessment of voids (Figure 8.3-1). Similar result trend, although in composite study, was observed in the work of Zhu et al. [275] where significant scatter in strength data was reported for two laminates with similar void content.

Samples with higher void percentages in some cases manifested lower shear strength values when compared to those with lower void percentages. The decrease in shear strength values of the solder joints with relatively higher void percentage could be as a result of the reduction in solder joint cross-sectional area due to voids. Hernandez et al. [276] reported that the interlaminar shear strength of composite laminates was found to be controlled by void volume fraction in panels with porosity above 1%, the interlaminar shear strength decreased

with the void volume fraction for void contents above 1%. Yoon et al. [277] studied the effects of isothermal aging on the joint reliability of a Sn–3.0Ag–0.5Cu (wt.%)/organic solderability preservative (OSP)-finished Cu solder joint; their results showed that the mechanical reliability of the solder joint was degraded by solder voids at the interface.

The varied locations, shapes and sizes of voids in the STIM layers (as observed in X-ray images in Figure 8.3-1) could have influenced the result cases where lower void percentages did not necessarily lead to reduced shear strength values. It has been reported in previous studies [177-178] that the mechanical durability of solder joints is not only affected by the formation of voids but also by the location and configuration of the voids. So, void locations, sizes and shapes [278] play important roles to comprehensively evaluate the influence of voids on mechanical properties as suggested by part of the simulation work in chapter 6. Voids could influence crack initiation, propagation or arrest crack depending on the location and configuration of the void. Additionally, the effect of IMC could influence and/or potentially overcome the effect of voids on failure mechanisms of the solder joints; a study [233] on IMC layer reported that factors such as the grain shape, randomly distributed grain boundary defects, thickness of the IMC layer and morphology of the solder/IMC interface have an effect on microcrack patterns and the overall mechanical strength of solder joints.

It is good to note that while some of the results on shear strength reported in this chapter have been validated using other experimental studies from literature, the aforementioned results should be confirmed by the evaluation of a higher number of samples. There is need for further experimental study to assess conclusively the effect of void locations and configurations on shear strength of STIM layer. The results in this chapter are only valid for qualitatively estimating the relative shear strength and void level of the studied STIM layers due to the limited number of samples studied.

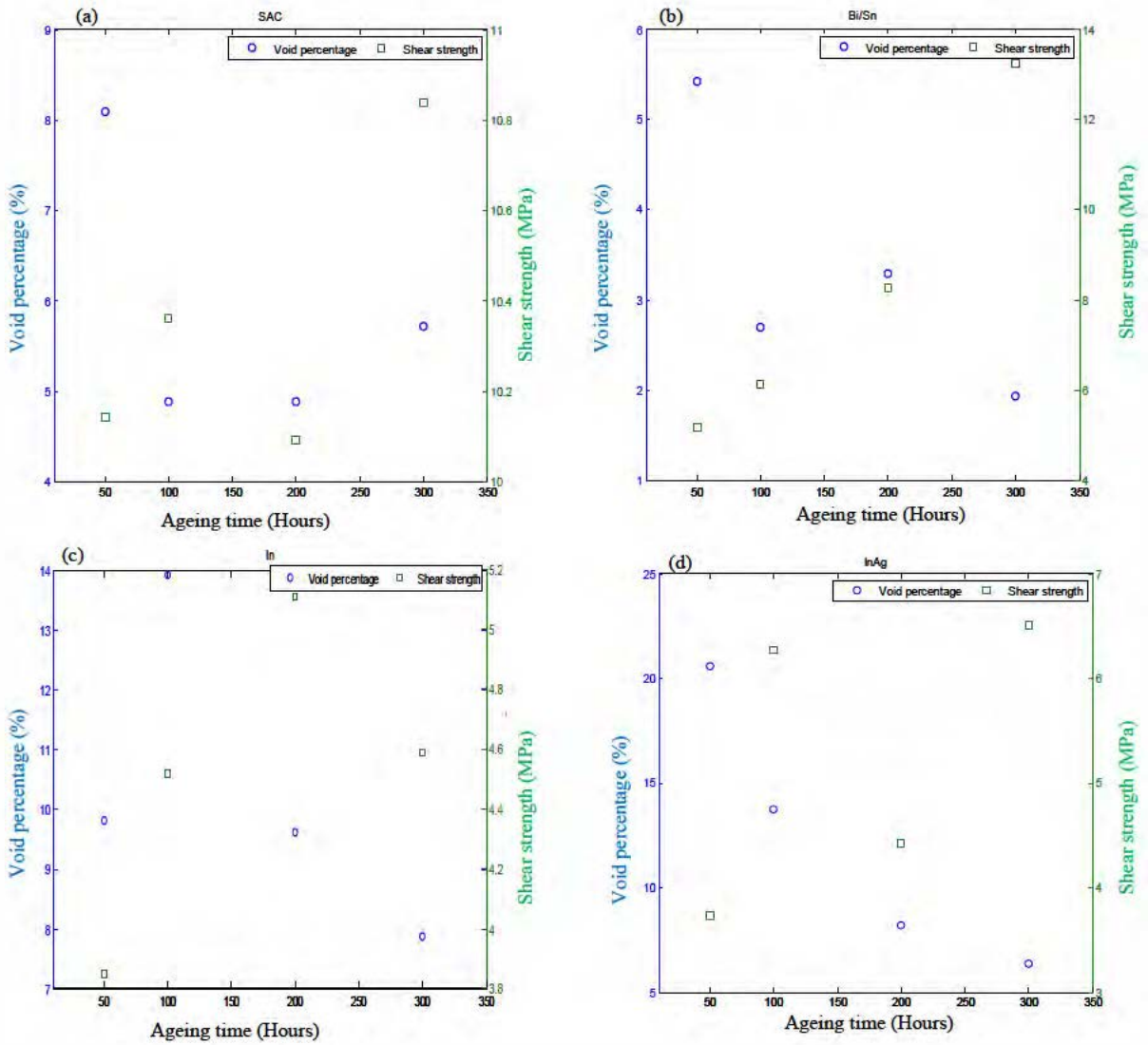



Figure 8.3-6: Void percentage and shear strength for (a) SAC (b) Bi/Sn (c) In (d)In/Ag

## 8.4 Summary

The levels of void content and shear strength of SAC305 and other representative Pb-free STIMs were evaluated under thermal ageing. The sixteen test vehicles consist of the different solder preforms sandwiched between metallised silicon die and copper heat spreaders. After reflow soldering, the samples were subjected to different thermal ageing time. SAC and Bi/Sn relatively manifested lower voiding percentage across the thermal ageing durations. After the inspection of the solder joints for voids, shear tests were subsequently carried out on the samples. Comparatively, the shear strength of SAC is higher and there was no significant change in the magnitude of shear strengths of SAC throughout the ageing period. This suggests a greater ability of the SAC305 alloy to maintain consistency under exposure to high temperature for a long time. In and In/Ag relatively showed lower shear strength values

compared to SAC. In general, based on the comparative results, SAC appears the most promising for STIM applications especially for harsh condition.

Correlation between voiding percentage and shear strength showed that high void percentages resulted to lower shear strength values (mechanical durability) in some cases but not in all cases. The different locations, shapes and sizes of the voids as observed in the X-ray images could have influenced the cases where higher void percentage did not necessarily result in lower mechanical durability of the solder joints. So, void locations, sizes and shapes play important roles to comprehensively evaluate the influence of voids on mechanical properties as suggested by part of the simulation work in chapter 6. Due to the limited number of samples studied in this chapter, there is need for further experimental work to assess conclusively the effect of void locations and configurations on shear strength of STIM layer.

# Chapter 9: Summary, conclusions and recommendations

## 9.1 Introduction

This chapter consists of two main sections including summary and conclusions based on works that have already been carried out as detailed in chapters 2-8 and recommendations for further work emanating from task which could not be completed within the time frame of this research work. The detail of each part is as below:

### 9.1.1 Summary and conclusions

Solder-based thermal interface material (STIM) apparently offer promising solution to improve the thermal performance of TIMs due to its relatively higher thermal conductivity and low thermal resistance compared to its tradition polymer-based counterparts; nonetheless, voiding has been identified as the major reliability concern of STIMs. Process induced voids in the solder die-attach layer could affect the thermal and mechanical performances of STIMs. These inevitable voids even become more critical as the electronic component and resulting solder interconnects become smaller like in a chip-scale package. The level of understanding about the effect of voids on the reliability of electronic components, however, still remains speculative and very little work has been reported on this subject especially with regards to solder die-attach layer. As a result, this work provides the first comprehensive study on the effect of voids on the thermo-mechanical and thermal performance of solder die-attach. In presenting the conclusions of this work, the contributions to literature should be assessed based on work done on solder die-attach layer and void configurations.

#### *9.1.1.1 Generation of random voids distribution and selection of a suitable Pb-free STIM layer*

A MATLAB algorithm was developed for the generation of representative volume element (RVE) of random spatial distribution of voids in a given solder joint. The algorithm is based on a well reported model, where the void placement and subsequent populating of a defined RVE window with non-overlapping voids are done according to Monte Carlo approach. This is the first time this approach has been used for solder voids modelling. The generated RVEs were firstly obtained as 2D RVEs and the generated 2D RVEs were subsequently extruded to form the required 3D RVE. While the former was implemented in MATLAB coding environment, the latter was carried out using a Java Script run within ANSYS Design Modeler Scripting User Interface.

Extensive thermal fatigue modelling suggests a favourable preference of SAC305 solder for studies on the effect of solder voids compared to SAC405. Simulation results showed that there is less significant difference between the fatigue life of SAC305 (which is relatively

cheaper) and SAC405 under harsh thermal-cyclic loading (-65 to +150$^{o}$C) representative of condition experienced by components placed in the automotive under-hood next to the engine. This is beneficial to the automotive industry considering the extreme cost constraints being undergone by the industry and that the relatively lower flow stress of SAC305 would play a key role in the absorption of shock/vibration on electronic components for automotive application. Visual inspection of damage contour distribution show that in a die-attach layer (large solder joint), regardless of the solder composition, damage often initiates from a small region at the edge of the solder joint. This critical site (damage initiation area) occupies a shallow depth from the surface of the solder joint region near the silicon die.

#### *9.1.1.2 Extensive thermo-mechanical simulation – Parametric studies on voids*

Previous research on solder voids suggests that the exact impact of voids on solder joints apparently depends on the size, location, percentage and configuration of voids. For elucidation purposes, extensive finite element modelling was employed in this work for detailed and precise analysis of the influence of void size, location, percentage and configuration on the thermo-mechanical of Pb-free solder die-attach layer. Parametric studies were carried out employing FEM to investigate the impacts of the different numerically generated random void configurations, sizes, volume fraction and locations on the thermo-mechanical performance of SAC305 STIM layer. Results suggest that the precise nature of the effect of voids on the thermo-mechanical performance of the studied solder joints depends on the size, percentage, location, and the distribution of the voids. Conclusions are as follows:

i. The sensitivity of solder joint fatigue life to the configuration of voids increases as the void percentage increases.
ii. Different void configurations would result in different damage distribution which could affect the rate of damage initiation and propagation. The effect of large voids on obtained damage parameters in the studied solder joints was more profound compared to small randomly distributed voids. It was observed that the small voids around the critical region of the solder joints appeared to enhance stress and strain localisation around the maximum damage site, thus facilitating damage initiation. Nonetheless, the small voids also showed potentials of arresting the damage propagation by blunting the crack tip and hence increase the overall fatigue life of the solder joint.

iii. Strain energy in the solder joint increases as void becomes closer to the critical site which may enhance damage initiation. When the voids are further away from the critical region, they do not alter/influence the damage distribution in the solder joint.

iv. Voids located in the surface of the solder joint is more detrimental compared to void embedded in the middle of the solder layer. Precisely, void situated in the surface between the solder joint and silicon die (where the critical site is located) is more detrimental to the solder joint reliability in comparison with void located in the solder/copper interface. This is in agreement with the IPC (IPC-A-610, IPC-7095) standard that regards voids at the interface as higher risk voids relative to the voids embedded in the solder joint.

These conclusions may translate to strict void inspection criteria for die-attach joints with large voids, joints with voids close to the critical site and void located at the interface of the solder joint and the chip.

#### *9.1.1.3 Extensive thermal simulation – Parametric studies on voids*

Thermal simulations were also performed to comprehend and characterise the thermal effects of the different numerically generated solder void sizes, configurations, percentage and location on the performance of chip-scale packaged power device. Conclusions are that:

i. Thermal resistance values are dependent on the heat generating area of the chip.

ii. Large voids have more detrimental impact on thermal resistance values compared to small distributed voids of equivalent void percentage.

iii. Shallow voids formed in the solder die attach layer next to the surface of the heat generating chip result in a relatively higher thermal resistance values compared to equivalent shallow voids present at other vertical positions further from the heat generating chip. Nonetheless, through-voids (voids extending through the whole solder layer) in the same lateral position as the shallow voids is accountable for the highest thermal resistance values. A void at the edge (very far from the heat source) of the solder die-attach layer may not result in hot spot (representing the hottest spot at the chip back surface).

Based on these conclusions, more attention should be given to large voids, centre voids and through voids when setting standards for solder joint inspection. Heat generating area should also be taken into consideration in the application of thermal resistance values in actual systems.

#### *9.1.1.4 Experimental investigation on voiding level and shear strength for representative Pb-free solders*

Following the numerical investigations, an experiment study was conducted using different Pb-free solder thermal interface materials (including SAC305) sandwiched between silicon chip and copper heat spreader. After reflow processes, the different solder joints were subjected to thermal ageing and characterised for voids percentage at set test time. In order to evaluate the integrity of the solder joints under thermal loading due to solder voids, the samples were tested for shear strength. Comparatively, SAC305 and Bi/Sn manifested lower voiding levels and results suggested a greater ability of the SAC305 alloy to maintain consistent higher shear strength values under exposure to high temperature (125$^{o}$C) for a long time (300 hours). Hence, SAC305 appears the most promising for STIM application especially for harsh condition. Correlation between voiding percentage and mechanical durability showed that high void percentages resulted to lower shear strength values (mechanical durability) in some cases but not in all cases. The different locations, shapes and sizes of the voids as observed in the X-ray images could have influenced the cases where higher void percentage did not necessarily result in lower mechanical durability of the solder joints. So, void locations, sizes and shapes play important roles to comprehensively evaluate the influence of voids on mechanical properties as suggested by part of the simulation work in chapter 6. Due to the limited number of samples studied in this work, there is need for further experimental work to assess conclusively the effect of void locations and configurations on shear strength of STIM layer.

## 9.2 Recommendations for future work

Based on the insight obtained from this work, future works are recommended to improve the FEA modelling and analytical approaches employed in this research work. These suggestions are presented in two sub-headings.

### 9.2.1 General recommendation

Although experimental studies from literature were used (where appropriate) to validate the results from the computer and numerical modelling approaches employed in this research work; it would be highly beneficial to empirically re-validate the findings of the numerical modelling adopting the already set down modelling parameters and materials. This would essentially improve the results of the research work reported in this thesis.

### 9.2.2 Specific recommendations

The specific recommendations are discussed in six sub-headings as follows:

#### i. More experimental characterisations

The studies conducted to explore the influence of voids only assessed the effect of voids on the shear strength of solder die-attach layer under thermal loading. The findings from this study should be confirmed by evaluating higher number of samples. Also, in order to completely understand the mechanical behaviour of solder die-attach layer, other types of loading such as fatigue, vibration, drop or shock could be explored for future investigations.

#### ii. Representative numerical Models

Though the algorithm used for the numerical models generation was able to implement random spatial distribution of circular voids adopting a Monte Carlo approach, the algorithm can be further improved to incorporate variation of void sizes and shapes within a given representative volume element (RVE). Existing micrographs of voided thermal interface materials not only reveal random arrangement of voids in a given RVE but also various sizes and shapes of voids. The shape of voids within a given RVE is not always circular as considered in the generated numerical models of voids. Voids are formed in different shapes which may influence stress, strain and thermal distribution in the solder die-attach layer.

#### iii. Periodicity of material

Periodicity of material could be incorporated in the future generation of RVEs. Periodicity of the material requires a choice of an RVE with the void-segments balanced on either side of the walls of the RVE. If a fraction of the void appears at one edge, this condition demands that the complementary fraction of the void MUST re-appear on the directly opposite edge of the given RVE. Wall-effects may develop if this condition is not satisfied. Although real materials do not experience this problem (wall-effects), this could be incorporated in RVEs in order to be representative of larger sample.

#### iv. Accumulated damage in large area solder joint

The method of employing damaged parameters averaged over certain thickness of element layers for fatigue lifetime prediction is questionable when the geometry/shape of the solder joint is different from flip-chip solder bumps or BGA solder joints (small area solder joints). This is because damage constants are for specific reference geometry of solder balls. In cases

where the studied joint is different from the reference case like in the studied large area solder joint, these constants cannot be used to correctly predict joint life time. As these damaged parameters are conventionally extracted from a certain volume taken around a critical region in the height direction of the solder bump or solder ball, it is unclear the pattern of the chosen volume of elements in large area solder joints (such as the ones studied in this work). This is because the location of the maximum damage in large area solder joint is often at the corner region which has a different shape and orientation compared to the critical region in small area solder joint. Addressing the foregoing through rigorous experiments and FE modelling could form the basis for future work.

### v. Material properties

The material property of the solder is considered to be homogenous in the FEA modelling. Micro-structural analysis of real solder joints often reveal region of intermetallic layers in the solder joints. These intermetallic layers can have an effect on the thermo-mechanical reliability of solder joints and should be considered in FEA of solder die-attach layer. This will help in developing fatigue life model for solder die-attach based on the in-depth understanding of the failure modes, mechanism and microstructures.

### vi. Thermal simulation

In the thermal simulation carried out in this study, only heat transfer by conduction was considered. Further study can incorporate heat transfer by convection and radiation by perhaps employing computational fluid dynamics (CFD) tool for the analysis. The incorporation of these heat transfer methods is more representative of actual real conditions and can help improve the overall results of the thermal simulation. In addition, further practical approaches and extensive modelling should be directed towards characterizing the performance degradation of CNT based TIMs in order to realize the promise of high thermal conductivity of CNTs with expected reliability.

# References

1. S.S. Tonapi, et al. *An Overview of Thermal Management for Next Generation Microelectronic Devices*. in *IEEE/SEMI Advanced Manufacturing Conference*. 2003.
2. Hu, X.J., et al., *3-Omega Measurements of Vertically Oriented Carbon Nanotubes on Silicon.* Journal of Heat Transfer, 2006. **128**(11): p. 1109-1113.
3. Kumar, S., *Thermal Management of RF and Digital Electronic Assemblies using Optimized Materials and PCB Designs*, in *MILAERO007 - Military and aerospace electronic news and information*. 2012.
4. *Summaries of EU legislation*, in *Euro 5 and Euro 6 standards: reduction of pollutant emissions from light vehicles*. 2010.
5. DieselNet. 1997-2012 [cited 2012 6 December]; Available from: http://dieselnet.com/.
6. Ernesto Gutierrez Gonzalez, Jesus Alvarez Florez, and S. Arab., *Development of the Management Strategies of the ECU for an Internal Combustion Engine Computer Simulation.* Mechanical Systems and Signal Processing 2008. **22**: p. 1356-1373.
7. Campbell, R.J. and K. Rajashekara., *Evaluation of Power Devices for Automotive Hybrid and 42V Based Systems*, in *SAE World Congress. Software/Hardware Systems, Systems Engineering, Advanced Electronics Packaging, and Electromagnetic Compatibility (EMC)*. 2004.
8. DENSO. *Moving Technology*. Cleaner Engines [cited 2010 07/07/2010]; Available from: www.globaldenso.com.
9. *Mikuni VM34SS.* [cited 2010 06/06/2010]; Available from: www.siue.edu/~rsutton/SR/mikuni.htm.
10. *ECU Design Services*, in *Pathway*. 2009.
11. *NTD6415ANL: Power MOSFET* in *Enabling Energy Efficient Solutions*. 1999-2010, ON Semiconductor.
12. Cola, B.A. (2010) *carbon nanotubes as high performance thermal interface materials*. Electronics Cooling.
13. *DTI Global Watch Mission Report*, in *Developments and trends in thermal management technologies - a mission to the USA*. December 2006.
14. Bailey, C. *Thermal Management Technologies for Electronic Packaging: Current Capabilities and Future Challenges for Modelling Tools*. in *Electronics Packaging Technology Conference*. 2008: IEEE.
15. Myers, B.A. (2003) *Cooling Issues for Automotive Electronics*. Electronics Cooling.

16. Bruce A. Myers, Gary Eesley, and D. Ihms (2010) *Electronics cooling in the automotive environment*. Electronics Cooling
17. Fan;, X., K.T. Aung, and X.L. Aung. *Investigation of thermal performance of various power-device packages*. in *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems, 2008. EuroSimE 2008*. 2008 IEEE.
18. Liu, X., X. Jing, and G.-Q. Lu., *Chip-scale packaging of power devices and its application in integrated power electronics modules.* IEEE Transactions on Advanced Packaging, 2002. **24**: p. 206 - 215.
19. Liu, X. and G.-Q. Lu, *Power Chip Interconnection: From Wirebonding to Area Bonding.* International Microelectronics and Packaging Society, 2000. **23**: p. 407-413.
20. Bindra, A., *BGA MOSFETs keep their cool at high power levels.* Electronic design, 1999. **47**: p. 43.
21. Schofield, H. and M. Standing, *Assembly of FlipFET™ Devices*, International Rectifier
22. Wen, S., *Design and Analyses of a Dimple Array Interconnect Technique for Power Electronics Packaging*, in *Material Science and Engineering*. 2002, Virginia Polytechnic Institute and State University.
23. Tunga, K. and S.K. Sitaraman, *Microstructure-evolution and reliability assessment tool for lead-free component insertion in army electronics,*. 2000, The George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology Atlanta.
24. Zdebel, P.J. and M. Tack. *Defining the New Era in Highly Efficient Power Electronics Design*. 2011 [cited 2013 05/08]; Available from: http://www.ecnmag.com/.
25. Wunderle, B., *Thermo-Mechanical Reliability of Flip-Chip Assemblies with Heat-Spreaders*. 2003.
26. Kandasamy, R. and A.S. Mujumdar, *Interface thermal characteristics of flip chip packages – A numerical study.* Applied Thermal Engineering, 2009. **29**(5–6): p. 822-829.
27. P. Teertstra, M.M. Yovanovich, and J.R. Culham, *Calculating interface resistance*, in *ElectronicsCooling*. May 1997.
28. Zhou;, F., et al., *Modeling Heat Transport in Thermal Interface Materials Enhanced With MEMS-Based Microinterconnects.* Components and Packaging Technologies, 2010 **33**: p. 16 - 24

29. Desai, A., J. Geer, and B. Sammakia. *A Statistical Analysis of Thermal Interface Materials Enhanced by Vertically Aligned Carbon Nanotubes*. in *Thermal and Thermomechanical Phenomena in Electronics Systems, 2006. ITHERM '06. The Tenth Intersociety Conference on*. 2006.
30. Maguire, L., M. Behnia, and G. Morrison, *Systematic evaluation of thermal interface materials—a case study in high power amplifier design.* Microelectronics Reliability, 2005. **45**(3–4): p. 711-725.
31. Farhad, S., D.C. Whalley, and P.P. Conway. *Thermal Interface Materials - A Review of the State of the Art*. in *Electronics Systemintegration Technology Conference, 2006. 1st*. 2006.
32. Berry, D.G., *Thermal Management Considerations for PCBs*, in *Measurement techniques and heat conduction*.
33. *Thermal Interface Materials*. 1996-2013 [cited 2012 9 February]; Available from: http://www.indium.com/TIM/.
34. Ram Viswanath, et al. (2000) *Thermal Performance Challenges from Silicon to Systems*. Intel Technology Journal Q3.
35. J.P. Gwinn and R.L. Webb., *Performance and testing of thermal interface materials.* Microelectronics Journal 2003. **34**: p. 215–222.
36. Sim, L.C., et al., *Thermal characterization of $Al_2O_3$ and ZnO reinforced silicone rubber as thermal pads for heat dissipation purposes.* Thermochimica Acta, 2005. **430**(1–2): p. 155-165.
37. Patrick K. Schelling, Li Shi, and K.E. Goodson, *Managing Heat for Electronics*, in *Materialstoday*. 2005. p. 30-35.
38. Frank P. Incropera, et al., *Fundamentals of Heat and Mass Transfer*. 2007, New York: John Wiley & Sons, Inc.
39. Blazej, D. (2003) *Thermal Interface Materials*. Electronics Cooling.
40. Narumanchi, S., et al. *Thermal interface materials for power electronics applications*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2008. ITHERM 2008. 11th Intersociety Conference on*. 2008.
41. Devpura, A., P.E. Phelan, and R.S. Prasher. *Percolation theory applied to the analysis of thermal interface materials in flip-chip technology*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2000. ITHERM 2000. The Seventh Intersociety Conference on*. 2000.

42. Prasher, R.S., *Surface chemistry and characteristics based model for the thermal contact resistance of fluidic interstitial thermal interface materials.* Heat Transfer, 2001. **123**: p. 969-975.
43. Lingbo, Z., D.W. Hess, and P. Wong. *Assembling Carbon Nanotube Films as Thermal Interface Materials*. in *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*. 2007.
44. Fleischer, A.S., et al. *Transient thermal management using phase change materials with embedded graphite nanofibers for systems with high power requirements*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2008. ITHERM 2008. 11th Intersociety Conference on*. 2008.
45. Jun Xu and T.S. Fisher, *Enhancement of thermal interface materials with carbon nanotube arrays.* International Journal of Heat and Mass Transfer 2006. **49**: p. 1658–1666.
46. Yoichi Taira , S. Kohara, and K. Sueoka. *Performance Improvement of Stacked Graphite Sheets for Cooling Applications*. in *Electronic Components and Technology Conference*. 2008: IEEE.
47. Quoc Ngo, et al., *Thermal Interface Properties of Cu-filled Vertically Aligned Carbon Nanofiber Arrays.* Nano Letters, 2004. **4** (12): p. 2403-2407.
48. Linderman, R., et al. *High-performance thermal interface technology overview*. in *Thermal Investigation of ICs and Systems, 2007. THERMINIC 2007. 13th International Workshop on*. 2007.
49. Thermal Gap Pads, Thermally Conductive Pads, (2006).
50. Rauch, B. *Understanding the performance characteristics of phase-change thermal interface materials*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2000. ITHERM 2000. The Seventh Intersociety Conference on*. 2000.
51. Ollila, T., *Navigating the maze of thermal interface materials*, in *Electronic Products Magazine*. 1999.
52. Bischak, G. and C. Vogdes. *Thermal management design criteria and solutions*. in *Northcon/98 Conference Proceedings*. 1998.
53. Chung, D.D.L., *Thermal Interface Materials.* Materials Engineering and Performance, 2001. **10**: p. 56-59.
54. Hurley and e. al, *Metallic solder thermal interface material layer and application of the same,* 2008: United States.

55. Houle, S.J., *Liquid solder thermal interface material contained within a cold-formed barrier and methods of making same*. 2007: US.
56. Reddy, G.P., et al. *Co-electrodeposited graphite and diamond-loaded solder nanocomposites as thermal interface materials*. in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*. 2010.
57. Subramanian, S.J. *Mechanical Modeling of a Solder Thermal Interface Material: Implications for Thermo-Mechanical Reliability*. 2005 ASME.
58. Chaowasakoo, T., et al. *Indium solder as a thermal interface material using fluxless bonding technology*. in *Semiconductor Thermal Measurement and Management Symposium*. 2009
59. *Solder Thermal Interface Materials*, Indium Corporation.
60. Jane He, D.V. Heerden, and J. Subramanian, *Direct Die Attach Using a Room Temperature Soldering Process*, in *Electronics Cooling*. 2006.
61. Pritchard, L.S., P.P. Acarnley, and C.M. Johnson, *Effective thermal conductivity of porous solder layers.* Components and Packaging Technologies, IEEE Transactions on, 2004. **27**(2): p. 259-267.
62. Fleischer, A.S., L.-h. Chang, and B.C. Johnson, *The effect of die attach voiding on the thermal resistance of chip level packages.* Microelectronics Reliability, 2006. **46**(5–6): p. 794-804.
63. Chia-Pin Chiu, James G. Maveety, and Q.A. Tran, *Characterization of solder interfaces using laser flash metrology.* Microelectronics Reliability, 2002. **42**: p. 93–100.
64. Ciampolini, L., et al., *Modelling thermal effects of large contiguous voids in solder joints.* Microelectronics Journal, 1999. **30**(11): p. 1115-1123.
65. Too, S.S., et al. *Indium thermal interface material development for microprocessors*. in *Semiconductor Thermal Measurement and Management Symposium, 2009. SEMI-THERM 2009. 25th Annual IEEE*. 2009.
66. Fay Hua, Carl Deppisch, and T. Fitzgerald. *Indium as Thermal Interface Material for High Power Devices*. in *Advancing Microelectronics*. 2006: IMAPS.
67. Lewis, B.e.a., *Thermal interface material and solder preforms,* 2010: United States.
68. Prasher, R., *Thermal Interface Materials: Historical Perspective, Status, and Future Directions.* 2006. **94**: p. 1571-1586.

69. Olsen, D. and H.M. Berg, *Properties of Die Bond Alloys Relating to Thermal Fatigue.* Components, Hybrids, and Manufacturing Technology, IEEE Transactions on, 1979. **2**(2): p. 257-263.
70. Zheng, Y., *Effect of surface finishes and intermetallics on the reliability of SnAgCu interconnects*, in *Department of Mechanical Engineering*. 2005, University of Maryland, College Park.
71. Carl Deppisch, et al., *The Material Optimization and Reliability Characterization of an Indium-Solder Thermal Interface Material for CPU Packaging.* Journal of the Minerals, Metals and Materials Society 2006. **58**: p. 67-74.
72. Yuquan, L., et al. *Reliability of flip chip packages with high thermal conductivity heat spreader attach*. in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*. 2008.
73. Luo, X. and D.D.L. Chung., *Effect Of The Thickness Of A Thermal Interface Material (Solder) On Heat Transfer Between Copper Surfaces.* The International Journal of Microdircuts and Electronic Packaging, 2001. **24**: p. 141-147.
74. Gamal Refai-Ahmed, et al. *Comparison of thermal performance of current high-end thermal interface materials*. 2007: ASME.
75. J. Chang, et al., *Finite Element Modeling Predicts the Effects of Voids on Thermal Shock Reliability and Thermal Resistance of Power Device.* Welding Research, 2006: p. 63-s - 70-s.
76. Wang, D., *Experimental Study of Void Formation in Solder Joints of Flip-Chip Assemblies*. 2005, The University of Texas at Austin.
77. *Recast of the WEEE Directive*, European Commission.
78. *Thermal Interface Material Comparison*. Thermal Pads vs. Thermal Grease, (2004).
79. Gerke, D., *Carbon Nanotube Technology*. 2009: Pasadena, California.
80. Quoc Ngo, et al., *Thermal Conductivity of Carbon Nanotube Composite Films.* 2004. **812**.
81. Chuang;, H.F., et al., *Improvement of Thermal Contact Resistance by Carbon Nanotubes and Nanofibers.* Nanoscience and Nanotechnology, 2004. **4** (8): p. 964-967.
82. *ScienceDaily*. Science News (2006).
83. Iijima, S., *Helical microtubules of graphitic carbon.* 1991. **354**: p. 56-58.
84. Iijima, S. and T. Ichihashi, *Single-shell carbon nanotubes of 1-nm diameter.* 1993. **363**: p. 603 - 605

85. D. S. Bethune, et al., *Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls.* 1993. **363**: p. 605 - 607

86. Hoenlein, W., et al., *Carbon nanotube applications in microelectronics.* Components and Packaging Technologies, IEEE Transactions on, 2004. **27**(4): p. 629-634.

87. Baughman, R.H. and A.A. Zakhidov, *Carbon Nanotubes - the Route Toward Applications.* Science, 2002. **297**(5582): p. 787 - 792

88. Weisenberger, M. *Project facts*. Carbon materials 2009 [cited 2010 November 6]; Available from: http://www.caer.uky.edu.

89. P. Kim, et al., *Thermal Transport Measurements of Individual Multiwalled Nanotubes.* PHYSICAL REVIEW LETTERS, 2001. **87**.

90. Eric Pop, et al., *Thermal Conductance of an Individual Single-Wall Carbon Nanotube above Room Temperature.* NANO LETTERS, 2006. **6**: p. 96-100.

91. Heremans, J. and C. P. Beetz, *Thermal conductivity and thermopower of vapor-grown graphite fibers.* Physics Review B, 1985. **32**: p. 1981–1986.

92. J. Heremans, I. Rahim, and M.S. Dresselhaus, *Thermal conductivity and Raman spectra of carbon fibers.* Physics Review B, 1985. **32**: p. 6742–6747.

93. Taejin Kim, et al., *Molecular dynamic simulation of heat pulse propagation in multiwall carbon nanotubes.* Physics Review B, 2007. **76**(15).

94. Kai, Z., et al. *Study on Thermal Interface Material with Carbon Nanotubes and Carbon Black in High-Brightness LED Packaging with Flip-Chip*. in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*. 2005.

95. Lin, W. and C.P. Wong. *Vertically aligned carbon nanotubes for thermal interface materials: Quality control, alignment improvement and laser flash measurement*. in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*. 2010.

96. Tansley, T.L. and D.S. Maddison, *Conductivity degradation in oxygen-aged polypyrrole.* Journal of Applied Physics, 1991. **69**: p. 7711-7713.

97. Shadab Shaikh, Khalid Lafdi, and E. Silverman, *The effect of a CNT interface on the thermal resistance of contacting surfaces.* 2007. **45**: p. 695–703.

98. K. Zhang, et al., *Carbon nanotube thermal interface material for high-brightness light-emitting-diode cooling* 2008. **19**.

99. Jong-Jin Park and M. Taya, *Design of Thermal Interface Material With High Thermal Conductivity and Measurement Apparatus.* 2006. **128**.

100. E. S. Choi, et al., *Enhancement of thermal and electrical properties of carbon nanotube polymer composites by magnetic field processing.* JOURNAL OF APPLIED PHYSICS, 2003. **94**: p. 6034-6039.
101. C. H. Liu, et al., *Thermal conductivity improvement of silicone elastomer with carbon nanotube loading.* Applied Physics Letters, 2004. **84**: p. 4248-4250.
102. Xuejiao Hu, L. Jiang, and K.E. Goodson. *Thermal conductance enhancement of particle-filled thermal interface materials using carbon nanotube inclusions*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM '04.* 2004: IEEE.
103. S. U. S. Choi, et al., *Anomalous thermal conductivity enhancement in nanotube suspensions.* Applied Physics Letters, 2001. **79**: p. 2252-2254.
104. M. J. Biercuk, et al., *Carbon nanotube composites for thermal management.* Applied Physics Letters, 2002: p. 2767.
105. Zhang, K., et al. *Thermal interface material with aligned CNT and its application in HB-LED packaging*. in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*. 2006.
106. Baratunde A. Cola, et al., *Effects of Growth Temperature on Carbon Nanotube Array Thermal Interfaces.* Journal of Heat Transfer, 2008. **130**.
107. S. Shaikh, et al., *Thermal conductivity of an aligned carbon nanotube array.* 2007. **45**: p. 2608–2613.
108. Baratunde A. Cola, et al., *Photoacoustic characterization of carbon nanotube array thermal interfaces.* Applied Physics, 2007. **101**.
109. Baratunde A. Cola, Xianfan Xu, and T.S. Fisher, *Increased real contact in thermal interfaces: A carbon nanotube/foil material.* APPLIED PHYSICS LETTERS, 2007. **90**.
110. Xu, J. and T.S. Fisher. *Enhanced thermal contact conductance using carbon nanotube array interfaces*. in *Components and Packaging Technologies*. 2006 IEEE
111. Tong;, T., et al. *Dense Vertically Aligned Multiwalled Carbon Nanotube Arrays as Thermal Interface Materials*. in *Components and Packaging Technologies*. 2007 IEEE.
112. Yang Chai, et al. *Carbon Nanotube/Copper Composites for Via Filling and Thermal Management*. in *Electronic Components and Technology conference*. 2007: IEEE.

113. Chuang, H.F., et al., *Improvement of Thermal Contact Resistance by Carbon Nanotubes and Nanofibers.* Nanoscience and Nanotechnology, 2004. **4** (8): p. 964-967.
114. Tong, T., et al., *Multiwalled Carbon Nanotube/Nanofiber Arrays as Conductive and Dry Adhesive Interface Materials.* ASME Conference Proceedings, 2004. **2004**(41774): p. 7-12.
115. Amama, P.B., et al., *Dendrimer-assisted controlled growth of carbon nanotubes for enhanced thermal interface conductance.* Nanotechnology, 2007. **18**.
116. Tong, T., et al. *Dense Vertically Aligned Multiwalled Carbon Nanotube Arrays as Thermal Interface Materials*. in *Components and Packaging Technologies*. 2007 IEEE.
117. Ajayan, P.M. and O.Z. Zhou, *Applications of Carbon Nanotubes.* Topics in Applied Physics, 2001. **80**: p. 391-425.
118. B. I. Yakobson, C.J. Brabec, and J. Bernholc, *Nanomechanics of Carbon Tubes: Instabilities beyond Linear Response.* PHYSICAL REVIEW LETTERS, 1996. **76**: p. 2511-2514.
119. Rodney Andrews, et al., *Multiwall Carbon Nanotubes: Synthesis and Application.* Accounts of chemical research, 2002. **35**: p. 1008-1017.
120. M.S. Dresselhaus, G. Dresselhaus, and A. Jorio, *Unsual Properties and Structure of Carbon Nanotubes.* Annual Review of Materials Research, 2004. **34**: p. 247-278
121. Cola, B.A., *Photoacoustic characterization and optimization of carbon nanotube array thermal interfaces*. 2008, Purdue University.
122. Ajayan, P.M., *Nanotubes from Carbon.* Chemical Reviews, 1999: p. 1787-1799.
123. M. R. Falvo, et al., *Bending and buckling of carbon nanotubes under large strain.* Nature, 1997. **389**: p. 582-584
124. Reich, S. and C. Thomsen, *Elastic properties of carbon nanotubes under hydrostatic pressure.* PHYSICAL REVIEW B, 2002. **65**: p. 65.
125. Chiara Daraio, V.F. Nesterenko, and S. Jin, *Highly nonlinear contact interaction and dynamic energy dissipation by forest of carbon nanotubes.* Applied physics letters, 2004. **85**: p. 5724-5726.
126. Chiara Daraio, et al., *Impact response by a foamlike forest of coiled carbon nanotubes.* JOURNAL OF APPLIED PHYSICS, 2006. **100**.
127. S.Dj. Mesarovic, et al., *Mechanical behavior of a carbon nanotube turf.* Scripta Materialia, 2007. **56**: p. 157–160.

128. H.J. Qi, et al., *Determination of mechanical properties of carbon nanotubes and vertically aligned carbon nanotube forests using nanoindentation.* Journal of the Mechanics and Physics of Solids, 2003. **51**: p. 2213 – 2237.
129. J. Suhr, et al., *Fatigue resistance of aligned carbon nanotube arrays under cyclic compression.* Nature Nanotechnology, 2007. **2**: p. 417 - 421
130. Anyuan Cao, et al., *Super-Compressible Foamlike Carbon Nanotube Films.* SCIENCE, 2005. **310**: p. 1307 - 1310.
131. Lourie, O. and H.D. Wagner, *Transmission electron microscopy observations of fracture of single-wall carbon nanotubes under axial tension.* Applied physics letters, 1998. **73**: p. 3527 - 3529.
132. Arif A. Mamedov, et al., *Molecular design of strong single-wall carbon nanotube/polyelectrolyte multilayer composites.* Nature Materials, 2002. **1**: p. 190 - 194.
133. C. Bower, et al., *Deformation of carbon nanotubes in nanotube–polymer composites.* APPLIED PHYSICS LETTERS, 1999. **74**: p. 3317 - 3319.
134. Chenyu Wei, Deepak Srivastava, and K. Cho, *Thermal Expansion and Diffusion Coefficients of Carbon Nanotube-Polymer Composites.* Nano letters, 2002. **2**: p. 647–650.
135. D. Qian, et al., *Load transfer and deformation mechanisms in carbon nanotube-polystyrene composites.* APPLIED PHYSICS LETTERS, 2000. **76**: p. 2868 - 2870.
136. Deepak Srivastava, C. Wei, and K. Cho, *Nanomechanics of carbon nanotubes and composites.* Applied mechanics reviews, 2003. **56**: p. 215 - 230.
137. Florian H. Gojny, et al., *Surface modified multi-walled carbon nanotubes in CNT/epoxy-composites.* Chemical Physics Letters, 2003. **370**: p. 820 – 824.
138. H. D. Wagner, et al., *Stress-induced fragmentation of multiwall carbon nanotubes in a polymer matrix.* Applied physics letters, 1998. **72**: p. 188 - 190.
139. M. Cadek, et al., *Morphological and mechanical properties of carbon-nanotube-reinforced.* APPLIED PHYSICS LETTERS, 2002. **81**: p. 5123 - 5125.
140. Harris, P.J.F., *Carbon Nanotube Composites.* International Materials Reviews, 2004. **49**: p. 31-43.
141. Watts, P.C.P. and W.K. Hsu, *Behaviours of embedded carbon nanotubes during film cracking.* Nanotechnology, 2003. **14**: p. L7 – L10.
142. P. M. Ajayan, et al., *Single-Walled Carbon Nanotube–Polymer Composites: Strength and Weakness.* Advanced materials, 2000. **12**: p. 750–753.

143. Xiaojing Xu, et al., *Mechanical properties and interfacial characteristics of carbon-nanotube-reinforced epoxy thin films.* APPLIED PHYSICS LETTERS, 2002. **81**: p. 2833 - 2835.

144. Du, A.J. and S.C. Smith, *Van der Waals-corrected density functional theory: benchmarking for hydrogen–nanotube and nanotube–nanotube interactions.* Nanotechnology, 2005. **16**(10): p. 2118.

145. Edwin H. T. Teo, et al., *A Carbon Nanomattress: A New Nanosystem with Intrinsic, Tunable, Damping Properties.* Advanced Materials, 2007. **19**: p. 2941–2945.

146. Jing Sun, L. Gao, and X. Jin, *Reinforcement of alumina matrix with multi-walled carbon nanotubes.* Ceramics International, 2005. **31**: p. 893-896

147. S. Chang, et al., *Processing and mechanical properties of c-nanotube reinforced alumina composites.* Ceramic Engineering and Science Proceedings 2000. **21**: p. 653-658.

148. A. V. Melechko, et al., *Vertically aligned carbon nanofibers and related structures: Controlled synthesis and directed assembly.* Journal of Applied Physics 2005. **97**: p. 041301-39

149. Y. Wu, et al., *The carbon nanotube based nanocomposite with enhanced thermal conductivity.* Solid State Phenomena (Volumes 121 - 123), 2007. **Nanoscience and Technology**: p. 243-246.

150. Bojan O. Boskovic, et al., *Large-area synthesis of carbon nanofibres at room temperature.* 2002. **1**: p. 165 - 168

151. S. Hofmann, et al., *Low-temperature plasma enhanced chemical vapour deposition of carbon.* Diamond and Related Materials, 2003.

152. Placidus B. Amama, et al., *Dendrimer-assisted low-temperature growth of carbon nanotubes by plasma-enhanced chemical vapor deposition.* The Royal Society of Chemistry, 2006: p. 2899–2901.

153. Chiang, J.-C., *Design and characterization of nanowire array as thermal interface material for electronics packaging*. December 2008, Mechanical Engineering, Texas A&M University.

154. Mirmira, S.R., E.E. Marotta, and L.S. Fletcher, *Thermal contact conductance of adhesives for microelectronic systems.* Journal of thermophysics and heat transfer 1997: p. 141-145.

155. Prasher, R.S. and J.C.C. Matayabas, *Thermal Contact Resistance of Cured Gel Polymeric Thermal Interface Material.* IEEE Transactions on components and packaging technologies, 2004. **27**: p. 702-709.
156. Vijay Wakharkar, et al., *Materials Technologies for Thermomechanical Management of Organic Substrates.* Intel Journal Technology, 2005. **09**(04): p. 309-323.
157. Lau, J., S. Erasmus, and S. Pan. *Effects of voids on bump chip carrier (BCC++) solder joint reliability*. in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*. 2002.
158. Dasgupta, A., P. Sharma, and K. Upadhyayula, *Micro-Mechanics of Fatigue Damage in Pb-Sn Solder Due to Vibration and Thermal Cycling.* International Journal of Damage Mechanics, 2001. **10**(2): p. 101-132.
159. Engelmaier, W., *Surface Mount Solder Joint Reliability: Issues, Design, Testing, Prediction*, in *Workshop Notes,* 1995, Engelmaier Associates, Inc.: Mendham, NJ.
160. Y.C. Chan, D.J. Xie, and J.K.L. Lai, *Experimental studies of pore formation in surface mount solder joints.* Materials Science and Engineering: B, 1996. **38**(1-2): p. 53–61.
161. *CBS News*. 2000.
162. Mei, Z., et al. *Kirkendall voids at Cu/solder interface and their effects on solder joint reliability*. in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*. 2005.
163. M. Montano, et al. *Novel Process Techniques To Reduce Voids in Solder Thermal Interface Materials Used for Flip-Chip Package Applications*. in *Summer Heat Transfer Conference*. 2005: ASME.
164. Yerman, A., et al., *Hot Spots Caused by Voids and Cracks in the Chip Mountdown Medium in Power Semiconductor Packaging.* IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 1983 **6**: p. 473 - 479
165. A. A. Primavera, et al. *Factors that affect void formation in bga assembly*. in *Proceedings of the Surface Mount Technology Association*. 1998.
166. A. Primavera, et al., *Factors that Affect Void Formation in BGA Assemblies.* Journal of Surface Mount Technology, 1999. **12**(1).
167. Lee, N.C., *Reflow Processing and troubleshooting SMT, BGA, CSP and Flip chip technologies*. 2002, U.S.A: Newnes Publication.
168. Lee, N.-C. (2005) *How to Control Voiding in Reflow Soldering*. Chip Scale Review.

169. J. Lau, et al., *Electronics Manufacturing with Lead-free, Halogen-free, and Conductive Adhesive Materials*. 2002, New York: McGraw Hill.
170. IPC, *Acceptability of Electronic Assemblies*, in *IPC-A-610C*. 2000.
171. IPC, *Design and Assembly Process Implementation for BGAs*, in *IPC-7095*. 2000.
172. *Military Standard Test Methods and Procedures for Microelectronics*, in *Mil-Std-883D Method 2030* 1993, Department of Defense.
173. Leila Ladani, A.D., *Effect of voids on thermomechanical durability of Pb-free BGA solder joints : Modeling and simulation.* Journal of electronic packaging, 2007 **129**(3): p. 273-277
174. Ladani, L.J. and A. Dasgupta, *Damage Initiation and Propagation in Voided Joints: Modeling and Experiment.* Journal of electronic packaging, 2008. **130**(1): p. 011008.
175. Ladani, L.J. and J. Razmi, *Interaction Effect of Voids and Standoff Height on Thermomechanical Durability of BGA Solder Joints.* Device and Materials Reliability, IEEE Transactions on, 2009. **9**(3): p. 348-355.
176. Yunus, M., et al., *Effect of voids on the reliability of BGA/CSP solder joints.* Microelectronics Reliability, 2003. **43**(12): p. 2077-2086.
177. Dudek, M.A., et al., *Three-dimensional (3D) visualization of reflow porosity and modeling of deformation in Pb-free solder joints.* Materials Characterization, 2010. **61**(4): p. 433-439.
178. Yu, Q., et al., *Effect of process-induced voids on isothermal fatigue resistance of CSP lead-free solder joints.* Microelectronics Reliability, 2008. **48**(3): p. 431-437.
179. Zhou, B. and B. Qiu. *Effect of Voids on the Thermal Fatigue Reliability of PBGA Solder Joints through Submodel Technology*. in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*. 2008.
180. Terasaki, T. and H. Tanie. *Fatigue crack propagation analysis for microsolder joints with void*. in *Electronics Materials and Packaging, 2005. EMAP 2005. International Symposium on*. 2005.
181. Junling Chang, D.J., W. Kempe and Xiaoming Xie, *Degradation of Sn-Ag-Cu heat-sink attachment during thermal shock cycling.* Soldering & Surface Mount Technology, 2005. **17**(4): p. 10-16.
182. M. Gonzalez, B.V., Jan Vanfleteren and D. Manessis, *Thermo-Mechanical FEM Analysis of Lead Free and Lead Containing Solder for Flip Chip Applications*, in *EMPC*. 2005: Brugge, Belgium. p. 440 - 445.

183. Zhu, W.H., et al. *Comparative study on solder joint reliability using different FE-models*. in *Electronics Packaging Technology, 2003 5th Conference (EPTC 2003)*. 2003.

184. Laxmidhar Biswal, Arvind Krishna, and D. Sprunger. *Effect of Solder Voids on Thermal Performance of a High Power Electronic Module*. in *Electronics Packaging Technology Conference* 2005: IEEE.

185. N. Zhu. *Thermal Impact of Solder Voids in the Electronic Packaging of Power Devices*. in *Semiconductor Thermal Measurement and Management Symposium*. 2002: IEEE.

186. Chiriac, V.A. and Y. Youmin. *Impacts of solder voids on PQFN packages' thermal and mechanical performances*. in *Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2010 12th IEEE Intersociety Conference on*. 2010.

187. K. Zeng and K.N. Tu, *Six Cases of Reliability Study of Pb-free Solder Joints in Electronic Packaging Technology.* Materials Science and Engineering, 2002. **38**: p. 55-105.

188. Ladani, L. and A. Dasgupta, *Effect of voids on thermomechanical durability of Pb-free BGA solder joints : Modeling and simulation.* Journal of electronic packaging, 2007 **129**(3): p. 273-277

189. Lai Zheng, B., et al. *Mechanics of Sn-4Ag-0.5Cu solder joints in a ball grid array assembly during reflow and temperature cycles*. in *Electronic Manufacturing Technology Symposium (IEMT), 2008 33rd IEEE/CPMT International*. 2008.

190. Zahn, B.A. *Impact of ball via configurations on solder joint reliability in tape-based, chip-scale packages*. in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*. 2002.

191. Padilla, E., et al., *Quantifying the effect of porosity on the evolution of deformation and damage in Sn-based solder joints by X-ray microtomography and microstructure-based finite element modeling.* Acta Materialia, 2012. **60**(9): p. 4017-4026.

192. Jiang, L., et al., *Three-dimensional (3D) microstructural characterization and quantification of reflow porosity in Sn-rich alloy/copper joints by X-ray tomography.* Materials Characterization, 2011. **62**(10): p. 970-975.

193. Kouznetsova, V., W.A.M. Brekelmans, and F.P.T. Baaijens, *An approach to micro-macro modeling of heterogeneous materials.* Computational Mechanics, 2001. **27**(1): p. 37-48.

194. Okereke, M.I. and A.I. Akpoyomare, *A virtual framework for prediction of full-field elastic response of unidirectional composites.* Computational Materials Science, 2013. **70**(0): p. 82-99.
195. Okereke, M.I., *Prediction of Finite Deformation of ThermoplasticMatrix Composites*, in *Solid Mechanics andMaterials Engineering Group, Department of Engineering Science,* 2009, University of Oxford.
196. Melro, A.R., P.P. Camanho, and S.T. Pinho, *Generation of random distribution of fibres in long-fibre reinforced composites.* Composites Science and Technology, 2008. **68**(9): p. 2092-2102.
197. Metropolis, N., *The beginning of the Monte Carlo method.* Los Alamos Science, 1987(Special Issue dedicated to Stanisław Ulam): p. 125–130.
198. Anderson, H.L., *Metropolis, Monte Carlo and the MANIAC.* Los Alamos Science, 1986. **14**: p. 96–108.
199. Buryachenko, V.A., et al., *Quantitative description and numerical simulation of random microstructures of composites and their effective elastic moduli.* International Journal of Solids and Structures, 2003. **40**(1): p. 47-72.
200. Garofalo, F., *Fundamentals of Creep and Creep-Rupture in Metals*. 1966: The Macmillan Company
201. Cadek, J., *Creep in metallic materials*. 1988: Elsevier Science Publisher.
202. Hertzberg, R.W., *Deformation and Fracture Mechanics of Engineering Materials*. 4th edition ed. 1996: John Wiley & Sons Inc.
203. Lau, J.H., *Creep of 96.5Sn3.5Ag Solder Interconnects.* Soldering & Surface Mount Technology, 1993. **5**(3): p. 45 - 52.
204. *ANSYS 10.0 Reference Manual*.
205. Anand, L., *Constitutive equations for hot-working of metals.* International Journal of Plasticity, 1985. **1**(3): p. 213-231.
206. Brown, S.B., K.H. Kim, and L. Anand, *An internal variable constitutive model for hot working of metals.* International Journal of Plasticity, 1989. **5**(2): p. 95-130.
207. Yeo, A., C. Lee, and J.H.L. Pang, *Flip chip solder joint reliability analysis using viscoplastic and elastic-plastic-creep constitutive models.* Components and Packaging Technologies, IEEE Transactions on, 2006. **29**(2): p. 355-363.
208. Schubert, A., et al. *Experimental and numerical reliability investigations of FCOB assemblies with process-induced defects*. in *Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th*. 2000.

209. *Solder Joint Failures*. [cited 2012 16/10]; Available from: http://www.siliconfareast.com/solder-joint-failures.htm.
210. Terashima, S., et al., *Effect of silver content on thermal fatigue life of Sn-xAg-0.5Cu flip-chip interconnects.* Journal of Electronic Materials, 2003. **32**(12): p. 1527-1533.
211. Otiaba, K.C., et al., *Numerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device.* Microelectronics Reliability, (0).
212. Kariya, Y., et al., *Effect of silver content on the shear fatigue properties of Sn-Ag-Cu flip-chip interconnects.* Journal of Electronic Materials, 2004. **33**(4): p. 321-328.
213. Mustafa, M., et al. *The effects of aging on the cyclic stress-strain behavior and hysteresis loop evolution of lead free solders*. in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*. 2011.
214. Collins, M.N., et al., *Thermal Fatigue and Failure Analysis of SnAgCu Solder Alloys With Minor Pb Additions.* Components, Packaging and Manufacturing Technology, IEEE Transactions on, 2011. **1**(10): p. 1594-1600.
215. Xueyou, Y. and L. Guoyuan. *Study of thermal fatigue lifetime of fan-in package on package (FiPoP) by finite element analysis*. in *Electronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP '09. International Conference on*. 2009.
216. Heather McCormick, P.S., Craig Hamilton, Zohreh Bagheri, and Simin Bagheri *THE Great SAC Debate: Comparing the reliability of SAC305 and SAC405 solders in a variety of applications*, in *Pan Pacific Symposium* 2007.
217. Polina Snugovsky, Z.B., Heather McCormic, *Failure mechanism of SAC 305 and SAC 405 in harsh environments and influence of board defects including black pad.* Journal of SMT Article, 2007. **20-3**.
218. Luke Garner, S.S., Daewoong Suh, Tiffany Byrne, Ashay Dani, Ted Martin, Michael Mello, Mitesh Patel and Richard Williams, *Finding Solutions to the Challenges in Package Interconnect Reliability.* Intel Technology Journal, 2005. **09**(04): p. 297-308.
219. Kittidacha, W., A. Kanjanavikat, and K. Vattananiyom. *Effect of SAC Alloy Composition on Drop and Temp cycle Reliability of BGA with NiAu Pad Finish*. in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*. 2008.
220. Birzer, C., et al. *Drop test reliability improvement of lead-free fine pitch BGA using different solder ball composition*. in *Electronic Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th*. 2005.

221. Zhao, X.J., et al. *Improvement of mechanical impact resistance of BGA packages with Pb-free solder bumps*. in *Electronics Packaging Technology Conference, 2006. EPTC '06. 8th*. 2006.

222. JEIDA (2000) *Challenges and Efforts Toward Commercialization of Lead-free Solder - Road Map 2000 for Commercialization of Lead-free Solder - ver 1.3*

223. NEMI, *National Electronics Manufacturing Initiative, News Release*. 2007.

224. Xingsheng, L. and L. Guo-Quan, *Effects of solder joint shape and height on thermal fatigue lifetime.* Components and Packaging Technologies, IEEE Transactions on, 2003. **26**(2): p. 455-465.

225. JEDEC, *Temperature Cycling*, in *JESD22-A104D*. 2009, JEDEC Solid state technology association.

226. Shi, X.Q., et al., *A New Creep Constitutive Model for Eutectic Solder Alloy.* Journal of Electronic Packaging, 2002. **124**(2): p. 85-90.

227. Lakhkar, N.R., *Effect of structural design parameters on wafer level csp ball shear strength and their influence on accelerated thermal cycling reliability*. 2010, The University of Texas at Arlington.

228. Tunga, K. and S.K. Sitaraman, *Predictive Model Development for Life Prediction of PBGA Packages With SnAgCu Solder Joints.* Components and Packaging Technologies, IEEE Transactions on, 2010. **33**(1): p. 84-97.

229. Wang, Q., et al. *Experimental Determination and Modification of Anand Model Constants for Pb-Free Material 95.5Sn4.0Ag0.5Cu*. in *Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, 2007. EuroSime 2007. International Conference on*. 2007.

230. Lee, W.W., L.T. Nguyen, and G.S. Selvaduray, *Solder joint fatigue models: review and applicability to chip scale packages.* Microelectronics Reliability, 2000. **40**(2): p. 231-244.

231. Müller-Fiedler, R. and V. Knoblauch, *Reliability aspects of microsensors and micromechatronic actuators for automotive applications.* Microelectronics Reliability, 2003. **43**(7): p. 1085-1097.

232. Johnson, R.W., et al., *The changing automotive environment: high-temperature electronics.* Electronics Packaging Manufacturing, IEEE Transactions on, 2004. **27**(3): p. 164-176.

233. An, T. and F. Qin, *Intergranular cracking simulation of the intermetallic compound layer in solder joints.* Computational Materials Science, 2013. **79**(0): p. 1-14.

234. Sarihan, V., *Temperature Dependent Viscoplastic Simulation of Controlled Collapse Solder Joint Under Thermal Cycling.* Journal of Electronic Packaging, 1993. **115**(1): p. 16-21.
235. Lau, J.H., *Flip chip technologies*. 1996, New York: McGraw-Hill.
236. Stinson-Bagby, K., *Microstructural Evolution in Thermally Cycled Large-Area Lead and Lead-Free Solder Joints*, in *Materials Science and Engineering*. 2002, Virginia Polytechnic Institute and State University: Blacksburg, Virginia.
237. Darveaux, R., *Effect of Simulation Methodology on Solder Joint Crack Growth Correlation and Fatigue Life Prediction.* Journal of Electronic Packaging, 2002. **124**(3): p. 147-154.
238. Hun Shen, N., et al. *Absolute and relative fatigue life prediction methodology for virtual qualification and design enhancement of lead-free BGA*. in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*. 2005.
239. Syed, A. *Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints*. in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*. 2004.
240. Reinikainen, T.O., P. Marjamaki, and J.K. Kivilahti. *Deformation characteristics and microstructural evolution of SnAgCu solder joints*. in *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, 2005. EuroSimE 2005. Proceedings of the 6th International Conference on*. 2005.
241. Schubert, A., et al. *Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation*. in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*. 2003.
242. Wiese, S., E. Meusel, and K.J. Wolter. *Microstructural dependence of constitutive properties of eutectic SnAg and SnAgCu solders*. in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*. 2003.
243. Zhang, Q., *Isothermal mechanical and thermo-mechanical durability characterization of selected pb-free solders*, in *Mechanical Engineering*. 2004, University of Maryland, College Park.
244. Qian, Z., A. Dasgupta, and P. Haswell. *Viscoplastic constitutive properties and energy-partitioning model of lead-free Sn3.9Ag0.6Cu solder alloy*. in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*. 2003.

245. Ladani, L.J., *Damage Initiation and Evolution in Voided and Unvoided Lead Free Solder Joints Under Cyclic Thermo-Mechanical Loading*, in *Mechanical Engineering*. 2007, University of Maryland.

246. Ladani, L.J., *Reliability Estimation for Large-Area Solder Joints Using Explicit Modeling of Damage.* Device and Materials Reliability, IEEE Transactions on, 2008. **8**(2): p. 375-386.

247. Topline. *Test Die, Daisy Chain & Isolated Pads, Experimental use in Lab, Variety of Applications*. [cited 2012 15 November]; Available from: http://www.topline.tv/Die_Test.html.

248. Chang, R.W. and F. Patrick McCluskey, *Reliability assessment of indium solder for low temperature electronic packaging.* Cryogenics, 2009. **49**(11): p. 630-634.

249. Lehman, L.P., et al. *Microstructure and Damage Evolution in Sn-Ag-Cu Solder Joints*. in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*. 2005.

250. S.T. Nurmi, et al., *The influence of multiple reflow cycles on solder joint voids for lead-free PBGAs.* Soldering & Surface Mount Technology, 2003. **15**(1): p. 31 - 38.

251. Walter D. Pilkey and D.F. Pilkey, *Peterson's Stress Concentration Factors*. 1997, New York: Wiley-Interscience.

252. Otiaba, K.C., et al., *Finite element analysis of the effect of silver content for Sn–Ag–Cu alloy compositions on thermal cycling reliability of solder die attach.* Engineering Failure Analysis, 2013. **28**(0): p. 192-207.

253. Pucha, R., J. Pyland, and S.K. Sitaraman, *Damage Metric-Based Mapping Approaches for Developing Accelerated Thermal Cycling Guidelines for Electronic Packages.* International Journal of Damage Mechanics, 2001. **10**(3): p. 214-234.

254. Carlson, R.O., et al. *Voids, Cracks, and Hot Spots in Die Attach*. in *Reliability Physics Symposium*. 1983: IEEE.

255. C.J. Reimer, et al., *A simulation study of IC layout effects on thermal management of die attached GaAs ICs.* IEEE Transactions on Components and Packaging Technologies, 2000. **23**: p. 341 - 351.

256. Liu, C., et al. *Thermal impact of randomly distributed solder voids on Rth-JC of MOSFETs*. in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*. 2008.

257. Sinnadurai, F.N., *Handbook of Microelectronics Packaging and Interconnection Technologies*. 1985, Scotland: Electrochemical Publications Limited.

258. Wiese, S. and K.J. Wolter, *Microstructure and creep behaviour of eutectic SnAg and SnAgCu solders.* Microelectronics Reliability, 2004. **44**(12): p. 1923-1931.
259. Kang, S.K., et al., *Microstructure and mechanical properties of lead-free solders and solder joints used in microelectronic applications.* IBM Journal of Research and Development, 2005. **49**(4.5): p. 607-620.
260. Corporation, I. *Thermal Interface Materials*. [cited 2012 9 February]; Available from: http://www.indium.com/TIM/.
261. JEDEC, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components*. 2005, JEDEC Solid state technology association.
262. *Indium thermal interface material development for microprocessors*. in *Semiconductor Thermal Measurement and Management Symposium*. 2009
263. Department of Defense, *Test method standard semiconductor devices*.
264. Lee, N.-C. (2005) *How to Control Voiding in Reflow Soldering*. Chips Scale Review.
265. Xu, D.-X., et al., *Experimental Wettability Study of Lead-Free Solder on Cu Substrates Using Varying Flux and Temperature.* Journal of Electronic Materials, 2008. **37**(1): p. 125-133.
266. Vaynman, S. and M.E. Fine, *Flux Development for Lead-Free Solders Containing Zinc.* Journal of Electronic materials, 2000. **29**(10): p. 1160-1163.
267. Pang, J.H.L., et al., *Thermal cycling aging effects on Sn–Ag–Cu solder joint microstructure, IMC and strength.* Thin Solid Films, 2004. **462–463**(0): p. 370-375.
268. Chang, R.W., *Influence of cryogenic temperature and microstructure on fatigue failure of indium solder joint*, in *Department of Mechanical Engineering*. 2008, University of Maryland.
269. Peng, W., *An Investigation of Reliability of High Density Electronic Package-to-Board Interconnections from the Perspective of Solder Joint Metallurgy*, in *Department of Electronics, Electronics Integration and Reliability*. 2010, Aalto University School of Science and Technology: Finland.
270. Fouassier, O., et al., *Microstructural evolution and mechanical properties of SnAgCu alloys.* Journal of Applied Physics, 2006. **100**(4).
271. Long, X., et al., *Deformation Behavior of Sn-3.8Ag-0.7Cu Solder at Intermediate Strain Rates: Effect of Microstructure and Test Conditions.* Journal of Electronic Materials, 2008. **37**: p. 189 - 200.

272. Hongtao, M., et al. *The Influence of Elevated Temperature Aging on Reliability of Lead Free Solder Joints*. in *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*. 2007.

273. Ding, F., *Flip chip and lid attachment assembly process development*. 2006, Auburn University.

274. Oliver, J.R., J. Liu, and Z. Lai. *Effect of thermal ageing on the shear strength of lead-free solder joints*. in *Advanced Packaging Materials: Processes, Properties andInterfaces, 2000. Proceedings. International Symposium on*. 2000.

275. Zhu, H.-y., et al., *Influence of voids on interlaminar shear strength of carbon/epoxy fabric laminates.* Transactions of Nonferrous Metals Society of China, 2009. **19, Supplement 2**(0): p. s470-s475.

276. Hernández, S., et al., *Effect of curing cycle on void distribution and interlaminar shear strength in polymer-matrix composites.* Composites Science and Technology, 2011. **71**(10): p. 1331-1341.

277. Yoon, J.-W., et al., *Effects of isothermal aging and temperature–humidity treatment of substrate on joint reliability of Sn–3.0Ag–0.5Cu/OSP-finished Cu CSP solder joint.* Microelectronics Reliability, 2008. **48**(11–12): p. 1864-1874.

278. Huang, H. and R. Talreja, *Effects of void geometry on elastic properties of unidirectional fiber reinforced composites.* Composites Science and Technology, 2005. **65**(13): p. 1964-1981.

# Appendices

**MATLAB Code used to implement MCRVEGen algorithm**

```
%% MonteCarlo 2D RVE Generator (Circles only)
%Author: Paul Buckley, Michael Okereke & Kenny Otiaba
%About:  Generates random placement of circles in a square RVE
%-------------------------------------------------------------------------
%Added Features
%       1. Incorporates Trimming of Inclusions Algorithm (v2)
%       2. Includes script creation for ANSYS Models
%-------------------------------------------------------------------------

%%
*************************************************************************
%Prepare workspace
    clc, clear; close all; format long

%% Begin to time operation
    tic

%%
*************************************************************************
%% Monte Carlo Computation Options
    Xrange          = 2.5;        % RVE X-axis Length
    Yrange          = 2.5;        % RVE Y-axis Length
    Diam            = 0.05;       % Diameter of Fibrous reinforcement
    Volfraction     = 0.02;      % Desired Volume Fraction
    PeriodMat       = 0;         % 0-Allow Surface Voids, 1-do not
    intVoiding      = 0;         % 0 - Internal Voids only, 1 - Allow any
void type
    percIntVoiding  = 10;        % Percentage of Radius to allow between
nearest boundary and inclusion diameter
    NOP             = 1000;      % Number of points/divisions of the circle
    reviseRVESize   = 0;         % 0 - Do not, 1 - revise RVE Size
    strSize         = 20;        % Number of Decimal places for printed
numbers (for Scripts)
    switchOffRVE    = 1;         % 0 - Do not print RVE Window, 1 - Print
RVE

%% ************************************************************************
%% Options for Creating ANSYS RVE BASED ON MONTE-CARLO ALGORITHM
   ansRVEScript     = 2;        %0 - Create MonteCarlo 2D RVE Plot WITHOUT
printing ANSYS JScript
                               %1 - Create MonteCarlo 2D RVE Plot AND
REQUIRED ANSYS JScript
   ansTrimBFibres   = 0;        %0 - Trim Boundary Fibres; 1 - do not

%% BEGIN COMPUTATION
%% ************************************************************************
disp('*****************************************************');
disp('Welcome to the Monte Carlo 2D RVE Generator for ANSYS  ');
disp('      Authors:  CPBuckley, MIOkereke & KOtiaba         ');
disp(['      Date:      ', num2str(date)]                          );
disp('*****************************************************');

%% Based on Computation Option Create Required RVE
for calcNumberOfCircles = 1:1
    R = 0.5*Diam; % Radius of Inclusion
    N=round(Volfraction*Xrange*Yrange/(pi*R^2));
    if N<1
```

```
        'Too few circles - abort';
    end

    % Revise calculation to determine exact volfraction to allow
    % for rounded integer (new) calculated number of inclusions,N
    if reviseRVESize == 0
        Volfraction =N*pi*R^2/(Xrange*Yrange);
    elseif reviseRVESize == 1 %Revise RVE Now
        Lrve=sqrt(N*pi*R^2/(Volfraction));
        Xrange = Lrve;
        Yrange = Lrve;
    end
    if Volfraction>0.9
        'Too many circles - abort';
        stop;
    end
end


%% Define FileName for saving all results
    for filesIDs = 1:1
        %Make Directory
            if N <=9
                if Xrange == Yrange
                    dirname =
['RVE0',num2str(N),'Voids_Size_',num2str(round(Xrange)),'Squared'];
                else
                    dirname =
['RVE0',num2str(N),'Voids_Size_',num2str(round(Xrange)),'Rectangle'];
                end
            else
                if Xrange == Yrange
                    dirname =
['RVE',num2str(N),'Voids_Size_',num2str(round(Xrange)),'Squared'];
                else
                    dirname =
['RVE',num2str(N),'Voids_Size_',num2str(round(Xrange)),'Rectangle'];
                end
            end
            lenDir = length(dir([dirname,'_*']));
            if isdir(dirname) ~=1 && lenDir == 0
                dirName = [dirname,'/',dirname,'_01'];
                rezLocation = mkdir(dirName);
            else
                cd(dirname)
                lenDir = length(dir([dirname,'_*']));
                cd ..
                if lenDir <9
                    dirName = [dirname,'/',dirname,'_0',num2str(lenDir+1)];
                else
                    dirName = [dirname,'/',dirname,'_',num2str(lenDir+1)];
                end
                rezLocation = mkdir(dirName);
            end

        %Create FileName
        fileName = [dirName,'/RVE2D_',num2str(N),'Voidss'];
    end

%% CHOOSE TO CREATE OR NOT CREATE ANSYS SCRIPT
```

```
    if ansRVEScript == 1
        %Simply generate RVEs (using the Monte Carlo Process)
        ansRVEGenerate
    elseif ansRVEScript == 0
        %Print ANSYS RVE-Generating Script
        ansPrintAnsysRVEScript
    elseif ansRVEScript == 2
        %Create MC RVE
        ansRVEGenerate
        %Print ANSYS script to go with it
        if intVoiding == 0 %Only if you DO NOT HAVE boundary inclusions
            ansTrimBFibres = 1; % Enforce No trimming of fibres
            ansPrintAnsysRVEScript
        end
    end

%% Save Datasets
        cd(dirName)
        save('DataSets','XY','XYAll','Xrange','Yrange', 'N',
'Volfraction','Diam','R');
        cd ../../

%% Trim Boundary Fibres
        if ansTrimBFibres == 0 && intVoiding == 1 % Do this only if YOU
HAVE boundary inclusions
            ansTrim_Boundary_Fibres
            ansPrintAnsysRVEScript
        end

%% End Timing of Algorithm events
        eventTime = toc;
        disp(['Total Duration for RVE creation  = ', num2str(eventTime), '
seconds'])

%% ************************************************************************
%% ************************************************************************
```

**ANSYS scripts used in calculating accumulated plastic work in the solder joints**

```
! CALC AVG PLASTIC WORK FOR CYCLE 1
set,4,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable wavg1=sumplwk/sumvolu
! CALC AVG PLASTIC WORK FOR CYCLE 2
set,8,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg2=sumplwk/sumvolu
! CALC AVG PLASTIC WORK FOR CYCLE 3
set,12,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
Wavg3=sumplwk/sumvolu! CALC AVG PLASTIC WORK FOR CYCLE 4
```

```
set,16,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
Wavg4=sumplwk/sumvolu
! CALC DELTA AVG PLASTIC WORK
Dwavg1=wavg2-wavg1
Dwavg2=wavg3-wavg2
Dwavg3=wavg4-wavg3
```