MODELLING OF THE RELIABILITY OF FLIP CHIP LEAD-FREE SOLDER JOINTS AT HIGH-TEMPERATURE EXCURSIONS

EMEKA HYGINUS AMALU

DOCTOR OF PHILOSOPHY

2012

MODELLING OF THE RELIABILITY OF FLIP CHIP LEAD-FREE SOLDER JOINTS AT HIGH-TEMPERATURE EXCURSIONS

Emeka Hyginus Amalu

BEng (Hons), MEng

Electronics Manufacturing Engineering Research Group (EMERG)

Department of Engineering Systems

School of Engineering at Medway

University of Greenwich

London, UK



A thesis submitted in partial fulfilment of the requirements of the University of Greenwich for the Degree of Doctor of Philosophy

March 2012

DECLARATION

I certify that this work has not been accepted in substance for any degree, and is not concurrently being submitted for any degree other than that of Doctor of Philosophy (Ph.D.) being studied at the University of Greenwich. I also declare that this work is the result of my own investigations except where otherwise identified by references and that I have not plagiarised the work of others.

Emeka Hyginus Amalu

(student)

Date

Professor Nnamdi N. Ekere

(Supervisor)

Date

ACKNOWLEDGEMENTS

Many individuals and corporate bodies have contributed towards my academic development. Perhaps I should start with my supervisor. I am extremely indebted to my supervisor, Professor Ndy Ekere, who has guided me throughout the duration of this study. His unparalleled supervision is second to none and has yielded the desired result necessary to bring this work to fruition. The contributions of the researcher's second supervisor, Dr. Raj Bhatti, are much appreciated as they have improved immensely the quality of the research reported in this thesis.

It is my pleasure to acknowledge the unquantifiable supports I received from the personal assistants of my supervisor. The aids of Mrs. Nicola Cox and Mrs Sharon Woods were excellent. The support staff of Engineering Systems and School of Engineering provided assistances throughout the duration of this research. The investigator is hugely grateful to them – especially Mr. Ian Cakebread, Mr. V. W. Cosgrave and Mr. Tony Kelly.

The investigator thanks Mr. Galadima Aminu of Petroleum technology Development Fund (PTDF), Abuja Nigeria, for his support and encouragement.

I can never thank you enough - my late beloved mother - Anna Udechukwu Ozormalu - for all your sacrifices, undying support and encouragements in all my life endeavours. I am not sure why I deserved such a great rare privilege; however, I will be eternally grateful to you.

The acknowledgement cannot be complete if Petroleum Technology Development Fund (PTDF) Nigeria and School of Engineering, University of Greenwich are not recognised for provision of fund to undertake this research. Undoubtedly, this academic pursuit would not have been initiated and actualised if not for their sponsorships.

ABSTRACT

At high-temperature operations of electronic control devices, Tin-Silver-Copper (SnAgCu) alloy solder joints used to assemble the component of the devices are functioning at homologous temperature above 0.8. In such ambient temperatures, solder alloys have limited mechanical strength and will be sensitive to strain rate. The sensitivity of solder properties to creep/visco-plastic deformation increases the rate of accumulation of plastic damage in the alloy and decreases the number of cycles to failure (N_f) of the joints. Most untimely rupture of solder joints in high-temperature electronics (HTE) system usually culminates in colossal loss of resources and lives. Typical incidences are reported in recent automotive and aircraft crashes as well as the collapse of oil-well logging equipment. To increase the mean time to failure (MTTF) of solder joints in HTE, an in-depth understanding and accurate prediction of the response of solder joints to thermally induced plastic strain damage is crucial.

This study concerns the prediction of the reliability of lead-free solder joints in a flip chip (FC) model FC48D6.3C457 which is mounted on a substrate and the assembly subjected to high-temperature excursions. The research investigates the effect of the high-temperature operations on reliability of the joints. In addition, the investigation examines the impact of control factors (component stand-off height (CSH), inter-metallic compound (IMC) thickness, number of thermal cycle and solder volume) on N_f of the joints. A model developed in the course of this investigation was employed to create the assembly solder joints architecture. The development of the model and creation of the bump profile involve a combination of both analytical and construction methods. The assembled package on a printed circuit board (PCB) was subjected to accelerated temperature cycle (ATC) employing IEC standard 60749-25 in parts. The cycled temperature range is between -38 °C and 157 °C. Deformation behaviour of SnAgCu alloy solder in the joints is captured using Anand's visco-plasticity model and the response of other materials in the assembly were simulated with appropriate model.

The results demonstrate that the reliability of solder joints operating at elevated temperatures is dependent on CSH, thickness of IMC and solder volume. It also shows that incorporating the IMC layer in the geometric models significantly improves the level of accuracy of fatigue life prediction to \pm 22.5% (from the \pm 25% which is currently generally accepted). The findings also illustrate that the magnitude of the predicted damage and fatigue life are functions of the number of ATC employed.

The extensive set of results from the modelling study has demonstrated the need for incorporating the IMC layer in the geometric model to ensure greater accuracy in the prediction of solder joint service life. The technique developed for incorporating the IMC layer will be of value to R&D engineers and scientists engaged in high-temperature applications in the automotive, aerospace and oilwell logging sectors. The results have been disseminated through peer reviewed journals and also presentations at international conferences.

CONTENTS

	PAGE
DECLARATION	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT	iv
CONTENTS	vi
FIGURES	xi
TABLES	xviii
NOMENCLATURE	XX
PUBLICATIONS FROM THE PHD RESEARCH	XXV
CHAPTER 1: Introduction	1
1.1 Background	2
1.2 Motivation for the study	4
1.3 Aim and objectives of the study	6
1.4 Programme of work for the study	6
1.5 Significant findings	9
1.6 Thesis overview	11
1.7 Publications from the study	11
CHAPTER 2: Literature Review: High Temperature Electronics	
(HTE) and Assembly of Flip Chip Component	13
2.1 Introduction	14
2.2 High temperature electronics (HTE)	14
2.3 Flip chip assembly and challenges	20

45

2.3.1 Flip chip device	20
2.3.2 Solder joint reliability	20
2.3.3 Interconnection technology	25
2.3.3.1 Flip chip attachment technique	27
2.3.4 Interconnection material and derivative	29
2.3.4.1 Solders	30
2.3.4.2 IMC	33
2.4 Fatigue life prediction	
2.4.1 Constitutive model for SnAgCu solder	
2.4.1.1 Creep models	37
2.4.1.2 Visco-plastic model	39
2.4.2 Life prediction model	
2.5 Summary	

CHAPTER 3: Prediction of Shape of Flip Chip Solder Bumped Joint and Introduction to Finite Element Modelling (FEM) of Its Assembly

3.1 Introduction	46
3.2 Solder bump model derivation and creation	46
3.3 Assembled flip chip architecture	53
3.4 Finite element modelling (FEM)	57
3.4.1 Background and methodology	57
3.4.2 Materials and their properties	58
3.4.3 Thermal loads and boundary conditions	56
3.5 Summary	61

87

CHAPTER 4: Evaluation of the Reliability of Realistic and Unrealistic Flip Chip Solder Joints at		
4.1 Introduction	63	
4.2 Methodology	65	
4.3 Results and discussion	66	
4.3.1 Study on bump equivalent plastic strain	66	
4.3.2 Effect of IMC on plastic strain behaviour of bump joint	70	
4.3.3 Study on bump joint plastic work	75	
4.3.4 Study on strain energy of bump joint	78	
4.3.5 Effect of IMC on bump joint fatigue life prediction	83	
4.4 Conclusions	86	

CHAPTER 5: Evaluation of the Impact of Component Stand-off Height (CSH) on High-temperature Fatigue Life of Flip chip Lead-free Solder Joints

5.1 Introduction	88
5.2 Methodology	90
5.3 Results and discussions	98
5.3.1 Study on stress and strain in flip chip bump joints	98
5.3.2 Study on plastic work density in FC solder joints	113
5.3.3 Effect of CSH on fatigue life of flip chip solder joints	114
5.4 Conclusions	116

CHAPTER 6: Study of the Effect of Thickness of Inter-metallic		
Compound on Damage and Fatigue Life of Lead-free		
Flip Chip Solder Joints at High-Temperature		
Excursions	117	
6.1 Introduction	118	
6.2 Methodology	120	
6.3 Results and discussion	126	
6.3.1 Study on equivalent plastic strain	126	
6.3.2 Study on equivalent stress	129	
6.3.3 Evaluation of hysteresis loop of FC bump joints	134	
6.3.4 Study on strain energy of FC bump joints	153	
6.3.5 Evaluation of accumulation of plastic work density	156	
6.3.6 Study on FC bump joints fatigue life Prediction	159	
6.4 Conclusions	161	

CHAPTER 7 Prediction of Damage and Fatigue Life of High-temperature Flip Chip Assembly		
Interconnections at Operations	162	
7.1 Introduction	163	
7.2 Background	164	
7.3 Methodology	167	
7.3.1 Finite element modelling	167	
7.3.1.1 Model and method	167	
7.3.1.2 Materials and properties	170	
7.3.1.3 Loads and boundary conditions	170	
7.4 Results and discussion	171	
7.4.1 Study on equivalent stress	171	
7.4.2 Study on hysteresis loop of the solder joint	179	

7.4.3 Assembly solder joint fatigue life prediction	181
7.4.4 Effect of thermal cycle number on magnitude of	
accumulated damage and predicted life of FC joints	188
7.5 Conclusions	195

CHAPTER 8: Conclusions and Recommendations for Further Work 197

8.1 Introduction	198
8.2 Conclusions	198
8.3 Recommendations for further work	200
8.2.1 General recommendations	200
8.2.2 Specific recommendations	201

References204Appendix: ANSYS Code used to Compute Plastic Work in Solder Joints

LIST OF FIGURES

PAGE

Figure 1-1	Programme of PhD research work	8
Figure 2-1	Range of high-temperature ambient	14
Figure 2-2	Effect of high-temperature on HTE failure rate	15
Figure 2-3	FC package showing dummy component and PCB	16
Figure 2-4	Flip chip assembly daisy chain layout	17
Figure 2-5	Effects of CTE mismatch in a typical FC assembly	22
Figure 2-6	Chip attachment process	24
Figure 2-7	Flip chip attachment process	27
Figure 2-8	Solder bump containing IMC	31
Figure 2-9	Metal strength plotted against its melting temperature	34
Figure 3-1	Solder ball and bump profile	50
Figure 3-2	Flip chip architecture	53

Figure 3-3	Flip chip assembly	54
Figure 3-4	Force interactions in flip chip solder joint	54
Figure 3-5	Longitudinal cross section of FC solder joint assembly	54
Figure 3-6	Plot of temperature profile of thermal load test	58
Figure 4-1	Plastic strain damage on critical solder bump	66
Figure 4-2	Plot of equivalent plastic strain on solder bump against load step	67
Figure 4-3	Plot of equivalent plastic strain for region 2 against load step	67
Figure 4-4	Plot of equivalent plastic strain distribution along	
	longitudinal sections of solder bump against load step	68
Figure 4-5	Plot of plastic work density against thermal cycle	74
Figure 4-6	Plot of change in plastic work density in solder bump against thermal cycle	75
Figure 4-7	Plot of percentage change in plastic work density in solder bump against thermal cycle	75

List of Figures

Figure 4-8	Strain energy damage in solder regions	77
Figure 4-9	Plot of strain energy density of solder bump against load step	79
Figure 4-10	Plot of regional strain energy density of solder against load	80
Figure 4-11	Comparison of predicted and measured mean life for eutectic SnPb solder joint	83
Figure 5-1	Parametric ANSYS script window showing outline of all parameters and parts of table of design	89
Figure 5-2	Parametric ANSYS script window showing full table of design points	90
Figure 5-3	Six sizes of solder bump	92
Figure 5-4	Radius of bond pads at both PCB and die sides	93
Figure 5-5	A single flip chip solder bump showing solder region contained in solder bump	93
Figure 5-6	Relationship between size of PCB bond pad diameter and solder bump shape parameters	95
Figure 5-7	Plots of bump stress and solder stress as functions of bond pad size	98
Figure 5-8	Plot of bump strain as a function of bond pad size	98

Figure 5-9	Damage in bump and solder using stress as indicator		
Figure 5-10	Figure 5-10 Relative position of damage in bump three and solder region using stress as the indicator		
Figure 5-11	Relative position of damage in bump five and its solder region using stress as the indicator	104	
Figure 5-12	Relative position of damage in bump six (B_6) and its solder region using stress as the indicators	104	
Figure 5-13	Damage in bump and solder using strain as indicator	106	
Figure 5-14:	SEM image of a solder joint cracked at interface of solder and IMC at die side after being subjected to ATC	108	
Figure 5-15	Plot of change in accumulated plastic work over solder region	110	
Figure 5-16	Plot of predicted assembly life over pad size	112	
Figure 5-17	Plot of predicted assembly solder joint life over bump	112	
Figure 6-1	Project schematic showing that parametric design were integrated in it	118	
Figure 6-2	Outline of design parameters showing input and Output Parameters and some part of table of design	119	

Figure 6-3 Outline of full table of design points showing design

	Parameter values and some generated values	120
Figure 6-4	A bump showing 6 μ m thickness of IMC at both die and PCB sides of the FC assembly	121
Figure 6-5	Model number plotted as a function of its IMCT	122
Figure 6-6	Relationship between model number and solder volume	123
Figure 6-7	Plot of strain behaviour of the five models over load step	125
Figure 6-8	Plot of values of maximum equivalent plastic strain as a function of model number for both solder and bump	126
Figure 6-9	Plot of behaviour of stress in solder over load step For the models	129
Figure 6-10	Plot of behaviour of stress in bump over load step for the five models	130
Figure 6-11	Plots of solder and bump stresses as function of model	131
Figure 6-12	Plot of bump stress and hysteresis loop	132
Figure 6-13	Plot of stress state of solder bump under thermal cycle (in percentage)	133
Figure 6-14	Evolution of hysteresis loop in different bump models	138

Figure 6-15	Plot of reduced plastic work of solder joint	
Figure 6-16	Plot of hysteresis in solder in joint	143
Figure 6-17	Plot of hysteresis in solder bump in joint	145
Figure 6-18	Variation of stress-strain curve of solder stress for various model number	146
Figure 6-19	Variation of stress-strain curve of bump stress for various model number	146
Figure 6-20	Plot of variation of percent by volume of IMC and solder in bump with models	147
Figure 6-21	Variation of bump yield stress and plastic strain with model no.	147
Figure 6-22	Plot of hysteresis loops of models	149
Figure 6-23	Plot of strain energy of the models	152
Figure 6-24	Plot of plastic work density as a function of thermal cycle no	154
Figure 6-25	Plot of change in plastic work density as a function of thermal cycle no.	154
Figure 6-26	Plot of change in plastic work density as a function of model no.	156
Figure 6-27	Plot of life of solder joint and bump joint as a	

	Function of model number.	157
Figure 7-1	A flip chip architecture with mesh	166
Figure 7-2	Plot of equivalent stress of joint member as a function of temperature load step	169
Figure 7-3	SEM images of solder bump	172
Figure 7-4	Stress distribution at solder bump	175
Figure 7-5	Plot of hysteresis loop of realistic and unrealistic solder bump joint	177
Figure 7-6	Visco-plastic damage in critical solder bump joint	184
Figure 7-7	Plot of accumulated damage and average Accumulated damage of solder joint @ cycle number as functions of temperature cycle number	187
Figure 7-8	Comparison of average damage from cycle 3 to 19 with average of other ATC	188
Figure 7-9	Comparison of predicted life when average damage from cycle 3 to 19 is utilised with life estimated when average of other ATC is employed	189

LIST OF TABLES

		PAGE
Table 2-1	Example of lead-free solder alloys melting between 180-200°C	29
Table 2-2	Example of lead-free solder alloys melting between 200-230°C	30
Table 2-3	Example of lead-free solder alloys melting above 230°C	30
Table 2-4	Constants in ANAND's constitutive model for SnAgCu solder	38
Table 2-5	Creep fatigue life models for SnAgCu by Syed	41
Table 3-1	Generated bump profile	49
Table 3-2	Parameters of flip chip	52
Table 3-3	Mechanical properties of assembly materials	56
Table 4-1	Solder bump configuration and plastic strain	71
Table 4-2	Effects of IMC on FC solder joint fatigue life	82

Table 4-3	Deviations of predicted solder joint fatigue life From measured/experimental value	83
Table 5-1	Configuration of PCB bond pad diameter	94
Table 5-2	Configurations of solder bumps, (B_i)	94
Table 5-3	Correlation between modelled assembly and similar experimental works from literature	109
Table 5-4	Relationship among bond pad size, solder bump damage and predicted life of solder joint	111
Table 7-1	Comparison of literature values of solder joint fatigue life with our current results	191

NOMENCLATURE

(a) ABBREVIATION

ALT	Accelerated life testing	HALT	Highly accelerated life testing
ATC	Accelerated thermal cycle	HATC	Highly accelerated thermal cycle
CAGR	Compound annual growth rate	HMP	High melting point
COB	Chip on board	HPC	High-performance computing
CSH	Component stand- off height	HT	High temperature
CSP	Chip scale package	HTE	High-temperature electronics
CTE	Coefficient of thermal expansion	HTHE	High-temperature harsh environment
Cu	Copper	HTME	High temperature microelectronics
DM	Design modeller	I/O	Input/output
ECU	Electronic control	1/0	Input/output
	unit	IC	Integrated circuit
FC	Flip chip	IEC	International electrotechnical commission
FCOB	Flip chip on board		
FE	Finite element	IMC	Inter-metallic compound
FEA	Finite element analysis	LHS	Left hand side
FEM	Finite element method	MEMS	Micro- electromechanical system

Nomenclature

MTTF	Mean time to failure	SiC	Silicon carbide
MWD	Measurement while drilling	SMC	Surface mount component
NEMI	National electronics manufacturing initiative	SMDs	Surface mount devices
Ni	Nickel	SMD SMT	Solder mask defined Surface mount technology
PCB	Printed circuit board	SnAgCu	Tin-Silver-Copper
R&D	Research and development	SOI	Silicon on insulator
R^2	Correlation coefficient	THT	Through-hole technology
RHS	Right hand side	WEEE	Waste from
SBJ	Solder bump joint		electrical and electronic equipment
SEM	Scanning electron microscope		

(b) NOTATION

<i>s</i> *	saturation value of s	W _{Die}	Weight of the FC
E _{cr}	Creep strain rate	v_T	Total volume of bump
ΔW_i	Plastic work accumulated	W _{acc}	Accumulated creep energy
$\Delta W_{p,avg}$	Average value of plastic work	w _p	Plastic work
d ^p	Effective inelastic	y_c	vertical distance in z
h_0	deformation rate Ball height	δv_T	Change in volume of solder bump
V _{if}	Regional volume fraction	E _{acc}	Accumulated creep strain
C'	Inverse of creep ductility	εί	Regional plastic strain
I_{χ}	Second moment of area	$ heta_h$	Obtuse angle surface tension makes with
P_0	Internal pressure		upper bond pad plane
P_a	Ambient pressure	Ø	Ball centre diameter
<i>R</i> _{1,2}	Principal radii of curvature of the	ΔV_i	Volume of element <i>i</i>
	solder surface at h	ΔW_j	Loop area
R _h	Radius of Cu pad at die	А	Pre-exponential factor
R _c	Ball centre	a	Strain rate
W	Creep energy density for failure		sensitivity of hardening/softening
		A_1	Constant

b	Averageofsummationofwidthsofcomponent andPCB	R _{arc} H₁/k	Bump arc radius Apparent activation energy
В	Bump	h _o	Hardening/softening
\mathbf{B}_{i}	Generated bumps size	i	Trajectory path
B _{ol Mjy}	Bump yield stress	j	Model number
C	Cycle number	Κ	Kelvin scale
		L	Load step
C $C_{I, C_{II, W_{I}}}$	Cycle W_{II} constants	m	Strain rate sensitivity of stress
$D\Delta W_p$	Change in plastic work	М	Moment about the neutral axis (CSH)
	density per cycle.	М	Model
D_i	PCB bond pad diameters	Ν	Strain rate sensitivity of
Do	PCB bond pad diameter		saturation value
E	Young Modulus of Elasticity	n	Number of ball on die
F	-	Ν	Newton
E _{IMC,P}	Error due to non incorporation of IMC	N_f	Number of cycle /repetition to failure
G	Elastic shear modulus	No.	Number
g	Gram	P_i	PCB bond pad size
Н	Perpendicular distance to the neutral axis	Q/R	Activation energy/Boltzmann's constant
h	Bump height		

R	Universal	gas	3	Plastic strain
R _{arc}	constant Bump arc		K	Boltzmann's constant
S	Deformation		ې	Multiplier of stress
	resistance		σ	Bending stress
Ŝ	Coefficient deformation	for	σ_b	Bump stress
	resistance satur value	ation	σ_s	Solder stress
S.	Solder region		$\sigma_{\rm v}$	Equivalent stress
S _i	Solder region	of	γ	Surface tension
So	initial value deformation resistance	of	$D\Delta W_{p,avg}$	Change in plastic work average
$S_{ol\ Mjy}$	Solder yield stre	ess	f	Function
Т	Absolute temperature		kg	Kilogram
T_a	Ambient		β	Volumetric expansion
	temperature		50	-
T_h	Homologous temperature		δθ	Range of temperature cycle limits
T_m	Melting temperature		σ	Effective Cauchy stress
W_D	Elastic strain er of distortion	lergy	σ	Stress
α	Stress level at w the power dependence br down	hich law reaks	υ	Poisson ratio

PUBLICATIONS FROM THE PHD RESEARCH

- [1] E.H. Amalu, N.N. Ekere (2011), High temperature reliability of lead-free solder joints in a flip chip assembly, Journal of Materials Processing Technology, vol. 212. pp. 471-488.
- [2] E.H. Amalu, N.N. Ekere, S. Mallik (2011), Evaluation of rheological properties of lead-free solder pastes and their relationship with transfer efficiency during stencil printing process, Materials and Design, vol. 32. pp. 3189-3197.
- [3] E.H. Amalu, W.K. Lau, N.N. Ekere, R. S. Bhatti, S. Mallik, K.C. Otiaba, G. Takyi (2011), A Study of SnAgCu Solder Paste Transfer Efficiency and Effects of Optimal Reflow Profile on Solder Deposits, Microelectronics Engineering, vol. 88. pp. 1610-1617.
- [4] E.H. Amalu, N.N. Ekere, R.S. Bhatti, G. Takyi and A.O.A. Ibhadode (2012), Numerical Investigation of Thermo-Mechanical Behaviour of Ball Grid Array Solder Joint at High Temperature Excursion, Advanced materials research vol. 367 (2012). pp 287-292, TRANS Tech publications, Switzerland.
- [5] G. Takyi, E.H. Amalu and P.K. Bernasko (2011), Effect of Solder Joint Integrity on the Thermal Performance of TEC for a 980 nm Pump Laser Module, Soldering & Surface Mount Technology, vol. 23. Iss. 2. pp. 115 -119.
- [6] K.C. Otiaba, N.N. Ekere, R.S. Bhatti, S. Mallik, M.O. Alam, E.H. Amalu, (2011), Thermal interface materials for automotive electronic control unit: Trends, technology and R&D challenges. Microelectronics Reliability. vol. 51, Iss. 12. pp. 2031-2043.
- [7] E.H. Amalu, N.N. Ekere and G. Aminu (2011) Effects of intermetallic compound on high temperature reliability of flip chip interconnects for fine pitch applications, in: Proc 3rd IEEE International Conference on Adaptive Science & Technology, 24-26 November 2011, Abuja, Nigeria. pp. 208-214.
- [8] K.C. Otiaba, R.S. Bhatti, N.N. Ekere, S. Mallik, E.H. Amalu and M. Ekpu (2011), Thermal effects of die-attach voids location and style on performance of chip level package, in: Proc 3rd IEEE International Conference on Adaptive Science & Technology, 24-26 November 2011, Abuja Nigeria. pp. 231-236.

- [9] M. Ekpu, R. Bhatti, N. Ekere, S. Mallik, E. Amalu and K. Otiaba (2011), Investigation of effects of heat sinks on thermal performance of microelectronic package, in: Proc 3rd IEEE International Conference on Adaptive Science & Technology, 24-26 November 2011, Abuja, Nigeria. pp. 127-131.
- [10] E.H. Amalu, N.N. Ekere, G. Aminu, (2011), Modeling High Temperature Reliability of Flip Chip Pb-free Solder Joint at varying Bond Pad Diameter, in proc: AES-ATEMA' 2011 International Conference on Advances and Trends in Engineering Materials and their Applications, Montreal, Canada, 01-05 August, 2011, pp. 385-393.
- [11] E.H. Amalu, N.N. Ekere, R.S. Bhatti and G. Takyi (2010), Investigation of Effects of Reflow Profile Parameters on Lead-free Solder Bump Volumes and Joint integrity, in: Proc: International Conference on Advances in Materials and Processing Technologies (AMPT 2010), 24th-27th October 2010, Paris, France. American Institute of Physics, AIP Conf. Proc. January 17, 2011. Vol. 1315, pp. 639-644.
- [12] E. H. Amalu, N.N. Ekere, R.S. Bhatti, G. Takyi and A.O.A. Ibhadode (2010), Numerical Investigation of Thermo-Mechanical Behaviour of Ball Grid Array Solder Joint at High Temperature Application, in Proc: 3rd International Conference on Engineering Research & Development: Advances in Engineering Science & Technology 7th-9th September 2010, Benin City, Nigeria, pp. 1242-1251.
- [13] K.C. Otiaba, N.N. Ekere, E.H. Amalu R.S. Bhatti, S. Mallick, (2010), Thermal Management Materials for Electronic Control Unit: Trends, Processing Technology and R&D Challenges, in Proc: 3rd International Conference on Engineering Research & Development: Advances in Engineering Science & Technology 7th-9th September 2010, Benin City, Nigeria, pp. 1270-1280.
- [14] E.H. Amalu, N.N. Ekere and R.S. Bhatti (2009), High Temperature Electronics: R&D Challenges and Trends in Materials, Packaging and Interconnection Technology, in: Proc 2nd International Conference on Adaptive Science & Technology, 14-16 December 2009, Accra, Ghana, pp. 146-153.
- [15] E.H. Amalu, Ndy N. Ekere (2012), Prediction of damage and fatigue life of high-temperature flip chip assembly interconnections at operations. Revised manuscript submitted to Journal of Microelectronics Reliability. January, 2012.

- [16] E.H. Amalu, Ndy N. Ekere and R.S. Bhatti (2012), High-temperature fatigue life of flip chip lead-free solder joints at varying component stand-off height. Revised manuscript submitted to Journal of Microelectronics Reliability. January, 2012.
- [17] K.C. Otiaba, R.S. Bhatti, N.N. Ekere, S. Mallik, M.O. Alam, E.H. Amalu, M. Ekpu (2012), Numeerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device. Article in press at Microelectronics Reliability.

Chapter 1: Introduction

CHAPTER 1

INTRODUCTION

1.1 Background

In a world that electronics, their devices and modules have become vital to the effective functioning of most systems from space craft, airplanes, power grids, oilwell logging tools and automobiles to implanted medical devices; proper understanding of how and when they fail is now a matter of both life or death and profit or loss. Equally for the military, soldiers at the battlefield depend on electronics for successful communication, navigation, surveillance and weapons launching. Knowing when a system will fail is needed to schedule and undertake maintenance or obtain replacement systems to avoid disappointment and accident.

The failure rate of solder joints of assembled components in electronic devices and modules has been demonstrated to increase at elevated temperature. Thus, indepth understanding of the behaviour of solder joints at high-temperatures is needed to accurately predict electronic product reliability. Accurate prediction of mean time to failure/mean time before failure (MTTF/MTBF) identifies the critical time to undertake system maintenance and/or obtain replacement system. Owing to the increase in the deployment of electronic systems to high-temperature harsh environment recently, the development of electronic systems that can operate reliably in harsh environmental conditions and at high-temperatures has been identified by the electronics manufacturing industry as a critical technology for the 21st century.

The integrity of solder bump joints of most flip chip (FC) devices mounted on metallised bond pads of substrates can be increased if optimal settings of static structural parameters of the joints were utilised in their assembly. The majority of geometric models of solder joints utilized in computer modelling studies on reliability of solder interconnects do not contain inter-metallic compound (IMC) even though it is a general knowledge that an IMC layer is always formed at the interface of tin-based solders and metalized copper substrates. In addition, the use of many numbers of accelerated temperature cycle (ATC) in testing virtual models of solder joints has not been a common practice. Most studies use one or two cycles. The main disadvantage of the first scenario is that a low integrity joint is formed; which has reduced MTTF. The exclusion of IMC in the models and utilisation of less than six thermal cycles in ATC are inappropriate. These practices yield inaccurate data in simulation output which leads to wrong interpretation of effects and inexact prediction of damage and life of solder joints.

The in-depth understanding of thermo-mechanical behaviour of realistic solder bump joint (SBJ) used to attach some surface mount devices (SMDs) to substrates such as printed circuit boards (PCBs) during microelectronic packaging is the key to improving the operational reliability of these packages. Solder joints in hightemperature electronic (HTE) products are considered as reliability critical because they frequently fail under thermal fatigue loads and their MTTF decreases at elevated temperature. Computer simulation is employed to quantify the impacts of static structural factors such as IMC and solder ball shape parameters on the number of cycle to failure (N_f) of the joint. The N_f is a function of accumulated visco-plastic damage of solder joint.

To date, most modelling studies on the reliability of solder bump joints have not included IMC in their models. IMC is generally known to impact solder joint integrity, however its specific contribution to the fatigue life of solder joints is yet to be fully understood. The non inclusion of IMC in models used to predict the N_f of solder joints is proposed as one of the causes of discrepancy between the value of assembled component solder joints fatigue life obtained by experiments and the estimated value from modelling studies [1].

The reliability of solder joints of a FC soldered on a printed circuit board (PCB) also depends on the profile of the solder bump [2-4]. The profile of solder bump in a FC package mounted on a substrate is governed by the geometric relationship between diameters of the bond pad at its die side and the bond pad on the substrate. Most often, these bond pads are defined by the solder mask. This technique is known as solder mask defined (SMD) technology. Other bump shape parameters such as component stand-off height (CSH) and arc radius, which trace the profile of the bump, are functions of the bond pads diameter.

1.2 Motivation for this study

The customers' demand for advanced and miniaturised electronic devices which possess high functionality and performance capabilities has necessitated that research and development (R&D) engineers design and develop smaller electronic packages to assemble these products. Surface mount technology (SMT) and the use of surface mount component (SMC) such as FC enable actualisation of the users' demand. The FC package evolved when the trend in interconnection technology advanced from wire bonding to solder bumping. Solder bump is used to attach the component to a substrate PCB through reflow soldering process. The solder joints of FC packages have demonstrated acceptable reliability in operation and hence the extensive use of the component to assemble microelectronic products which operate at normal ambient.

In recent times, advanced packaged microelectronic modules have increasingly found applications in sectors where operating ambient temperatures are harsh [5-9]. Since the life expectancy of solder joints in these components in these systems reduces exponentially as the operating temperature increases, their long term reliability will be adversely impacted. The integrity of these joints may be more critical since, in addition to component/joint size reduction, SMT uses a small amount of solder to connect the package to the PCB. Consequently, failure of HTE systems at interconnects has increased in recent times. One well known scenario is the failure of automotive electronic control unit (ECU) of many automobiles recently. The cost of recalls and the loss of customer good-will associated with the failure are undesirable.

The failure of a solder joint of a FC in HTE leads to failure of the whole unit. The joints of the assembled package fail partly by accumulation of damage caused by plastic deformation of solder. The other cause is mismatch in the thermal expansion coefficient (CTE) of bonded materials in the joint. Plastic work density (also known as strain energy density) is an index used to determine the damage. The change in the plastic work density from cycle to cycle accumulates the damage in the joints. The assembly of reliable FC solder joint that will meet expected satisfactory operation, whilst in service, requires a proper understanding and control of these key factors impacting its fatigue failure.

Thus, a study focused on investigating the effects of reliability factors and their interactions as well as effect of the operating condition on integrity of the solder joint is needed to provide further information on damage mechanism of FC solder joints. The information will be used to improve the solder joint reliability and also predict with reasonable accuracy its service life. To achieve this goal, a modelling study to predict the reliability of lead-free solder joints in a FC assembly at high temperature excursion is carried out.

1.3 Aim and objectives of the Study

The aim of this research work is to study high-temperature reliability of lead-free solder joints in a flip chip assembly. The objectives of the study are to:

- Investigate high-temperature fatigue life of flip chip lead-free solder joints at varying component stand-off heights.
- Establish the contribution of thickness of IMC on the integrity of FC bump joints at elevated temperature operations.
- Investigate the effects of percentage by volume of IMC in FC bump joint on its high-temperature reliability.
- Study the impact CSH has on high temperature reliability of FC solder bump joints.
- Investigate the dependency of accumulated damage and fatigue life of solder joints on the number of ATCs employed and establish the appropriated number of cycle suitable for accurate damage value determination.

1.4 Programme of work for this study

The study began with extensive review of relevant and related previously published works. The main focus of the literature review is to identify the gaps in knowledge in the area of reliability of solder joints in a flip chip assembled on a printed circuit board using lead-free solder alloys and which is subjected to accelerated temperature cycle. Four gaps in knowledge were recognised after substantial search of literature. It was found that there is a discrepancy between experimentally determined and predicted solder joints fatigue life. In addition, the effect of component stand-off height on the reliability of flip chip assembly was inconclusive as divergent opinion was held by different researchers. Similarly, it was discovered that the effect of the thickness of IMC on the integrity of solder bump joints has only been investigated using experimental methods. The reported studies centred on the relationship between the thickness of IMC and the mechanical strength of the joints. A complimentary modelling study was needed to quantify the reliability of the joints in such condition. Moreover, it was found that the determination of accurate accumulated damage in the solder joints is inconclusive. There was no established definite number of thermal cycles to be employed in the determination of this accurate solder joint damage. Many researchers have been employing different number of thermal cycles.

These four identified gaps formed the integral part of the studies carried out in this study and also reported in this thesis. Experiments were designed to investigate these concerns. The four-case design employed two geometric models for case A, six geometric models in case B, five geometric model in case C and two geometric models in case D. These solid models were input into ANSYS finite element modelling software to perform static structural analysis on them. The modelling procedure involved meshing the geometric models, applying the models of the materials, boundary conditions and thermal load. The measured output parameters from the modelling include the viscoplastic deformation, stress, plastic work density, strain energy density and fatigue life of the solder bump joints in the models. The programme of work is presented in figure 1.1.

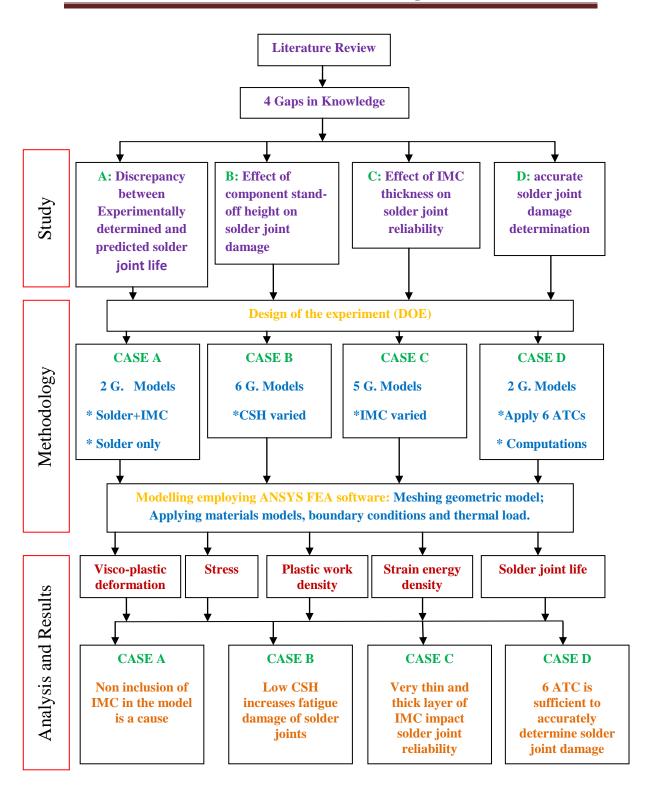


Figure 1-1 Programme of PhD research work

1.5 Significant findings

To the best of my knowledge and since most of the concepts have been published, many findings from this work are considered significant.

- (i) The incorporation of IMC in the geometric model employed to predict the number of cycle to failure of the solder bump joints in a FC assembly improves the accuracy of the model from $\pm 25\%$ which is currently generally accepted to $\pm 23.5\%$ and also increases the accuracy of the predicted fatigue life of the critical bump.
- (ii) The failure mechanism of solder bump which consists of IMC is different from the one which does not contain IMC; a combination of fatigue damage and plane plastic shear strain principally drive failure in bumps with IMC while plastic deformation driven by shear damage is a key failure mechanism in bumps without IMC.
- (iii) Low CSH promotes fatigue cracks at interconnects between FC IMC at die side and solder region.
- (iv) The integrity of solder joints in a FC component becomes significantly critical when the diameter of SMD bond pad on its PCB exceeds 110% of the size of diameter of SMD bond pad at its die side at high-temperature operations.
- (v) The impact of very thin and very thick IMC on the reliability of solder joint is more significant than moderate thickness.
- (vi) The failure mode in the solder bump joints of a FC assembly is a combination of fatigue damage which occurs at early period of

device operations and both shear and visco-plastic damage which are accumulated over its prolonged operations.

- (vii) Visco-plastic based models are arguably inadequate to predict solder joint life.
- (viii) The interconnect boundary between IMC at the die side and solder region frequently fail by fatigue crack mechanism because the difference in stress magnitude and amplitude between the two constituents are highest in the joint assembly.
- (ix) The average damage from cycle of hysteresis loop stabilisation to the onset of tertiary damage is sufficient for modelling study to predict damage and fatigue life of solder joints in a flip chip assembly.
- (x) The magnitude of damage as well as the fatigue life predicted for a FC solder joints is a function of the number of ATCs used in the modelling.
- (xi) Flip chip model FC48D6.3C457DC can be used for assembly applications which function at 150°C for about 400hours. Thus, it can reliably operate in traditional wire line logging at 150°C and measurement while drilling (MWD) at 150°C for up to 400 hours.

1.6 Thesis Overview

Chapter 1 gives a brief overview of the research work presented in this thesis. It presents the overview in six sub-headings ranging from introduction through to motivation and outline of the thesis. The chapter also presents the publications from this research work. It ends with the significant findings and contributions of the study. As a sequel to chapter 1, the thesis presents in chapter 2 the review of literature relevant to this investigation. The research on geometric model derivation, creation of FC architecture and generic approaches to finite element modelling is contained in chapter 3. Chapter 4 deals with the reliability of realistic lead-free solder joints in a FC assembly at high temperature excursions cycle loading. In chapter 5, the impact of CSH on the fatigue life of the solder joints is presented. The effect of thickness of IMC on high temperature reliability of the solder bump joints which are cycled between -38°C and 157°C temperatures is presented in chapter 6. Chapter 7 considers the effect of a number of thermal cycles on the magnitude of damage accumulated in the joint and also determines how many cycles are sufficient to determine accurately solder joint damage. This chapter in addition evaluates the impact of number of cycles on predicted solder joint life. Finally, chapter 8 presents the conclusions and recommendations for future work.

1.7 Publications from the Study

Two journal papers [1, 10] and four conference papers [5, 11-13] have been published from the work presented in this report. There are other recent publications by the author in the course of this PhD research. These include four journal papers [14-17] and two conference papers [18, 19]. The highlights of publications based on the work reported in this thesis are:

- The review on high temperature microelectronics presented in chapter 2 is based on a paper [5] published at an IEEE conference in 2009.
- The FC solder bump joint shape prediction presented in chapter 3 is an aspect of a paper [1] published in Journal of Materials Processing Technology.
- The evaluation of the reliability of realistic and unrealistic flip chip solder joints at high-temperature applications presented in chapter 4 is the complementary part of the paper covered in part in chapter 3.
- The work which covers the impact of CSH on high-temperature fatigue life of FC lead-free solder joints presented in chapter 5 is written in a manuscript and the revised version has been submitted to the Microelectronics Reliability Journal. This work had been published earlier in a conference in Canada in 2011 [11].
- The results from the investigation of effect of IMC on damage and fatigue life of lead-free solder joints in a FC assembly are presented in an IEEE conference in 2011 [13]. The work is also being developed further for journal publication.
- Chapter 8 reports on investigation which has been written in a manuscript and the revised version has been submitted to the Journal of Microelectronics Reliability [20].

CHAPTER 2

LITERATURE REVIEW: HIGH-TEMPERATURE ELECTRONICS (HTE) AND ASSEMBLY OF FLIP CHIP COMPONENT

2.1 Introduction

This chapter contains the review of previously completed research work in the area of High-Temperature Electronics (HTE), FC assembly, challenges of solder joint reliability and prediction of solder joint fatigue life. The review on HTE is centred on its classification in terms of application sectors and categorisation in terms of its function. The information available on HTE market volume in the various sectors of its applications is summarised. In addition, the temperature range of interest to industries was reviewed and ranked.

In the review on FC assembly and challenges, the history of FC was mentioned briefly. The reason is given for the continued increase in its usage in manufacture of integrated circuit (IC), giving rise to the increase in its market volume. Other sections of this review are on solder joint reliability, interconnection technology and interconnection materials and their derivative.

The review on previous works on the prediction of fatigue life of solder joint was carried out in two broad sub-headings. These are the constitutive model for lead free solder and the life prediction model.

2.2 High temperature electronics (HTE)

Electronics which operates in ambient temperature above 125°C is termed hightemperature electronics (HTE). It is a technology designed for applications such as electronic control unit (ECU) in automobile, power electronics in trains and aeroplanes and oil-well logging modules which operate at high ambient temperature. At the heart of many high-temperature electronics devices are the high-temperature electronics module assembled using flip chip components that

often need to handle very strong thermal loads and endure hostile environment. Traditionally, electronics operates within the range of -55°C/-65°C to 125°C temperatures. Recent advancements in technology have necessitated the replacement of pneumatic and mechanical sensors and control devices operating at elevated temperature in systems with electronic systems. This trend compels such microelectronics assembly units to operate under harsh environmental conditions and at very high temperatures. Amalu et al. [5], reported that the reliability of electronic systems is partly dependent on its operating ambient conditions; and reliability generally decreases in harsh operating conditions. In the same paper, the authors stated that the life expectancy of components and systems is known to reduce exponentially as the operating temperature increases; adversely impacting long-term system reliability. In a report prepared by Sandia National Laboratories on the first high-temperature electronics products survey in 2005, Normann [8] not only stated that long-term reliability of electronic system at high- temperature (HT) is a key challenge, but also identified reliability as a major driving force in the development of HTE applications as HT components of modules and sensors must be reliable.

For ease of classification, HTE application sectors can be grouped into three and its devices categorised into two main divisions; while the sectors are aerospace, oil-well and geothermal drilling and automotive industries, the categories are power (power converters such as DC/DC and AC/DC) and data acquisition. The HT operating requirements of these industries vary in terms of market volume and operating ambient temperature. Nornann [8] reported that the drilling industry market for HTE is small - 100 to 1000(s) devices per year and the aerospace industry has 10 to 100 times the market for HTE as the drilling industry.

Equally, there are huge challenges and opportunities for the automotive sector. The market for electronics applications in vehicles is estimated to reach £80 billion by the end of 2008 as new technologies and standards continue to push the

adoption of electronics in vehicles to provide further driver assistance, safety, passenger comfort, information and entertainment [5, 21]. As the electronics content in vehicles increase, more and more electronic devices (including micro-electromechanical system (MEMS)) will be deployed in high-temperature harsh environment (HTHE) to meet specific applications in the 21st century telematic vehicle. For example, a growing number of "smart" devices have been developed and deployed to help improve performance of the engine, transmission, steering, and traction control [5]. As some of these sensor electronics and control devices are deployed under-bonnet, and in other harsh body environments, they can rapidly cycle from 180°C to -40°C operating temperature, depending on driving location and climate [5, 22]. Johnson et al. [6] are of the view that high-temperature electronics used in automotive systems will continue to grow. They reported that in 2003, the electronics content in an automotive was \$1510 and is expected to reach \$2285 per vehicle in 2013.

In the same survey reported in ref. [8], Normann presented the response of 23 application engineers who were asked the temperature range of interest to their industries. Fig. 2-1 presents this response.

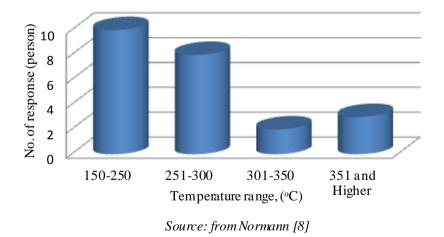


Figure 2-1 Range of high-temperature ambient

One of the key effects of operation of solder joint at HT regions is the reduction in MTTF. Consequently, reliability should always be kept in mind at the assembly

stage of HT components as there is a growing body of evidence that HTE have greatly improved operating lifetimes at lower temperatures. Normann [8] reported that Honeywell HT Silicon on insulator (SOI) electronics rated for 5 years at 225°C have a potential for 10 years at 200°C and 20 years at 150°C. Fig. 2-2 shows schematically the effect of HT on electronic component solder joint. The pertinent question still remains - is the MTTF of HTE within standard acceptable limit and also customer's requirement.

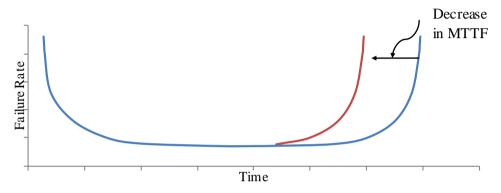
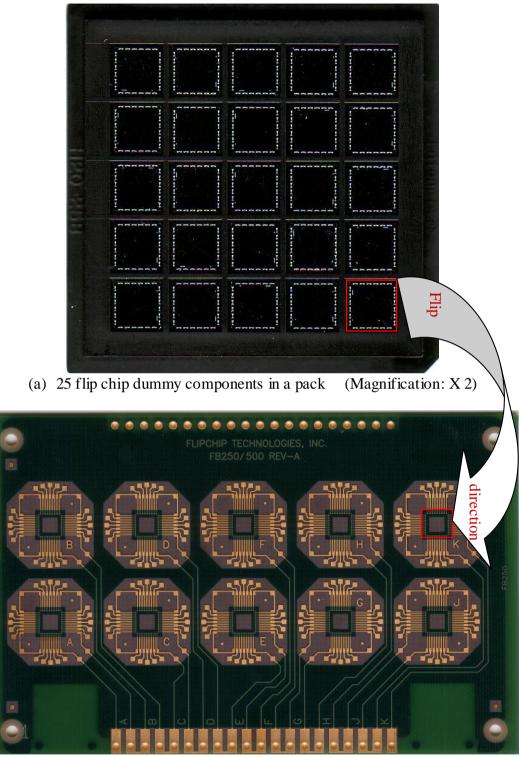


Figure 2-2 Effect of high-temperature on HTE failure rate

The technologies employed in HTE assembly manufacture are through-hole technology (THT) and SMT. Recently, it has been reported that better reliability and performance are achieved through the utilisation of a combination of the two technologies [23]. The combination of THT and SMT is named hybrid technology. SMCs used in the assembly of HTE include multi layer ceramic capacitor, inductor, screen printed resistor, ball grid array (BGA) and FC device. Fig. 2-3 (a) shows a pack of 25 FC packages and fig. 2-3 (b) is a picture of FC48 laminate gold substrate PCB which can be used to mount 10 pieces of the FC. The red boxes in the figure provide a guide for the exact chip position while the arrow shows the flip direction during assembly process. The connection lines are shown on the PCB. The terminals identified as A, B, C, D, E, F, G, J, K and also T_1 and T_2 (fig. 2-4) are used to monitor the resistances in each of the daisy chain layout. Figure 2-4 shows the layout of the daisy chain.

Chapter 2: Literature Review



(b) Printed circuit board used to mount 10 FC die (Magnification: X 2)

Figure 2-3 Flip chip package showing 25 flip chip dummy components in a pack and a printed circuit board used to mount 10 FC die

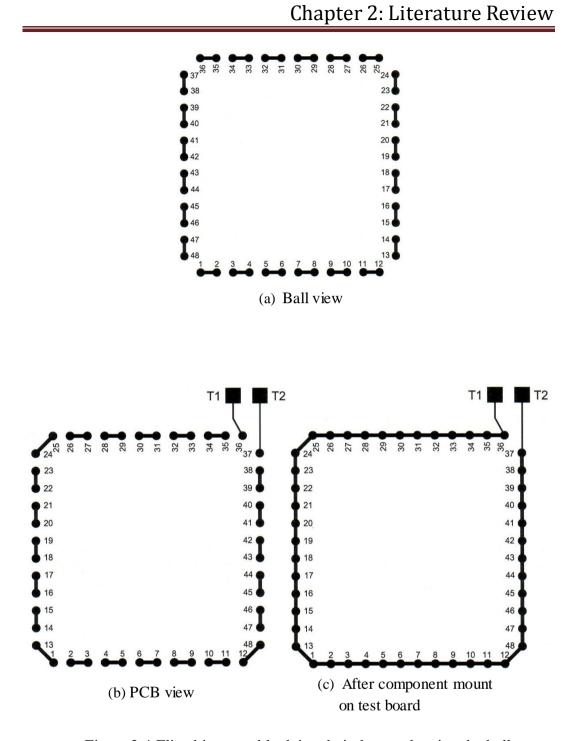


Figure 2-4 Flip chip assembly daisy chain layout showing the ball view , PCB view and the view after component mount on test board

Source: 2007 TopLine dummy components

2.3 Flip chip assembly and challenges

The review on FC assembly and the associated challenges is presented in four sections. These sub-headings are flip chip device, solder joint reliability, interconnection technology and interconnection material and derivative.

2.3.1 Flip chip device

The FCs assembly of die on substrates have been in existence since first developed in the 1960's [24] by IBM [25] and are one of the advanced components used in microelectronics assembly. The device can also be used in stack die technology. With increasing usage of FC in ICs manufacture, the invention is currently poised to be the technology of route for the actualization of ever increasing miniaturization trend and high electronic product performance in contemporary advanced microelectronic packaging.

Consequently, the FC market is growing rapidly at about \$16bn in 2010 [26]. Data from the report [26] shows that FC constitute 13% of all IC packages and predicted growth of about 10.5% compound annual growth rate (CAGR) for wafer bumping during 2010 to 2016.

2.3.2 Solder joint reliability

The desirable properties necessitating the wide acceptance and usage of FC includes higher I/O, improved electrical and thermal performance, miniaturised size and lower cost. However, the recent use of microelectronics as sensors or control devices at HT ambient increases the rate of creep/visco-plastic degradation of joints of their assembly. Although the advance in interconnection technology from wire bonding to solder bumping empowered FCs to have better advantage in electrical performance at high-temperature over other microelectronics (HTM), nonetheless

the miniaturized size increases thermal fatigue failure of the assembly arising from frequent fractures of its solder bumps. The plastic strain response of solder bumps to induced thermal load accumulates damage in the joints which subsequently causes the failure.

Amalu et al. [5] reported that miniaturisation is still a key design trend in electronics industry and Johnson et al. [6] also reported that HTE used in automotive systems will continue to grow. As electronic modules increasingly get smaller and find applications in sectors where operating ambient temperatures are high, assembly and packaging engineers have come under pressure to mount components with high solder joint integrity to meet customer expectation of reliable package performance at extreme high-temperature in the field.

A number of factors impact the reliability of solder interconnects used to attach components of HT electronic modules to the substrate. In their recent study, Amalu et al. [15] identified proper reflow soldering as a factor. Other factors include properties of the solder alloy at high temperature excursion, CTE of the bonded materials, thickness and properties of IMC, operating high temperature condition, cyclic nature of the applied thermal load and solder joint geometry. Xie et al. [27] reported that large die-to-package ratio could incur high stress level on solder joints due to high CTE mismatch. Thus, mismatches in the CTE of the different bonded materials in the assembly accounted for stress inducement and thermo-mechanical failure of solder joints during temperature cycling. The effect of CTE mismatch is shown schematically in fig. 2-5.

The cyclic nature of loading these modules are subjected to, whilst in the field, depreciates the service life of solder joints of their components. Hsu and Chiang [28] reported that the reliability of solder joints depended strongly on the thermomechanical behaviour of the materials and the geometry of the solder joints such

as stand-off height and contact angle. In furtherance of this statement, the author believes that the architecture of solder joint and specifically the profile of the solder bump joints play a crucial role in the overall device reliability. It is pertinent to note that CSH and diameter of bond pads (at both upper and lower interconnects of solder bump) determine the joint geometry and are thus key fatigue and static structural factors. Reichl et al. [29] reported that thermomechanical aspects of component and system reliability become more and more important with growing miniaturisation as the local physical parameters and field quantities show increase in sensitivity due to inhomogeneities in local stresses, strains and temperature fields. Generally, the impact of static structural factors on reliability of chip on board (COB) increases with miniaturisation and the physics of fatigue failure is usually by inducement of plastic strain in the joint. Strain accumulation causes the joint to develop stress which initiates crack. In their work, Libres and Arroyo [30] put up a hypothesis that the observed bump cracks at bulk solder are result of solder fatigue and extensive solder plastic deformation during temperature cycling, coupled with a change in the mechanical properties of the underfill material at the exit side. Furthermore, another work by Yang and Ume [31] cited references suporting the claim that, due to constrains of thermal expansion, excessive strains/stresses might be induced and might eventually initiate and propagate fatigue cracks in solder bumps. Ladani and Razmi [32] have reported that damage mechanism by fatigue cracks is most destructive in the presence of voids in the solder joint.

FC device is the key component which has facilitated miniaturisation of HTE. Li and Wang [33] reported that thermal fatigue failure, due to the facture of solder joints which was caused by the mismatch deformation, is frequently encountered in FC assemblies. This situation could be more critical at elevated temperature of operations. Although it is a common knowledge that the change in interconnection technology from wire bonding to solder bumping improved high temperature performance of FC assemblies from the electrical point of view, however the extreme operating environment of HTE significantly impacts chip-level devices reliability by inducing untimely failures at the board level and FC technology is no exception. Xie et al. [27] believe that board level reliability concern over chip scale packages (CSPs) is that finer pitch limits the size of solder ball attached on die and stencil thickness used in assembly which leads to much smaller joint volume and stand-off height while larger die-to-package ratio typically means higher stress level caused by the CTE mismatch. This situation may not be different for FC assembly.

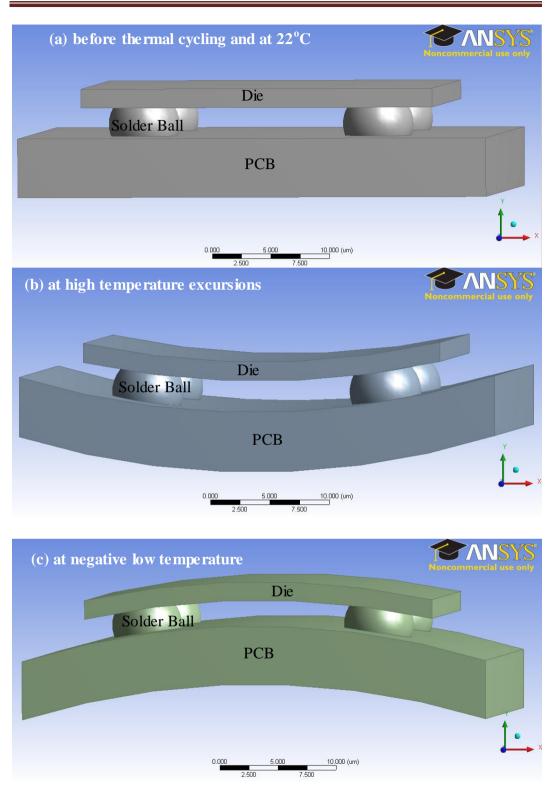
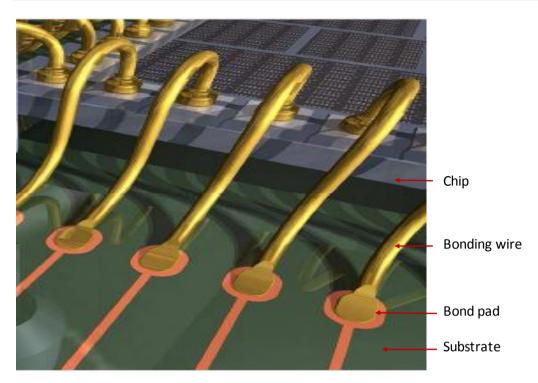


Figure 2-5 Effects of CTE mismatch in a typical flip chip assembly showing the three conditions of assembly operations temperature.

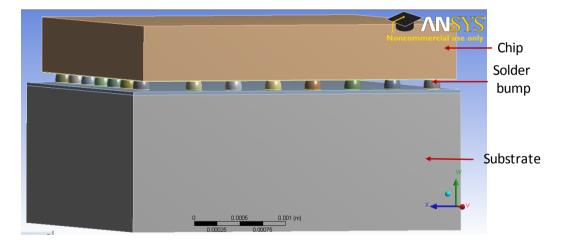
Mallik et al. [34] cited that the useful lifetime of electronic devices can decrease significantly owing to the large thermal stresses that occur especially at solder joint interfaces. Ridout and Bailey [35] reported that solder joints are often the cause of failure in electronic devices.

2.3.3 Interconnection technology

The chip interconnects to the substrate remain the key challenge in HTE assembly. There are basically two attachment methods. These are wire bonding and solder bumping. Fig. 2-6 shows the chip attachment process. While fig. 2-6 (a) presents a chip attached to substrate bond pads by wire bonding, fig. 2-6 (b) shows the solder bump interconnection method. It is observed and also reported that most electronic failures occur at the solder joint and the frequency of failure increases at elevated temperature and with SMCs. Nonetheless, it is reported that by using hybrid microelectronics technology, engineers can increase the maximum operating temperature limit of HTE device up to 250°C with reduced failure. Li, [23] demonstrated the ability to use hybrid microelectronics technology to upgrade the operating temperature of a module from about 177°C to 225°C. This seems to have demonstrated a solution to one of the problems with SMT as it regards the failure of solder joints in SMCs.



(a) Wire bonding process for chip on board (COB)



(b) Solder bumping process for flip chip package

Figure 2-6 Chip attachment process showing the wire bonding process for chip on board (COB) and the solder bumping process for flip chip package

2.3.3.1 Flip chip attachment technique

FC may be attached to a substrate by welding, adhesive bonding and soldering. The welding method includes two processes. These are the thermo-compression bonding and thermosonic bonding processes. While the former uses fluxless process to allow fine pitch connection, the latter uses ultrasonic energy and heat and also lower process temperatures. Adhesive bonding is a low temperature processing method basically applied to processes involving very fine pitch leadfree joints. Soldering could be fluxed or fluxless usually in the presence of solder alloy paste. One major advantage of this process is that it supports processing on SMT assembly line. Recently, soldering is the most widely used interconnection technology in the electronics manufacturing sector. The advance in interconnection technology from wire bonding to solder bumping empowered FCs to have better advantage in electrical performance at high temperature over other microelectronic components used in HTE manufacture due to shortened electrical path. In a typical FC assembly (fig. 2-7), the silicon chip (fig. fig. 2-7(a)) is directly attached face down (flipped) onto a PCB (fig. 2-6(b)) using solder balls attached on the chip which form solder bumps on reflow soldering [18].

In addition to acting as the conductive interconnect, the bumps make electrical connection across the bond pads, provide mechanical support to the die, serve as spacer between chip and the PCB, aid precise positioning of the silicon chip which is vital in packaging microelectronic devices and relieve CTE mismatch stresses in the joint. Although the package has self aligning capability [36], to reduce the challenges inherent in mounting the die precisely for micro-electromechanical systems (MEMS), bond pads are present in both the chip and substrate side of the new version of the device. These bond pads increase the accuracy of lateral positioning of the component challenged during reflow soldering due to solder uncontrollable flow aggravated in the absence of solder mask. The advantages of FC in manufacture of micro-electronic devices include reduced

board real-estate use, shortened electrical path culminating in higher speed and reduced delaying inductance and capacitance issues, rugged interconnection method, low cost, time active alignment and superior noise control. Despite all these advantages, the package still have disadvantages which includes difficulty to inspect, CTE mismatch between die and substrate and difficult to rework. In comparison to wire bonding, it is more difficult to determine which joint has failed in FC assembly. Furthermore, CTE mismatch occasions fatigue failures of the joint. A number of applications use FC device as their component. These include computers, telecommunications, liquid crystal display (LCD), consumer products, portable hand-held devices, medical electronics, smart cards, automotives, sensors (eg image), digital TVs, high brightness Light Emitting Diodes (LEDs), auto electronic control systems, fast Double Data Rate (DDR) memory devices.

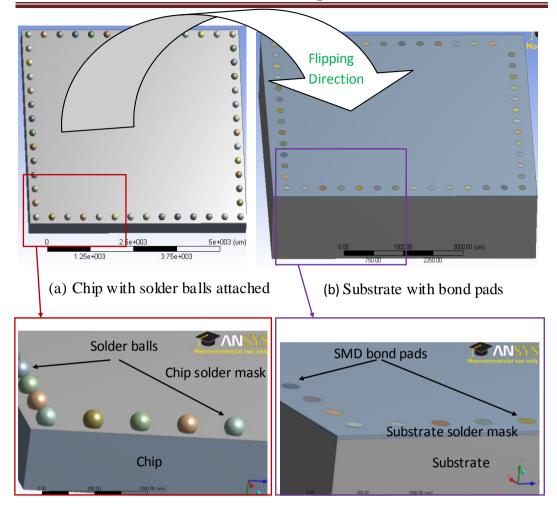


Figure 2-7 Flip chip attachment process showing the chip with solder balls attached and the substrate with bond pads

2.3.4 Interconnection material and derivative

The interconnection material used to make the joints investigated in this study is the solder alloy and its derivative is the IMC. Solders are therefore reviewed for high temperature applications. The contribution of IMC to the integrity of solder joint operating at elevated temperature is also reviewed towards reliability improvement of solder joint at HT excursions.

2.3.4.1 Solders

Many materials including silicon carbide (SiC), used in the manufacture of components, substrates and ceramics substrates, have been reported to possess the capacity for direct insertion (with high reliability operation) in HTHE. The interconnection of components made with SiC to the substrates remains the key challenge.

Although high lead solder (eg 95Pb-5Sn) has melting point of approximately 300°C, the eutectic tin-lead solder alloy (Sn63-Pb37) was the most popular material for soldering process. However, one of its major shortcomings is that it cannot be used for operating temperatures greater than 125 °C since its melting point is about 183 °C. In consequence, it is usually and commonly used in the assembly of consumer and other ambient electronics.

Owing to the ban in the use of lead in electronics by European Union's waste from electrical and electronic equipment (WEEE) directive which came into effect in July 2006, and following the increasing environmental and health concerns over the toxicity of lead combined with strict legislation [5, 14, 37], new lead-free solder alloys have been developed and employed in electronic packaging. Currently, different constitutive compositions exist of the main alloying elements (Sn-Ag-Cu) with their varying melting points (eutectic) temperature. The alloying composition range recommended by the National Electronics Manufacturing Initiative (NEMI) and Soldertec are Sn-3.9Ag-0.6Cu and Sn-[3.4-4.1] Ag-[0.45-0.9] Cu, respectively [5, 38].

Although this Sn-Ag-Cu eutectic solder with melting point temperature of 217°C has been in use for the HTE interconnects operating at temperature up to 150°C,

its thermo-mechanical reliability at this temperature and also higher temperature applications has been a concern. For instance, the fine-grained microstructure developed in lead-free solders may be beneficial from a mechanical fatigue stand point, however it may not be ideal for visco-plastic and creep resistance since creep deformation at the service temperature may be by grain boundary sliding.

Several other constitutive lead-free solders tried at elevated temperatures have either one issue or the other. Among the lead-free solders developed, high melting point 80Au-Sn, Sn-5Sb and Au-Si alloys can withstand HT service conditions up to and above 230°C. Tables 2-1 to 2-3 presents solder compositions and their melting points ranges - from 180°C to 280°C. It may be pertinent to note that these high melting point solders cannot be utilized in a wide range of manufacturing situations due to cost, joint integrity and the degradation of the properties of electronic components caused by HT soldering [37, 39, 40]. Joint integrity is directly related to the stress concentration set-up at the solder joints.

		1	
teAlloy	Composition	Melting	Source
System	(wt %)	Range (°C)	Source
Sn-Zn	Sn-9Zn	198.5(e)	Belmont Metals,
			Indium
Sn-Bi-Zn	Sn-8Zn-3Bi	189-199	Senju Metals
Sn-Bi-In	Sn-20Bi-10In	143-193	Indium Corp.

Table 2-1 Example of lead-free solder alloys melting between Eutectic 180 °C -200°C temperatures

Alloy System	Composition (wt%)	Melting Range (°C)	Source
Sn-Ag	Sn-3.5Ag	221 (e)	Most solder manufacturers
Sn-Ag	Sn-2Ag	221-226	Midco Ind.
Sn-Cu	Sn-0.7Cu	227 (e)	Most solder manufacturers
C. A. D'	Sn-3-5Ag-3Bi	206-213	Nihon Handa
Sn-Ag-Bi	Sn-7.5Bi-2Ag	207-212	Tamura Kaken
Sn-Ag-Cu	Sn-4Ag-0.5Cu	217(e*)	Heraeus
Sn-Ag-Cu-Sb	Sn-2Ag-0.8Cu 0.5Sb	216-222	AIM
Sn-Ag-Zn	Sn-3.5Ag-1Zn	217	AIM

Table 2-2 Example of lead-free solder alloys melting between 200-230°C

*several other compositions close to that quoted also claim to be the eutectic alloy

Alloy System	Composition (wt %)	Melting Range (°C)	Source
Sn-Sb	Sn-5Sb	232-240	Most solder manufacturers
Sn-Au	Au-20Sn	280 (e)	Mitsubishi materials, Indium Corp.

Source of Tables I-III: after Nimmo, K. (1997), "Review of current issues in lead-free soldering", *Proceedings of the Surface Mount International Conference*, San Jose, CA, pp.467-75

2.3.4.2 IMC

Metallurgical reactions between solder and metallised copper bond pad during reflow assembly process and component operations in the field produce and grow respectively inter-metallic compound (IMC) at the interfaces of the bonded materials [41-47]. Fig. 2-8 shows a solder bump with IMC sandwiched between solder bulk and substrate. Sakuma et al. [45] noted that solder balls, very small solder volumes (< 6 microns in height) form IMC in the junctions during the bonding or reflow processes. The contributions of IMC [48] and the CTE mismatch of the bonded structural materials to solder joint integrity are nontrivial. The brittle nature of IMC has been reported by [49, 50] to impact the reliability of solder joints in chip-level devices. In their investigation, Laurila et al. [49], pointed out that due to IMCs' inherent brittle nature and the tendency to generate structural defects, too thick IMC layer at the solder/conductor metal interface may degrade the reliability of the solder joints. For instance, at high temperature operation, the inter-metallics formed at the joint undergo very significant degradation. This degradation is due to thermal stress set up by the incompatible differential nonlinear expansion of the constituent bonded materials in the assembly. This usually results to grain coarsening of the compounds. This metallurgical phenomenon increases the damage of the interconnection.

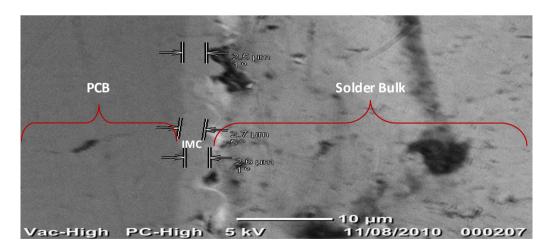


Figure 2-8 Solder bump containing IMC between the PCB and the solder bulk

This challenge posed a huge limitation to its (solder joint) continued use at elevated temperature. Thus there is an urgent need to understand the behaviour of solder joint containing IMC and which operates at elevated temperature. Such indepth knowledge when applied in assembly of components using solder joint will produce high integrity joint which will optimally and reliably perform at elevated temperature. The need for this investigation has prompted this research.

The study of the behaviour of realistic solder joint employing numerical and computer modelling approach has been somewhat difficult in the past. Ridout and Bailey [35] stated that the inter-metallic layer formed between the solder joint and the copper pads is usually ignored in modelling studies, due partly to its size and partly to the lack of material property data. The non incorporation of IMC in the models of solder joints is one possible cause of discrepancy between the predicted and the experimentally determined fatigue life of solder joints [1]. Recently, IMC material property data has been available and current technology in computers has enabled high productivity computing (HPC) required to handle very many elements resulting from the inclusion of very thin thickness of IMC in a geometric model of solder bump.

It is reported by Amalu et al. [11] that solder joint incorporating IMC as a component is a better model than the one without IMC to predict the response of FC assembly to thermal fatigue load. Thus, further study incorporating IMC in the joints of components' models assembly is possible and needed to improve the accuracy of results generated from modelling studies to predict the reliability and fatigue life of solder joints. Such investigation will provide further understanding of thermo-mechanical behaviour of lead-free solder joints in a FC assembly in HTE at elevated temperature excursion characteristic of aerospace and automotive applications as well as well-logging operations.

2.4 Fatigue life prediction

The accurate prediction of reliability of solder joints in safety critical microelectronic products is of huge concern as such joints often fail under thermal fatigue loads. The CTE and stiffness mismatch between the package and the board result in thermal stresses in solder joints during assembly and life operation in the field. The damage caused by these stresses accumulates as the electronic devices are subjected to multiple cycles, ultimately causing failures of solder joints. Although the MTTF of solder joints is adversely affected at HT, however it can be significantly increased if the effects of HT excursions on N_f of the joints are quantified while taken into account the impacts of static structural factors such as IMC and solder bump shape parameters. Contribution of HT excursions to damage of SnAgCu solder joints is critical because the failure of the joint is a function of accumulated plastic damage which increases in magnitude when the joint operates at high homologous temperature (T_h) . The mechanical strength of solders in joint which normally operates at high T_h ambient range of 0.44 to 0.81 deteriorates faster at higher T_h because the properties of solders become more sensitive to plastic strain rate such as creep/visco-plastic deformation. Fig 2-9 shows the relationship between the strength of a metal and its ambient temperature (in Kelvin) expressed as a function of its melting temperature, T_m . The ambient temperature is designated as $T_{a.}$

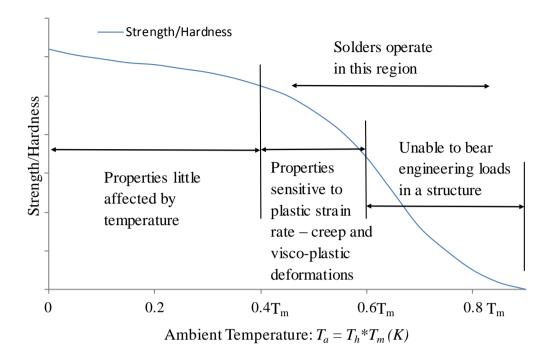


Figure 2-9 Strength of a metal as a function of its melting temperature

To meet the customer's insatiable desire for faster, cheaper, smaller and higher reliability HTE, electronics manufacturing industries need to painstakingly qualify the performance of solder joints in these devices at HT excursion during the design stage. Unfortunately, every component has a unique interconnect reliability which makes it unrealistic in terms of cost and time to carry out testing for every singular COB model. The situation is even made complex considering that other static structural factors also influence the response of the joints of the components to plastic deformation. Virtual laboratory offers promise to overcome this challenge. ATC is used to simulate the operational service conditions of the assembled COB in the laboratory. Simulation tools are employed in life prediction models utilised in virtual qualification of solder joints without extensive model testing. The basic assumption for life prediction model is that the damage in solder joints during temperature cycling is primarily due to steady state creep/visco-plastic strain accumulation.

Constitutive life models are first used to capture the magnitude of plastic deformation of SnAgCu solder alloy before this value is input into the life prediction models. The constitutive relations are either creep or visco-plastic base damage models. Although visco-plastic damage model proposed by Anand, which is widely accepted, is used in this study, a review of both damage models is presented.

2.4.1 Constitutive model for SnAgCu solder

Two constitutive models of SnAgCu are reviewed. These are the creep and the visco-plastic models.

2.4.1.1 Creep models

Four creep models are reviewed in this sub-section.

Schubert et al. [51] proposed the constitutive relation for SnAgCu solder given in equation (2-1).

$$\varepsilon_{cr} = A_1 [\sinh(\alpha\sigma)]^n exp\left(\frac{-H_1}{kT}\right)$$
(2-1)

Where $A_1 = 277984s^{-1}$, $\alpha = 0.02447$ MPa⁻¹, n = 6.41, $H_1/k = 6500$, E (MPa) = $61251 - 58.5T(^{\circ}K)$, CTE = 20.0ppm/K, Poisson's ratio = 0.36. Syed [52] reported that Schubert et al. [51] combined data from different sources and from their own testing on different compositions of SnAgCu solder (Sn3.8Ag0.7Cu, Sn3.5Ag0.75Cu, Sn3.5Ag0.5Cu, and CastinTM); identified two regions for stress-strain rate behavior, but postulated the high stress region as power law break-down region, and chose hyperbolic sine function to represent creep data.

In their work, Wiese et al. [53] represent the steady state creep behaviour using double power law model given in equation (2-2).

$$\dot{\varepsilon}_{cr} = A_1 exp\left(\frac{-H_1}{kT}\right) \left(\frac{\sigma}{\sigma_n}\right)^{n_1} + A_2 exp\left(\frac{-H_2}{kT}\right) \left(\frac{\sigma}{\sigma_n}\right)^{n_2}$$
(2-2)

Where $A_1 = 4X 10^{-7} s^{-1} A_1$, $H_1/k = 3223$, $n_1 = 3.0$, $A_2 = 10^{-12} s^{-1}$, $H_2/k = 7348$, $n_2 = 12$,

 $\sigma_n = 1$ MPa, E (MPa) = 59533 – 66.667T (°K). They studied the creep behaviour of bulk, PCB sample and FC solder joint samples of Sn4.0Ag0.5Cu solder and identified two mechanisms for steady state creep deformation for the bulk and PCB samples.

Zhang et al. [54] modelled the steady state creep behaviour using hyperbolic sine function presented in equation (2-3) which postulates power law break-down at high values of stress. The model is converted to tensile form [52].

$$\varepsilon_{cr} = A_1 [\sinh(\alpha\sigma)]^n exp\left(\frac{-H_1}{kT}\right)$$
(2-3)

Where $A_1 = 143.4 \text{ s}^{-1}$, $\sigma = 0.108 \text{ MPa}^{-1}$, n = 3.7884, $H_1/k = 7567$, E (MPa) = 24224 - 0.0206 (°K). They generated their data on single lap shear specimen of Sn3.9A g0.6Cu solder alloy.

Morris et al. [55] employed double power law constitutive relation to represent creep data generated from single lap shear specimens of Sn3.0Ag0.5Cu solder joints. They suggested stress exponents of 6.6 and 10.7 for the low and high stress regions. Thus: $H_1/k = 11425$, $n_1 = 6.6$, $H_2/k = 9020$, $n_2 = 10.7$ G (MPa) = 27360 - 40.5T (°K)

2.4.1.2 Visco-plastic model

In actual usage conditions, the temperature cycle duration of solder joint is in the order of minutes to days and the homologous temperature is within the creep region. Therefore, solder joints formed using SnAgCu alloy solder are presumed to deform primarily due to creep. Creep models are used to simulate the behaviour of materials over a relatively long period at low strain. Thus, many researchers have used creep models to capture the rate-dependent plasticity of the solders in the joints. Unfortunately, this condition of low strain over a long period cannot be modelled exactly in the laboratory due to time and cost implications. ATC and HATC are utilised instead. At high temperature excursions, the solder joint is at elevated temperature and solder physical behaviour becomes very sensitive to strain rate, temperature, strain hardening and softening.

Anand proposed a model to predict the behaviour of metal being hot-worked. Although the Anand's model was originally developed for the metal forming applications [56-58], it is however applicable to general applications involving strain and temperature effects, including but not limited to solder joint analysis and high temperature creep. It is proposed and believed that the systematic effects of all complex factors which influence damage of solder joints may be better accounted in and modelled using Anand's visco-plasticity [56-58].

The advantage of this model is that it is categorised into the group of the unified plastic models where the inelastic deformation refers to all irreversible deformation that can not be simply or specifically decomposed into the plastic deformation derived from the rate-independent plasticity theories and the part resulted from the creep effect. In comparison to the traditional creep approach, the Anand's model introduces a single scalar internal variable "*s*", called the

deformation resistance, which is used to represent the isotropic resistance to inelastic flow of the material.

Constant	Parameter	Value	Definition
C1	S _o (MPa)	39.09	Initial Value of Deformation Resistance
C2	Q/R (1/Kelvin)	8930	Activation Energy/ Boltzmann's Constant
C3	A (1/Sec)	22300	Pre-Exponential Factor
C4	ξ (Dimensionless)	6.0	Multiplier of Stress
C5	m(Dimensionless)	0.182	Strain Rate Sensitivity of Stress
C6	h _o (MPa)	3321.2	Hardening/Softening Constant
C7	Ŝ (MPa)	173.81	Coefficient for Deformation Resistance saturation value
C8	n(Dimensionless)	0.018	Strain rate sensitivity of saturation value
C9	a (Dimensionless)	1.82	Strain Rate Sensitivity of Hardening/Softening

Table 2-4 Constants in Anand's constitutive model for SnAgCu solder [48]

.

The flow equation (2-4) represents the Anand's constitutive model whose parameters are defined in table 2-4.

$$d^{p} = Ae^{\left(-Q/RT\right)} \left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m}$$
(2-4)

Other parameters associated with the model and which are not defined in table 2-4 such as d^p , *R*, *T* and σ are effective inelastic deformation rate, universal gas constant, absolute temperature and effective Cauchy stress respectively. The evolution of "*s*", is described by:

$$\dot{s} = \left\{ sign\left(1 - \frac{s}{s^*}\right)h_0 \left|1 - \frac{s}{s^*}\right|^a \right\} d^p$$
(2-5)

 s^* is the saturation value of "s" associated with a given temperature and strain rate pair and it is described by equation (2-6) and \hat{S} is a coefficient for saturation.

$$s^* = \hat{S} \left[\frac{d^p}{A} e^{(Q/RT)} \right]^n \tag{2-6}$$

2.4.2 Life prediction model

The models proposed for predicting the fatigue life of solder joint under temperature cycle load may be divided into six main categories. The division is based on the fundamental mechanism presumed to induce damage and drive the failure. These six categories are based on accumulation of the following: stress, visco-plastic strain, creep strain, strain energy, strain energy density and damage. However, most of these equations are developed for leaded solders and only recently Schubert, et al. [51], Zhang et al. [54] and Syed [52] proposed models for SnAgCu solder. Among this list, reference [52] appears to be the most widely accepted and easier to apply too. The model is therefore discussed further in details.

For a single creep mechanism, Syed [52] proposed the equations (2-7) and (2-8) which involve cyclic fatigue creep:

$$N_f = (C'\varepsilon_{acc})^{-1} \tag{2-7}$$

Where N_f is the number of repetitions or cycles to failure, $C' = 1/\varepsilon f$ is the inverse of creep ductility and ε_{acc} is accumulated creep strain per cycle. Moreover,

$$N_f = (W' w_{acc})^{-1} (2-8)$$

Where N_f is the number of repetitions or cycles to failure, W' is the creep energy density for failure and w_{acc} is accumulated creep energy density per cycle.

For two creep mechanisms such as equation (2.2), the equations (2-7) and (2-8) translate to:

$$N_f = (C_1 \varepsilon_{acc}^I + C_{II} \varepsilon_{acc}^{II})^{-1}$$
(2-9)

and

$$N_f = (W_1 w_{acc}^I + W_{II} w_{acc}^{II})^{-1}$$
(2-10)

For models (2-7 to 2-10) to be utilised, it requires that constants C', C_I and C_{II} for creep strain based models and W', W_I , and W_{II} for dissipated creep energy density based model be determined. Normally, the life prediction model parameters are determined using the actual test data generated by measuring the N_f during temperature cycle tests, and some way of quantifying the strain or strain energy density during the temperature cycle. Based on the results of his experiment and the constitutive relations he used, Syed [52] proposed the models in table 2-5 with values of the constants.

S/No	Constitutive	Predictive Creep	
	model	fatigue life model	Model
1	Double power	Partitioned Acc. strain	$N_f = (0.106\varepsilon_{acc}^{l} + 0.045\varepsilon_{acc}^{ll})^{-1}$
2		Total Acc. strain	$N_f = (0.0468\varepsilon_{acc})^{-1}$
3		Creep energy density	$N_f = (0.0015 w_{acc})^{-1}$
4	Hyperbolic	Acc. Creep strain	$N_f = (0.0513\varepsilon_{acc})^{-1}$
5	Sine	Creep energy density	$N_f = (0.0019 w_{acc})^{-1}$

Table 2-5 Creep fatigue life models for SnAgCu by Syed [52]

It what mentioning that Stoyanov et al. [59] in a similar study to find N_f of FC solder, used 0.0014 as value of W'. They obtained the value by fitting a linear regression model to a set of experimental data and assumed that the solder creep behaviour is modelled using the hyperbolic sine constitutive equation [52, 59].

2.5 Summary

This chapter has presented a review of literature from a number of studies whose investigations centred on HTE and the reliability of assembled component solder joint used in its assembly. The information from the literature review was utilised in the formulation of the research problem which the study attempts to address and the knowledge gained was also employed in designing this research work.

The challenge of solder joints of micro-electronics which operates at hightemperature ambient is also presented. The desire for the solder joint of miniaturised component to operate reliably in this environment is much anticipated. These have formed the basis to select FC assembly for this study.

The review highlighted that the reliability of HTE modules is still a concern. It also points out that its market will continue to grow due to the fact that it increasingly finds applications in sectors and systems where it replaces pneumatic and hydraulic devices and modules. Greater application of HTE has been in the range of 150 °C to 250°C. Solder joint was identified as the most susceptible to failure in HTE assembly. The causes of this failure, the site and the mode reported in literature were reviewed. The review on interconnection materials and derivative identified lead-free solders suitable for high-temperature applications and recognised that SnAgCu solder is an ideal for operations below 160°C considering cost and availability. Thus, SnAgCu alloy solder was selected for this study. An identification of the significant contribution of the thickness of IMC at elevated temperature to the reliability of solder joint operating in such ambient was made through the review. Consequently, research questions were formulated to investigate this assertion further and the geometric models of solder joint utilised in the investigation reported in this thesis contain IMC. The review also shows that visco-plastic model could be a better model than creep in capturing the plastic deformation in the solder joint at high-temperature excursions. On this basis, the Anand's visco-plastic model was employed to simulate the behaviour of the SnAgCu solder alloy in this study. Furthermore, the review revealed that Syed model is one of the most widely accepted and used to predict fatigue life of leadfree solder joint. Although the model was developed for creep constitutive model of solder joint, it was adapted in Anand's visco-plastic model and utilised in this investigation.

Chapter 3: Solder Joint Shape Prediction and FEM

CHAPTER 3

PREDICTION OF SHAPE OF FLIP CHIP SOLDER BUMPED JOINT AND INTRODUCTION TO FINITE ELEMENT MODELLING (FEM) OF ITS ASSEMBLY

3.1 Introduction

The details of the derivation of geometric model of the FC solder bump and subsequently its creation as well as the application of finite element modelling to study its reliability are presented in this chapter. The profile of the bump joint is created using a combination of analytical method and construction geometry. The geometry creation was done in ANSYS design modeller which is compatible with parametric ANSYS script that allows the change of parameter of the model with ease. The major advantage of this method of joint creation is that it allows layer of IMC thickness to be included in the joint. The results show that the inclusion of this layer increases the accuracy of simulation results. This model creation method also aids parametric studies on the static structural analysis of the assembly configuration by providing a platform to vary the design parameters easily.

This chapter discusses the background of the simulation. It also discusses the FEM methodology in the subsequent section. It further outlines the mechanical properties of assembly materials and presented models employed to describe materials behaviour under temperature load. The details of the applied thermal load and specification of the boundary conditions are also provided. It ends with a summary of the presentations in this chapter.

3.2 Solder bump model derivation and creation

Previously, many researchers including Hsu and Chiang [28] and Ladani and Razmi [32] determined solder ball geometry exclusively using surface evolver software tool based on energy method. In their study, Chiang and Yuan [60], Sidharth and Natekar [61] and Yeung and Lee [62] used both surface evolver and analytical methods to predict solder bump geometry. In the model creation in this study, the solder bump geometries were determined using a combination of truncated sphere theory, the force-balanced analytical method and ANSYS software design modeler (DM). The function describing the shape of the bump was derived using the structure in Fig. 3-4 - a double truncated sphere model. Prior to mounting, the model was a truncated sphere, Fig. 3-2(c), where $d_{(-z)} = h_0 = 140 \mu m$ (Refer to table 3-2 and fig. 3-2 (C)).

If $h_0 + y = 2R_c = \emptyset$, where h_0, y, R_c and \emptyset are ball height, vertical distance in z direction, ball centre radius and diameter respectively, then:

at $d_{(-z)} = \frac{h_0 + y}{2}$,

 $R_z = R_{(\frac{h_0 + y}{2})} = R_c = 89 \,\mu\text{m} \cdot R_c$ is also the diametric radius.

From truncated sphere theory, equation (3-1),

$$h_{0} = R_{c} + \sqrt{R_{c}^{2} - R_{h}^{2}}$$
(3-1)
$$R_{h} = \sqrt{R_{c}^{2} - (h_{0} - R_{c})^{2}}$$
(3-2)

Where R_h is the radius of Cu pad at die bond pad interconnect. Eq. (3-2) and parameter values in table 3-2 were used to compute the diameter of bond pad at interconnect as 146 µm. Force-balanced analytical theory and DM were used sequentially to compute the values of the two unknown parameters in Eq. 3-10 height (*h*) and radius of the arc (R_{arc}) – after mounting and reflow soldering of the assembly. The algorithm is based on many assumptions reported in [60]. These assumptions are:

- the solder joints attain static equilibrium when solidification occurs;
- the solder pads on the substrate are circular and are perfectly aligned during solidification;
- the free surface of the solder joint is axisymmetric;

- the meridian defining the free surface of the solder joint is approximated by a circular arc;
- the solder pad is completely covered by solder and the solder does not spread beyond the pad;
- the solder pad is perfectly wettable, and the surrounding materials are perfectly non-wettable

The governing equation of static structural equilibrium of forces is:

$$P_0 = P_a + \gamma \left(\frac{1}{R_1} + \frac{1}{R_2}\right) + \rho g(h - z)$$
(3-3)

Pressure (P) and radius (R) are functions of height such that:

$$p_{0,a} = p_{(z)} \text{ and } R_{1,2} = R_{(z)}$$
 (3-4)

Where R_1 and R_2 are the principal radii of curvature of the solder surface at height, h and P_0 , P_a and Y are internal pressure, ambient pressure and surface tension respectively. The line of action of R_{2h} is perpendicular to that of Y.

For simplicity, the FC weight can be assumed negligible and $g \rightarrow 0$ such that equation (3) reduces to:

$$P_0 - P_a = \Upsilon\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$
 (3-5)

In axisymmetric case, the equilibrium equation is [60]:

$$\Upsilon R R'' - \Upsilon (R')^2 + P R [1 + (R')^2]^{3/2} - \Upsilon = 0$$
(3-6)

The *R* defines the profile of solder free surface and R'' and R' are derivative of *R*.

For equilibrium of forces acting at the plane surface at height, h:

$$\frac{1}{n}W_{Die} = -2\pi R_h \Upsilon \sin(\pi - \theta_h) + P_h \pi {R_h}^2$$
(3-7)

Where W_{Die} is the weight of the FC, *n* is the number of balls of the die and θ_h is the obtuse angle the surface tension makes with the upper bond pad plane. The coefficient of W_{Die} represents the share weight component a ball experiences in supporting the FC die.

The solder volume is defined as:

$$V = \pi \int_{0}^{h} (R)^{2} dz$$
 (3-8)

In a similar study, Heinrich et al. [63] approximated the meridian defining the joint's contour free surface, R_z , to a circular arc, R_{arc} . Employing this approximation, the volume and unbalanced force are expressed as:

$$V = \pi \int_0^h [R_{arc}(z)]^2 dz$$
 (3-9)

and

$$\delta F = \frac{1}{n} (W_{Die}) - \frac{\pi R_h}{2hR_{arc}} \left[\pm (R_0 + R_h) - \sqrt{\frac{4R^2 arch^2}{(R_0 + R_h)^2 + h^2}} - h^2 \right] for \begin{cases} h_0 \le 140\\ R_{arc} \le 178 \end{cases}$$
(3-10)

It is also assumed that a reflowed FC on a PCB assembly is in static equilibrium and thus $\delta F = 0$ in equation (3-10). An ideal configuration of $R_0 = R_h$ was chosen for this investigation because variation in the size of bond pads diameter of die and substrate impacts solder joint reliability. This is discussed in details in chapter 5. Determination of the values of R_{arc} and h parameters in equation (3-10) for which $\delta F = 0$ was done through a combination of numerical and construction geometry approaches. The computation started with maximum initial guess for h_0 , R_{arc} equal to 140 μm , 178 μm , respectively and run for several iterations in an excel spreadsheet. Optimal solution was reached at $h \approx$ 120 μm and $R_{arc} \approx$ 148.82 μm . As a check, these values were used to create the model in DM whose volume was read-off. This volume has to be the same with the initial volume of the ball before mounting when $d_{(-z)} = h_0 = 140 \mu m$. To verify this methodology, some models (fig. 3-1) with different parameter settings were created in this way and some observed slight volume deviations between the computed initial volume and created model volume (in DM) were corrected via further iteration trials in the DM. The values of the model parameters were reintegrated back into the iteration tool for validation. A major deviation was recorded in parameter settings of S/N 2 in table 3-1. The table 3-1 presents the bumps configuration in S/N 1 to 8. The optimal values of the solder bump shape parameters $(n, h, R_o, R_h, R_{arc} \text{ and } \frac{1}{n} W_{Die})$ used in this study are (48, 120 µm, 73 µm, 73 µm, 148.8 µm and $1.2X10^{-5}N$) respectively. The mass of FC was determined by weighing using an electronic balance called Ohaus Analytical plus and its weight, W_{Die} equal to 5.891 * 10⁻⁴N, was computed. This equipment has a measuring accuracy of 10^{-9} g. The improvement provided by this approach lies in the use of principle of truncated sphere theorem and force-balanced analytical method to develop the expression (Eq. 3-10) for FC solder bump architecture; and the involvement of DM to determine values of the two parameters of Eq. 3-10. This approach has the capacity to reduce the time and magnitude of computation involved when analytical method is applied alone through the involvement of DM.

	Table 3-1 Generated bump profile																		
S/N	h	\mathbf{R}_{0}	$R_{\rm h}$	Rarc	h^2	Rarc^2	Ro+Rh	(Ro+Rh)^2	22*Rh/14*h*Rarc	4*F*E	H+E	J/K	L-E	M^0.5	G-N	I*O	W/48	Rarc (Drawing)	D0
0	140	0.0	73	89.0318	19600	7926.661	73.0	5329.00	0.009203	6.21E+08	24929.00	24928.81	5328.81	72.9987	0.001315	1.21031E-05	1.2E-05		0.0
1	130	58.4	73	131.4067	16900	17267.72	131.4	17265.96	0.006715	1.17E+09	3416596	3416552	17265.52	131.3983	0.001659	1.11409E-05	1.2E-05	126	116.8
2	126	65.7	73	139.3391	15876	19415.38	138.7	19237.69	0.006534	1.23E+09	35113.69	3511322	19237.22	138.6983	0.001707	1.11553E-05	1.2E-05		131.4
3	120	73.0	73	148.8156	14400	22146.08	146.0	21316.00	0.006424	1.28E+09	35716.00	35715.49	21315.49	145.9982	0.001753	1.12636E-05	1.2E-05		146.0
4	114	80.3	73	160.073	12996	25623.37	153.3	23500.89	0.006286	1.33E+09	36496.89	36496.40	23500.40	153.2984	0.001605	1.00876E-05	1.2E-05		160.6
5	107	87.6	73	174.0236	11449	30284.21	160.6	25792.36	0.006161	1.39E+09	3724136	37240.74	25791.74	160.5981	0.001928	1.18763E-05	1.2E-05		175.2
6	101	94.9	73	190.055	10201	36120.9	167.9	28190.41	0.005976	1.47E+09	38391.41	38390.81	28189.81	167.8982	0.001787	1.0678E-05	1.2E-05		189.8
7	94	102.2	73	210.2696	8836	44213.3	175.2	30695.04	0.005804	1.56E+09	39531.04	3953033	30694.33	175.1980	0.002027	1.17666E-05	1.2E-05		204.4
8	88	109.5	73	233.238	7744	54399.96	182.5	3330625	0.005589	1.69E+09	4105025	4104953	33305.53	182.4980	0.001984	1.10862E-05	1.2E-05		219.0

Chapter 3: Solder Joint Shape Prediction and FEM

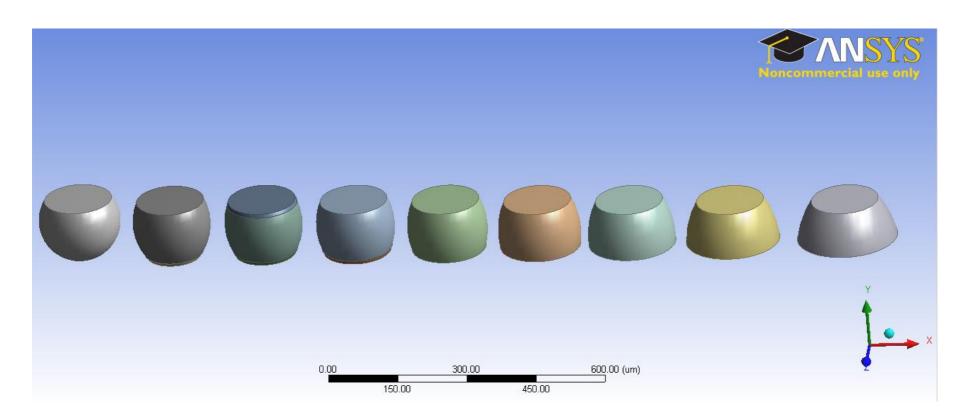


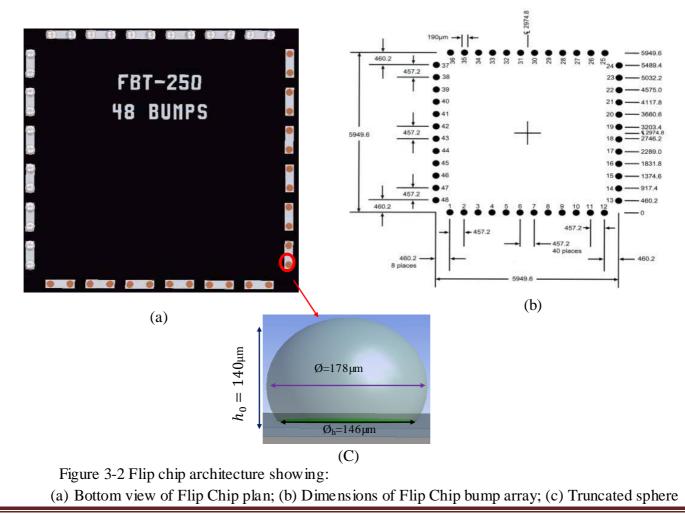
Figure 3-1 Solder ball and bump profile

3.3 Assembled flip chip architecture

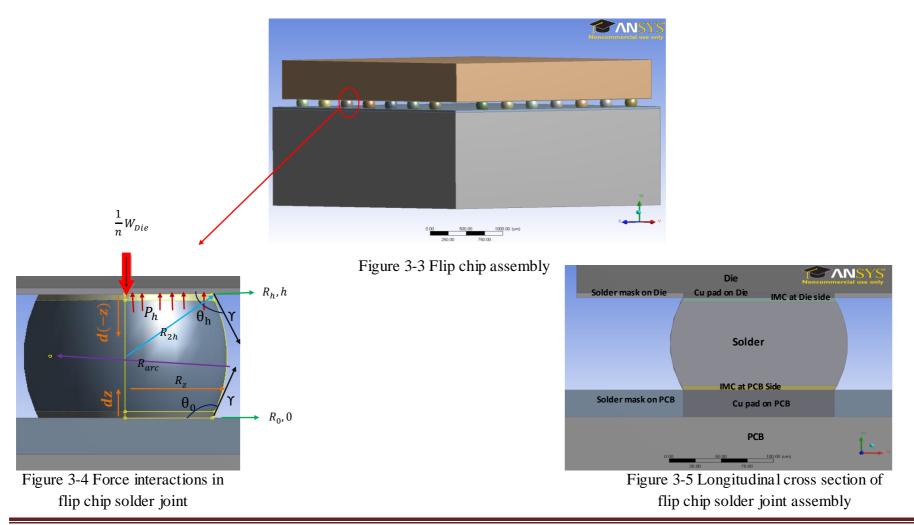
Fig. 3-2 shows the FC architecture where fig. 3-2(a) illustrates the attachment of the ball grid array (BGA) to the die in a daisy chain layout, while fig. 3-2(b) presents the dimensions of the BGA matrix and fig. 3-2(c) is a representation of a singular ball mount. Table 3-2 depicts the FC parameters whose assembly is represented in fig. 3-3 and fig. 3-4 is the magnified structure of one of the joints showing force interactions when the FC is mounted on a PCB using reflow soldering process. Fig. 3-5 is a longitudinal cross-section of the joint assembly.

Bumps	Bump Matrix	Pitch	Die Size (mm)	Bump Size Height & Diameter	Tray quantity	Pb-Free Lead Free SAC - Sn/Ag/Cu Order Number	Ref	Quick View
48	12*12 Perimeter	18mil 457µm	6.3mm	140μm ø178μm	25pcs Waffle 2"	FC48D6.3C457- DC	FBT250	FET-255 43 FED'5

Chapter 3: Solder Joint Shape Prediction and FEM



Chapter 3: Solder Joint Shape Prediction and FEM



3.4 Finite element modelling (FEM)

The FEM method employed in this study is discussed under three main headings. The first discussion is centred on the background and the FEM methodology. The models used to simulate the response of the materials to the applied thermal load were presented and discussed subsequently. This section ends with the specification of the applied temperature load and boundary conditions.

3.4.1. Background and methodology

FEM method is widely used to study and predict the reliability of FC solder joints in field operations. Determining the behaviour of the system via simulation complements experimental investigation especially in solder joint reliability analysis where plastic work, strain energy and strain energy density magnitudes need to be generated from numerical modelling and fed into a fatigue life model. A three-dimensional representative solid model of the FC assembly after reflow is built into the finite element analysis code. The commercial finite element package (ANSYS V.13) was used in the studies reported in this thesis. The high productivity computing (HPC) involved in the course of carrying out this research work was done by a Work Station Server Computer resident at the Electronics Manufacturing Engineering Research Group (EMERG) laboratory. A quarter of the realistic model with mesh is modelled. The advantage of symmetry of the structure was harnessed and only a quarter of the device need be modelled. Since the result of finite element modelling is mesh sensitive, appropriate mesh achieved through body sizing methods were employed.

3.4.2. Materials and their properties

The three-dimensional geometric model of the FC assembled on a PCB is a composite structure comprising many materials of diverse properties. Basically, three material models were utilised to characterise the materials in the assembly. PCB and SnAgCu alloy solder are assumed to be orthotropic and visco-plastic respectively and all other materials are assumed to be linear elastic and isotropic in nature. These materials and their properties are presented in table 3-3.

S/No	Component	Young's Modulus (GPa)			C.T.E (ppm/ ⁰ C)			Poisson Ratio			Shear Modulus (GPa)		
Ś	Com	E_{x}	E_y	$\mathbf{E}_{\mathbf{z}}$	$\alpha_{\rm x}$	α_y	$\boldsymbol{\alpha}_z$	ν_{xy}	ν_{xz}	ν_{yz}	G _{xy}	G _{xz}	G_{yz}
1	Die[25]	130			3.30			0.28			50.8		
2	Mask[64]	4.14			30.0			0.40			1.48		
3	Cu Pad[65]	129			17.0			0.34			48.1		
4	SnAgCu[59]	43			23.2			0.30			16.5		
5	Sn-Cu IMC[45]	110			23.0			0.30			42.3		
6	PCB[66]	27	27	22	14	14	15	0.17	0.2	0.17	27	22	27

Table 3-3 Mechanical properties of assembly materials

3.4.3. Thermal load and boundary conditions

Guided by other previous works in reliability modelling of solder joints and in a desire to explore the system behaviour over relatively long duration of temperature loading, six complete thermal cycles between -38°C and 157°C in 25 load steps were used in the simulations of the work reported in this thesis. The loading started from 22°C (room temperature), ramped up at 15°C/min (market environmental condition and IEC standard 60749-25 in parts) [67, 68] to 157°C where it dwelled for 10 minutes and ramped down to lower dwell region at the same rate where it also rested for 10 minutes.

The FC assembly (fig. 3-3) was simply supported and its conditions at the supports are:

at symmetric surfaces (-x,z),
$$u_{(-x)} = u_{(z)} = 0$$
 (3-10)

at PCB base,
$$y = 0$$
 and $u_{(y)} = 0$ (3-11)

such that the assembly observed plane volumetric deformation. Where $u_{(x)}$, $u_{(y)}$, $u_{(z)}$ represent displacement in x, y and z directions respectively. Assumptions which aided simplification of this structure for finite element analysis include:

- The assembly was at stress free state at room temperature of 22°C which was also the starting temperature of the thermal loading.
- The assembly is at homogeneous temperature at load steps and maintains thermal equilibrium with the ambient.
- Initial stresses (may be from reflow soldering process) in the package was neglected.
- All contacting surfaces were assumed to be bonded with perfect adhesion.

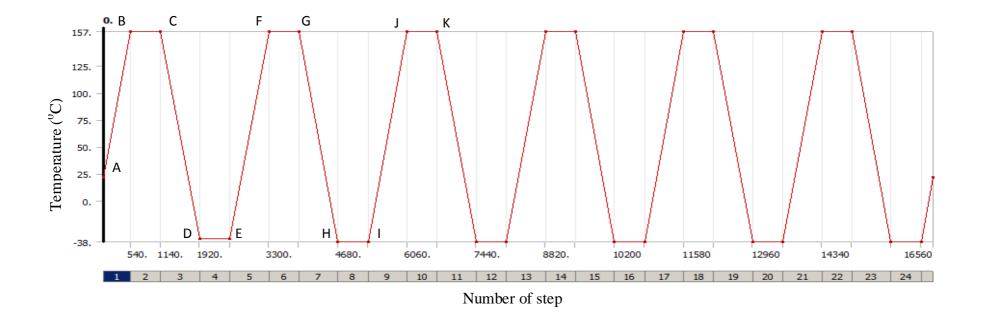


Figure 3-6 Plot of temperature profile of thermal load test condition used in flip chip numerical test

3.5 Summary

This chapter has presented a prediction method and THE methodology developed in this investigation which combines analytical and construction geometry to determine realistic solder bump joint shape. It is argued that the method and model is capable of reducing time and amount of computation involved when analytical methods are employed alone in the determination and creation of the geometric model through the involvement of construction. A huge advantage of this model and method is that it allows the incorporation of IMC in the geometric model of solder bump joint with ease. The generic method and procedure of the FEM employed to simulate the work presented throughout the chapters of this thesis is also outlined.

CHAPTER 4

EVALUATION OF THE RELIABILITY OF REALISTIC AND UNREALISTIC FLIP CHIP SOLDER JOINTS AT HIGH-TEMPERATURE APPLICATIONS

4.1 Introduction

As miniaturisation of electronics modules advances and the usage of FC in assembly of HTE increases, the reliability concern of solder joints in the assembly has increased due to their high mortality rate recently. The reliability of HTE devices in operation is directly affected by the static structural integrity of the joints of assembled FC component used in their assembly. The integrity of solder joint depends to a large extent on the IMC formed at the joint.

Extensive studies which focus on the improvement of solder joint reliability have been carried out both experimentally and numerically. Some discrepancies on the predicted life of the interconnect using FEM and determined life by experiment have been observed in most cases. Unfortunately, most of the geometric models of solder joints utilized in these studies do not contain IMC. Majority of the studies assume that IMC is too thin in thickness to have significant contribution to solder joint damage, and consequently do not incorporate it in their models. This assumption is inappropriate and could yield inaccurate data in simulation output which leads to wrong interpretation of results. This condition may develop because it is widely known that an IMC layer is always formed at the interface of tin-based solder and metallised copper bond pad. Another reason for exclusion of IMC in the geometric model is that meshing such small layers usually results in very large models which requires high-performance computing (HPC) with computers of very large memories and disc spaces. These high specification computers were not readily available. A further reason for non inclusion is the lack of availability of data on the properties of IMCs. To increase the accuracy of prediction of solder joints failure for safety critical operations, better understanding of the contribution of IMC to solder joint damage is needed.

This chapter presents an investigation of the visco-plastic behaviour of solder joints of two models of a flip chip FC48D6.3C457DC mounted on a PCB via SnAgCu solder and which were subjected to the same temperature load conditions. The Anand's model was employed to capture the plastic deformation of solder in the joints while the performances of other materials of the assembly are simulated with appropriate material models. While the bumps of one of the models are realistic with 6 μ m thickness of IMC at interconnects of solder and metallised bond pad, the other is made up of conventional bumps without IMC at their interconnects. The solder bump profiles were created using a combination of analytical method and construction geometry (see chapter 3). The assembled package on PCB was subjected to ATC using IEC standard 60749-25 in parts.

A key contribution of this study is the finding that incorporating IMC in the geometric model of solder joint leads to an improvement from the 25% accuracy of fatigue life prediction achieved in most existing models to 23.5%. It is also found that the IMC sandwiched between bond pad at chip side and solder bulk is the most critical and its interface with solder bulk is the most vulnerable site of damage. Proposition is made that non inclusion of IMC in geometric model of solder joint composed of tin-based solder and metallised copper bond pad causes discrepancy between its fatigue life predicted using FEM and determined by experiment.

The incorporation of IMC in the solder joint geometric models means that new material models will be developed for accurate acquisition of accumulated damage in the solder bump. In addition, the existing life prediction models will be inadequate and have to be modified accordingly. Accurate prediction of life of solder joints in modules has huge benefits to mission safety critical sectors. In general, it will indicate time for preventive maintenance/replacement

(MTTF/MTBF) of these devices to avoid untimely breakdown. Accidental failure of these devices may result in undesirable loss of material and/or life.

The IMC material property data has been made available recently and high productivity computers are also in existence. Thus, further study incorporating IMC in FC solder joints is possible. This investigation will provide further understanding of thermo-mechanical behaviour of lead-free solder joints in a FC assembly in HTE at elevated temperature excursions characteristic of aerospace and automotive applications as well as oil-well logging operations.

4.2 Methodology

FEM discussed in section 3.4 was employed in the investigation. The Anand's visco-plastic model also discussed in section 2.4.1.2 was utilised to capture the solder plastic deformation in the joints of the FC assembly (fig. 3-3) which was loaded and bounded as discussed in section 3.4.3. Each bump of the FC (fig. 3-5) was divided into three portions to mark off two segments at interconnects. These marked off portions are IMC in the model containing IMC or solder in the model not containing IMC. The thickness of each segment is 6µm because Sakuma et al. [45] and George et al. [69] reported that IMC can grow up to this magnitude with time and in high soak temperature. In a similar study, Xu et al. [41] reported a similar situation. This condition is typical of those experienced by HTE. The 6 µm thickness material in contact with copper bond pad on the die is named "region 1", the same thickness in contact with the copper bond Pad on PCB is "region 3" while the central part is "region 2". In figure 3-5, IMC at die side, solder bulk and IMC at PCB side are region 1, region 2 and region 3 respectively. The partitioning into three regions allows for detailed study of strain distributions along the longitudinal axis of the joints as well as shear force at interconnection boundaries. The joint assembly is simply called a bump. Our investigation was carried out in two modules named "Solder only" and "Solder+IMC" under the same conditions. While in solder only module, all regions of the bumps are made of solder; solder+IMC has its regions 1 and 3 made of IMC and region 2 solder.

4.3 Results and discussion

The results and their discussion are carried out in five sub-headings. These sections are study on equivalent plastic strain of the bump, the effect of IMC on solder joint plastic strain behaviour and study on plastic work of the FC solder joints. More results which were also discussed are the study on strain energy of the FC bump joint and the effect of IMC on solder joint fatigue life prediction.

4.3.1 Study on bump equivalent plastic strain

Plastic strain impacts the reliability of FC assembly and this research work investigates this impact in the two types of solder bump described in section 4.2. The depiction of the plastic strain damage distribution on the critical corner solder bumps of the modelled quarter symmetry of the assemblies is shown in fig. 4-1. Comparison of fig. 4-1(a and b) shows the effects of IMC on plastic response of the solder joints. It can be seen that fig. 4-1(a) has a maximum damage at the interconnect between IMC at PCB side and solder region 2. A comparative study of figs. 4-1 (c and d) also shows that strain distribution exist along the longitudinal axis of the bump. Graphical plots in figs. (4-2 to 4-4) are the read out points of plastic strain on solder bump and regions over load step. In figure 4-2, the thermal cycle history, with vertical axis as secondary axis, was superimposed on the plot to aid explanation. These plots show that SnAgCu alloy solder joint experiences volumetric plastic deformation. The rate of change of this deformation (also known as strain rate) is quite dependent on the composition of the bump and thus is different in the two compositions under investigation.

The plot in fig. 4-2 shows a significant difference in plastic strain response in the two different solder joint compositions. The trend in solder only joint demonstrates ductile deformation. The bump records the highest plastic strain rate in the first cycle and higher in the second. It then stabilises in the third into steady state for the rest of the cycle. A sharp increase in plastic strain is observed at first ramp down load from step two to three. Another sharp increase is observed in second upper dwell region corresponding to cycling from step five to six with peak at step six. These are recognised as critical load steps and determine the degree to which plastic strain is induced in the solder material. The phenomenon observed in the first two cycles could be regarded as thermal shock. Solder materials under this condition could have strain hardened and thus stabilised through stress relaxation at the onset of third thermal cycle. Furthermore, these results indicate that ramp down rates and upper dwell time of first and second cycles respectively are crucial parameters in ALT and HALT of solder joints. Since it is a general knowledge that failure of solder joint is caused by the average (till device failure) of accumulated plastic work per cycle, it may be inappropriate therefore to use few thermal cycles in modelling the behaviour of solder joints as observed in many works in the past. Bumps composed of Solder+IMC do not appear to experience thermal shock and although it attains stability with fairly constant homogeneous amplitude of deformation in the third load step, the difference between the second and the rest cycle is only marginal. The deformation amplitude is higher in solder+IMC than in the other. It can be inferred that fatigue failure mechanism is predominant in this type of joint than in the solder only configuration.

Plot of equivalent plastic strain over the load step of region 2 for the two cases is depicted in fig. 4-3. The trend of deformation in this region is the same as that of fig. 4-2. The deference in magnitude exists between the two. Since the presence of IMC is the only difference in structure and both the loading and other consideration are the same, then the presence of IMC must have caused the

difference in deformation value and trend. Fig. 4-4 is the plot of plastic strain over load step for all the regions of both compositions. In the plot, region 1 of solder only bump experienced the highest strain while region 2 of solder+IMC bump recorded the least value. Thus, the presence of IMC restricts the visco-plastic deformation of solder and increases the stress in the joints. Strain gradient is found across the regions of solder only joint with maximum value at region 1 and minimum at region 3.

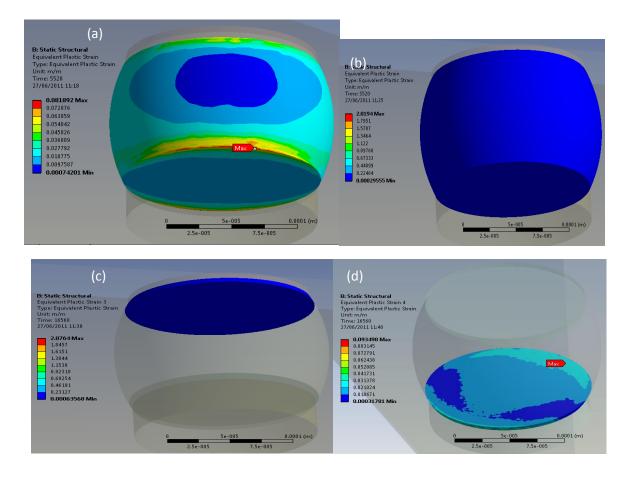
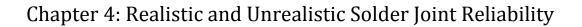


Figure 4-1 Plastic strain damage on critical solder bump showing:

(a) Plastic strain distribution on solder+IMC bump (b) Plastic strain on solder only bump; (c) Plastic strain on solder only region 1; (d) Plastic strain on solder only region 3



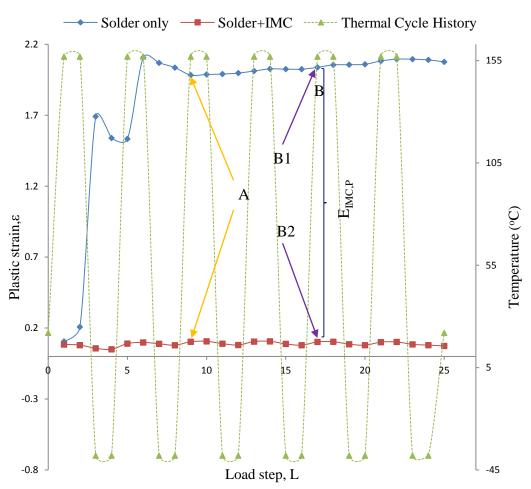
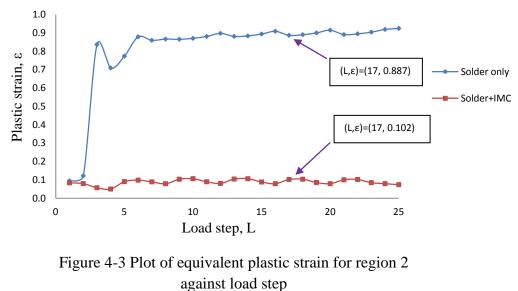


Figure 4-2 Plot of equivalent plastic strain on solder bump against load step



Chapter 4: Realistic and Unrealistic Solder Joint Reliability

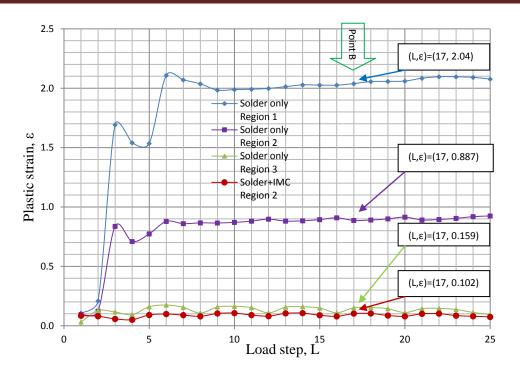


Figure 4-4 Plot of equivalent plastic strain distribution along longitudinal sections of solder bump against load step

4.3.2 Effect of IMC on plastic strain behaviour of solder bump joint

Fig. 4.2 is the plot of read out data points of plastic strain over the load step for the solder bump compositions. It is observed that a higher value of plastic strain is recorded when the bump is assumed to be composed of solder only. This is expected since solder only bump contains more solder by volume and the higher plastic strain value is advantageous in cushioning the effect of CTE mismatch and thermal shock during life operation. The plot (solder only) can be seen to stabilise at start of cycle number three shown as point A in the graph. An estimated difference in the plastic strain ($E_{IMC,P}$) between the two models was computed at the middle (Point B) of the remaining cycle because the strain rate is fairly at steady state from cycle three to six. At point B, the value of B1 and B2 are 2.038 and 0.0791, respectively. The percentage variation ($E_{IMC,P}$)% in the plastic strain value of the two compositions using solder only composition as the reference

point is approximately 96.1%. It is a general knowledge that solder bumps of a Sn-based solder and Au/Ni/Cu based bond pad on substrate consist of IMC; it is also known that critical parameters such as accumulated plastic work density and strain energy density of solder joint used in fatigue life models to compute service life of solder joint of electronic assembly depend on the plastic strain of the joint. Thus, ignoring the use of IMC in model development and analysis may have significant effect on predicted life of such solder joint. Muralidharan et al. [70] in a similar thermal cycling reliability study of solder joint reported an observed discrepancy between experimental results and FEM predictions. The discrepancies between the experimental results and FEM predictions have been a concern and many suggestions have been put forward. The author proposes, based on the result of this investigation that one of the causes is the non incorporation of IMC in the geometric model used to simulate the assembly response to temperature load, especially in high-temperature operating devices where IMC layer thickness is nontrivial and can grow up to 6 µm in magnitude.

The contribution of $E_{IMC,P}$ may be derived numerically. The underlying physics of the thermo-mechanics involved in the plastic strain deformation is governed by the equation:

$$\frac{\delta V_T}{\delta \theta} = \beta V_T \tag{4-1}$$

Where δV_T is the change in volume of the solder bump during thermal loading. V_T is the total volume of the bump made up of three volumetric regions. The β and $\delta\theta$ are volumetric expansion coefficient and range of temperature cycling limits. From bump geometry and configuration (fig. 3-4 and fig. 3-5),

$$V_T = V_1 + V_2 + V_3 \tag{4-2}$$

Where 1, 2 and 3 designate the three regions of the bump.

For solder only composition:

$$V_{T,(Solder only)} = V_{region 1} + V_{region 2} + V_{region 3}$$
(4-3)

For Solder + IMC composition:

$$V_{T,(Solder+IMC)} = V_{IMC} + V_{region 2} + V_{IMC}$$
(4-4)

Thus, change in volume is:

$$\delta V_{T,(Solder only)} = \beta \delta \theta (V_{region 1} + V_{region 2} + V_{region 3})$$
(4-5)

$$\delta V_{T,(Solder+IMC)} = \beta \delta \theta (V_{IMC} + V_{region 2} + V_{IMC})$$
(4-6)

From equation (4-5):

$$\frac{\delta V_{T,(Solder\,only)}}{V_{region\,1} + V_{region\,2} + V_{region\,3}} = \beta \delta \theta \tag{4-7}$$

Similarly, equation (4-6) gives:

$$\frac{\delta V_{T,(Solder+IMC)}}{V_{IMC} + V_{region \, 2} + V_{IMC}} = \beta \delta \theta \tag{4-8}$$

IMC in not visco-plastic and thus all changes are from region 2. Equation (4-8) therefore reduces to:

$$\frac{\delta V_{(region 2)}}{V_{IMC} + V_{region 2} + V_{IMC}} = \beta \delta \theta \tag{4-9}$$

Equation (4-7) may be re-written as:

$$\frac{\delta V_{(region 1)} + \delta V_{(region 2)} + \delta V_{(region 3)}}{V_{region 1} + V_{region 2} + V_{region 3}} = \beta \delta \theta$$
(4-10)

Applying volume constancy condition,

$$V_{IMC} + V_{region 2} + V_{IMC} = V_{region 1} + V_{region 2} + V_{region 3} = V_T \quad (4-11)$$

Combination of equations (4-9), (4-10) and (4-11) yields:

$$\frac{\delta V_{(region 2)}}{V_T}\Big|_{Solder+IMC} \neq \underbrace{\frac{\delta V_{(region 2)}}{V_T}}_{\mathsf{E}_{\mathsf{IMC, p}}} + \frac{\delta V_{(region 1)} + \delta V_{(region 3)}}{V_T}\Big|_{Solder only}$$
(4-12)

With reference to Eq. 4-12, it can be seen that if the thickness of IMC tends to zero in solder+IMC model, $\delta V_{(region 2)} \approx \delta V_T$ and the difference between the LHS and RHS of the equation will be minimised. Thus, the smaller the IMC thickness in a joint, the smaller the effects of its negligence in modelling reliability studies of the FC solder joints. Plastic strains at the regions may be called regional plastic strain, ε_i . Their values were read off from fig. 4-4 at point B and presented in table 4-1. Input of these values in equation (4-12) may provide further understanding of the expression.

Region (i=1,2,3)	Thickness, t _i (μm)	Volume, V _i (µm ³)	Regional plastic strain $\varepsilon_i = \frac{\delta V_i}{V_i}$ $i = (1,2,3)$ Solder onlySolder+IMC				
1	6.0	1.04E+05	2.04	0			
2	108.0	2.30E+06	0.887	0.102			
3	6.0	1.04E+05	0.159	0			
Bump v	olume, V_T	2.51E+06					

Table 4-1 Solder bump configuration and plastic strain

If volumetric strain relationship is expressed simply as:

$$\delta V_i = \epsilon_i V_i \qquad i = 1, 2, 3 \tag{4-13}$$

Then, equation (4-12) can be re-written as:

$$\frac{\epsilon_2 V_2}{V_T} \Big|_{\text{Solder+IMC}} \neq \frac{\epsilon_2 V_2}{V_T} + \frac{\epsilon_1 V_1 + \epsilon_3 V_3}{V_T} \Big|_{\text{Solder only}}$$
(4-14)

$$\epsilon_2 \frac{V_2}{V_T} \Big|_{\text{Solder+IMC}} \neq \epsilon_2 \frac{V_2}{V_T} + \epsilon_1 \frac{V_1}{V_T} + \epsilon_3 \frac{V_3}{V_T} \Big|_{\text{Solder only}}$$
(4-15)

$$\epsilon_2 V_{2f}|_{\text{Solder+IMC}} \neq \epsilon_2 V_{2f} + \epsilon_1 V_{1f} + \epsilon_3 V_{3f}|_{\text{Solder only}}$$
(4-16)

 $V_{if(i=1,2,3)}$ is the regional volume fraction. Substituting numerical values from table 4-1 into Eq. (4-16):

$$0.09|_{Solder+IMC} \neq \underbrace{0.81}_{\mathsf{E}_{\mathsf{IMC},\,\mathsf{p}}} + 0.09|_{Solder\,only} \tag{4-17}$$

It can be suggested based on equation (4-17) and as can be seen from figs. (4-2, 4-3 and 4-4) that the presence of IMC has contributed to the decrease in plastic deformation value of solder of region 2 from approximately 0.81 in solder only bump to 0.1 in solder+IMC. As observed in fig. 4-4, solder only region 1 has the highest value of deformation and even solder only region 3 has deformation value higher than solder +IMC region 2. Consequently, since these two regions in solder+IMC model are made of IMC which do not undergo visco-plasticity, their impact on region 2 as a result of their deformation is minimal/zero. The two regions seem to serve as an inhibitor preventing solder+IMC region 2 to plastically deform freely. A corollary result is that boundary stress is induced at the interface between the solder bulk and the IMC regions. At reduced solder bump volume, the effect of similar observation may be critical and significantly impacts solder joints reliability as large solder volume is desirable to produce large plastic strain needed to cushion the effect of CTE mismatch. In this analysis, the percentage difference in plastic strain values of the two compositions using solder only composition as the reference is approximately 90%. The difference between this value and the 96.1% computed earlier using fig. 4-2 is about 6.0%.

4.3.3 Study on bump joint plastic work

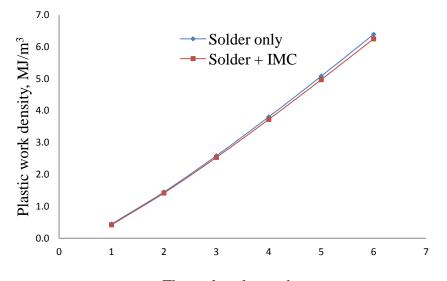
A body accumulates plastic work (w_p) when an external load imposed on the body induces plastic strain in the body. Thermal load on chip level assembly does the same on solder bump used to attach the chip on board. The accumulated plastic work is a measure of damage in the body and is thus referred to as a damage parameter where a high value signifies low joint reliability and vice versa. Plastic work density (ΔW_p) has been shown to be a better parameter in estimating solder joint fatigue life. Numerically, the average value of ΔW_p can be expressed as:

$$\Delta W_{p,avg} = \frac{\sum_{i=1}^{n} \Delta W_i \cdot \Delta V_i}{\sum_{i=1}^{n} \Delta V_i}$$
(4-18)

Where, ΔW_i is plastic work accumulated in a cycle in element i and ΔV_i is the volume of the element. The ANSYS software code used in computing the magnitude of the change in plastic work is given in Appendix A. It is observed in fig. 4-5 that solder only joint experiences higher magnitude of nominal plastic work, which increases continuously with load step for both joints until failure occurs.

The change in plastic work density over load step induces accumulated plastic work which is the cause of failure of solder joint. Its plot over load step is shown in fig. 4-6. It is observed that the highest damage leap occurs in load step two; the impact of this loading could be described as thermal shock and is independent of joint composition. The two joints investigated show differences in response to the load from load step two onwards with solder only composition developing higher inelastic deformation. From the plot of percentage change in plastic work over load step (fig. 4-7), it is seen that the nonlinearity in the accumulation of damage could give way to steady state plastic work accumulation. This is an indication

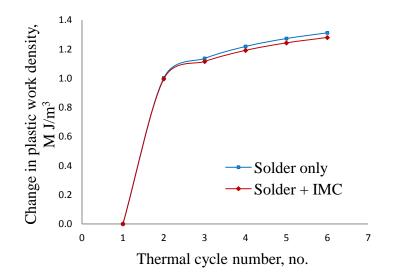
that solder joints experience strain hardening and stress relaxation afterwards which could be advantageous to joint reliability. This finding underscores the concern needed in determining the real value of $\Delta W_{p,avg}$. From this view point, the use of one or two thermal cycle(s) is/are inadequate in modelling studies. The author recommends at least six thermal cycles. The argument for the recommendation of six ATC is strengthened in chapter 7.

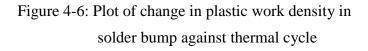


Thermal cycle number, no.

Figure 4-5: Plot of plastic work density against thermal cycle in solder bump

Chapter 4: Realistic and Unrealistic Solder Joint Reliability





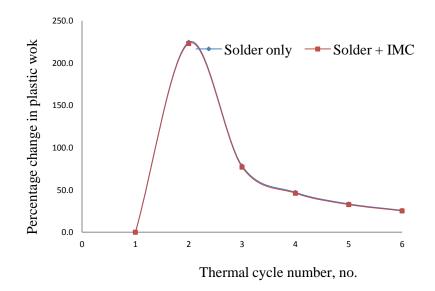


Figure 4-7: Plot of percentage change in plastic work density in solder bump against thermal cycle

4.3.4 Study on strain energy of bump joint

The work done by external forces in producing deformation in a body is stored within the body as strain energy; the strain energy per unit volume is referred to as strain energy density. The thermal load imposed on the solder joints induces plastic deformation which culminates in thermal stress. The deformation is stored in the body as strain energy. Strain energy damage in solder at various regions of the two models are represented in fig. 4-8. It can be seen from fig. 4-8 (a and b) that IMC influences solder joint strain energy. Fig. 4-8 (c and d) shows the contribution of IMC to strain energy development at the interconnect of IMC at PCB side and solder region 2 for the two models. The severity of bump with IMC can be observed. A comparison of strain energy of region 3 for the two bumps is presented in fig. 4-8 (e and f) to show the character and evolution of damage distribution on IMC and solder, respectively. It is observed that while solder damage is fairly evenly distributed, IMC damage concentrates at the periphery of the diametric plane of interconnect – a potential site for crack initiation.

The plots of output data of strain energy as a function of load step are shown in figs. 4-9 and 4-10. Fig. 4-9 (b) is the section of fig. 4-9 (a) in dotted green colour ellipse. In the plot, while solder only joints exhibit higher strain energy density with lower amplitude and localised resonances, solder+IMC bumps can be seen to observe higher amplitude of oscillation. Although it is observed that strain energy density value of solder only bumps is higher than solder+IMC, however the higher amplitude of oscillation of solder+IMC bumps coupled with its character of damage (damage concentration at the periphery) indicates that its reliability may be more critical and its failure will mainly be driven by fatigue crack mechanism. It is the author's opinion that the higher stain energy of solder only bump is due to the greater volume of solder it contains and also greater freedom of thermal expansion. These properties are advantageous in cushioning the effect of CTE mismatch of the bonded joint materials. This opinion is supported by the

non colour gradient of fig. 4-8 (b) in comparison to fig. 4-8 (a). It also supports the discussion in section 4.3.2.

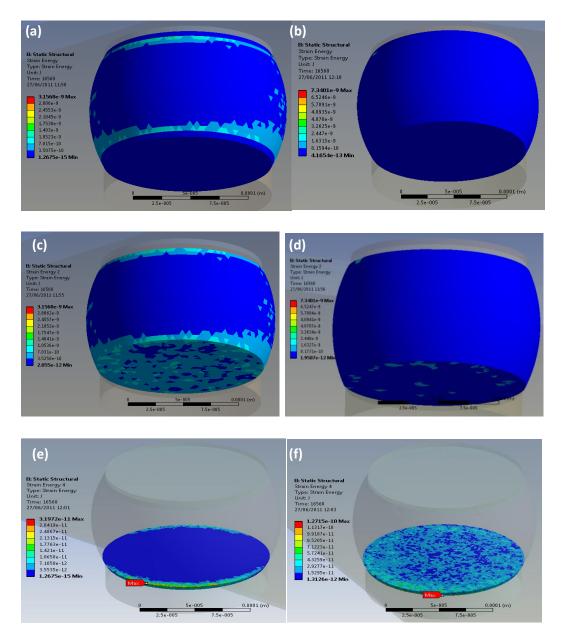


Figure 4-8: Strain energy damage in solder regions showing:

(a) Strain energy on solder+IMC bump; (b) Strain energy on solder only bump; (c) Strain energy on solder+IMC region 2; (d) Strain energy on solder only region 2; (e) Strain energy on solder+IMC region 3; (f) Strain energy on solder only region 3

The strain energy density for all the regions in the two bumps is plotted in fig. 4-10. Some localised resonances are observed in the first two cycles at load step three and six. The instantaneous energy at work could be intrinsic energy at maximum plastic deformation load for step three and the other, intrinsic energy at the onset of strain hardening and stress relaxation. It is also observed that the solder only region 2 developed the highest strain energy density within the first cycle and solder only region 1 was the highest in the second. This phenomenon indicates the existence (in solder only bump) of different critical plane volumetric strain energy densities which result in shear force between planes of solder regions and also strain energy density gradient along the longitudinal axis of the bump.

Fig. 4-10 (b) enclosed in the green circular shape is a magnified portion of fig. 4-10 (a) in green elliptical shape too. In this enclosed part, it is observed that solder+IMC region 1 is the most critical and solder+IMC 3 is the least at onset of joint stabilisation (cycle no. 3). These findings also support the claim that the use of one or two thermal cycles may not be adequate in modelling investigations. The differences in strain energy density magnitudes between regions 1, 2 and 3 of solder+IMC bump signify that plane shear strain (with different magnitude) exists at regional planes of the bump and the magnitude is maximum at interface between IMC at die side and its solder region 2. The significance of this finding is that the interface between IMC at die side and its solder region 2 is the most susceptible failure site in a FC that is properly assembled on a PCB (see fig. 7-3). It can be seen from the plot that strain energy density gradient across solder+IMC bump is greater than that across solder only bump. The distribution of damage caused by strain energy across the longitudinal section of the solder bump has shown regions of concern and criticality. It may also have shown the inherent inaccuracy in modelling study when IMC is not integrated in the finite element geometry model.

Chapter 4: Realistic and Unrealistic Solder Joint Reliability

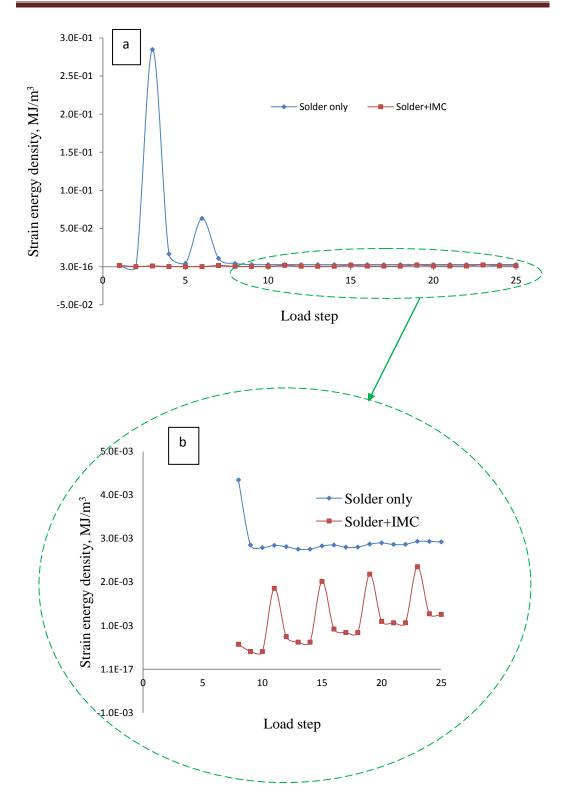


Figure 4-9 Plot of strain energy density of solder bump against load step

Chapter 4: Realistic and Unrealistic Solder Joint Reliability

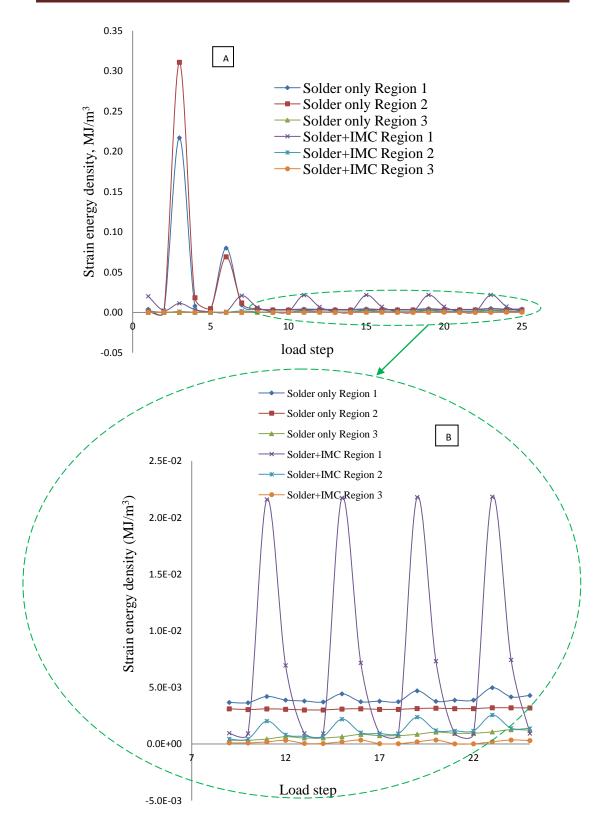


Figure 4-10 Plot of regional strain energy density of solder against load

Page 82

4.3.5 Effects of IMC on solder bump joint fatigue life prediction

Many models have been proposed to calculate the fatigue life of solder joints and these have been discussed in section 2.4.2. The most commonly used and widely accepted models are based on a single parameter, the plastic work density, as the damage indicator. The models Seyd [52] proposed for SnAgCu solder bump joint life prediction is adopted for this study. These models are discussed extensively in section 2.4.2. The particular model employed is given as number 3 in table 2-5 of section 2.4.2. The model is used because it is based on a single creep mechanism similar to the Anand's model utilised to capture the solder damage evolution. For convenience, it is restated again in Eq. (4-19).

$$N_f = (0.0015 w_{acc})^{-1} \tag{4-19}$$

As has been discussed in section 2.3.2, while Syed [52] used 0.0015 as value of the constant W' Stoyanov [59] used 0.0014 instead. In this study, an average value of 0.00145 between the two models is utilised as presented in Eq. (4-20).

$$N_f = (0.00145 w_{acc})^{-1} \tag{4-20}$$

Although equation (4-19) is developed for creep, it is used in this study where W_{acc} is due to visco-plasticity and not creep plasticity. Darveaux [71] proposed a model based on Anand's constitution but the model was developed for tin-based solder. The author has no knowledge of model for SnAgCu based on Anand's constitutive equation.

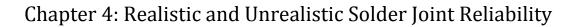
The numerical value of W_{acc} which can be seen to impact reliability/cycle to failure of the FC is affected by the presence of IMC as can also be seen in figs. 4-5, 4-6, 4-9 and 4-10. It is pertinent to note that damage in solder joint is caused by change in plastic work density from cycle to cycle and not the nominal value of the plastic work density. From the data used to plot fig. 4-6, the value of W_{acc} for solder only and solder+IMC are 0.940 MJ/m³ and 0.926 MJ/m³, respectively.

Table 4-2 summarises the results of the effect of IMC on the FC solder joints fatigue life estimation.

Model	W	Wacc	Predicted life (Cycle)	% change from solder only bump
Solder only	0.001451	0.940	734	0
Solder+IMC	0.001452	0.926	745	1.5

Table 4-2 Effects of IMC on FC solder joint fatigue life

The results show that the thickness of IMC used in this study is capable of increasing the fatigue life of solder joint by 1.5 percent when compared to the result obtained when IMC is not incorporated in the model. This result is so because the damage parameters (W' and W_{acc}) upon which the model is based depends only on the solder. Syed [52] published fig. 4-11 showing that measured and predicted mean fatigue lives of solder joint vary. He reported in the same paper that his model predicts life within 25% of measured life in most cases and that the 25% is a widely acceptable limit. Darveaux [71] states that the accuracy of relative predictions is within ±25%. Having used reference [52] life prediction model and incorporated IMC in our physical model, we have demonstrated that the 25% can be improved upon and reduced to 23.5% using data from literature. The deviations of predicted from experimental values reported by many authors using different life prediction and physical models not including IMC are presented in table 4-3.



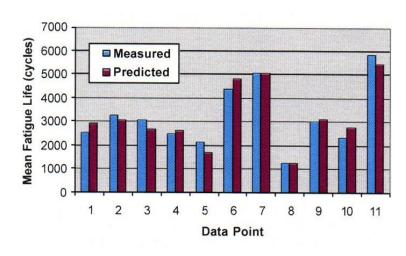


Figure 4-11 Comparison of predicted and measured mean life for eutectic SnPb solder joint [52].

Table 4-3	Table 4-3 Deviations of predicted solder joint fatigue life from							
measured/experimental value								
Author	Package	Solder	Model	Experimental (Cycle)	Predicted (Cycle)	Deviation from experimental		
Lee and Lau [72]	PBGA	SnAgCu	Coffin-Mason	4772	3310	-31		
Zhang et al. [73]	CSP	SnPb	Modified Darveaux	856	745	12.9		
Rodgers et al [74]	MicroBGA	SnAgCu	Schubert et al.	4123	2417	-41.4		
			Modified					

SnPb

SnPb

Coffin-

Manson

Anand/Zahn

2826

54

2840

60

0.5

11.1

Lau and Lee [75]

Yang and Ume [31]

PBGA

FC

(%)

Table 4-3 Deviations of	f predicted solder	joint fatigue	life from

The variation in the values of experimental and predicted solder joint fatigue life in table 4-3 is expected because the values depend on many factors which vary among the investigations. While the experimental values depend on the test conditions, the predicted values depend on the inputs to the computer used in the simulations and maintenance of consistency in the modelling procedure.

Specifically, factors which include but are not limited to package size, solder type, model used, experimental parameters (ATC), computer simulations (mesh size) affect the results.

4.4 Conclusions

Thermo-mechanical reliability study on realistic flip chip model FC48D6.3C457DC solder bump joints using FEM has been conducted and reported in this chapter. The impact of IMC on the reliability of lead-free solder joints has been investigated. Based on the results of this study and the key findings, the following conclusions may be made:

- The non incorporation of IMC in the geometric model of solder joint is one possible cause of discrepancy between the predicted and the experimentally determined fatigue life of solder joints. The interface between IMC at die side and solder bulk is the most critical site of solder joint failure.
- Failure mechanism is dependent on the bump composition. A combination of fatigue loading, occasioned by high amplitude of cyclic plastic strain, and plane plastic shear strain principally drive failure in bumps with IMC while plastic deformation driven by shear damage is a key failure mode in bumps without IMC.
- The occurrence of strain hardening and stress relaxation in solder joints change plastic work density values over thermal cycles and thus make the use of few temperature load cycles inadequate in modelling studies.
- Deformation gradient accumulates along the longitudinal section of the solder bumps and causes device failure.
- Two load steps of thermal cycle history are critical and may impact the accelerated and highly accelerated life testing (ALT and HALT) of solder joint.

CHAPTER 5

EVALUATION OF THE IMPACT OF COMPONENT STAND-OFF HEIGHT (CSH) ON HIGH-TEMPERATURE FATIGUE LIFE OF FLIP CHIP LEAD-FREE SOLDER JOINTS

5.1 Introduction

FCs assemblies of dies on substrates are one of the advanced components of microelectronics. The small size package is currently poised to be the strategic technology to match ever progressive miniaturization trends in electronics packaging. One challenge to this potential is the recent uses at high-temperature ambient of microelectronics as sensors or control devices because it increases the rate of visco-plastic degradation of joints of their components. The response of solder bumps to induced thermal load culminates in plastic strain which accumulates damage in the joints. Accumulation of damage in the joints subsequently leads to fatigue failures of the joint. Another challenge is that elevated temperature operations reduce the MTTF of HTM. The factors which affect the reliability of solder joints have been discussed in section 1.1 and CSH is identified as one of them. The geometric relationship between the size of diameter of PCB bond pad and that of die bond pad is used to control and determine the CSH. The bond pads are usually defined by solder mask.

In this chapter, research work which investigates the high-temperature fatigue life of FC lead-free solder joints at varying CSH is presented. It is the purpose of this study to determine how magnitude of indices such as stress, strain and plastic work density used to measure static structural reliability of solder joint depend on CSH. Furthermore, this chapter outlines the effect of CSH on the fatigue life of FC solder joints. The solder joint was partitioned into regions to aid investigation. A whole joint is named a bump and section of the joint containing only solder is called solder region or simply solder. The CSH was defined as a function of the geometric relationship between bond pad size on the die and that on the PCB. The study on the stress and strain in the FC joint provides a relationship between stress and strain developed in the interconnects in both the bump and solder and the bond pad size. It also yields site of joint failure and its mechanism. The research finding on plastic work density furnishes the relationship between change in accumulated plastic work density and volume of the solder region. The fatigue life of component solder joint was predicted at varying CSH to evaluate the effect of CSH on the integrity of FC joint at high-temperature excursions. The outcome reveals that the number of cycle to failure (N_f) of a solder joints is a function of the CSH. This chapter ends in conclusions drawn from the findings of this study.

Different bump sizes possess different shape and CSH. The key issue remains that identical FCs are often mounted on different diameters of PCB bond pads during assembly. Different manufacturing processes employed by different PCB manufacturing companies produce variations in diameter of the bond pad. As a result, CSH could vary for identical component assembly. One of the key consequences of mounting identical FCs on PCB bond pads with different diameters is the variant in solder bump shapes and specifically the CSH. Moreover, slight change in reflow process such as increase in reflow time or temperature causes solder to flow out of the pad and spread on the PCB. This incidence occurs even in the presence of solder mask on the PCB. The solder bump profile is generally known to impact the reliability of solder joint as distinct bump configurations possess different thermo-mechanical behaviours during device operation in the field. Thus, investigation of the effects of variation of CSH on solder joint damage partly and fatigue life of the joints subsequently will provide further knowledge necessary to improve the integrity of FC solder joints.

This chapter discusses results of a modelling study focused on the effects of CSH on static structural integrity of lead-free solder joints of FC48D6.3C457 package which is cycled between -38 °C and 157 °C temperatures. The result analysis is based on accumulation of damage indicators such as stress, strain and plastic work density in the solder joints. The accumulated damage was used to predict the life of different architectures of the FC assembly.

5.2 Methodology

FEM discussed in section 3.4 was employed in this investigation. Anand's viscoplastic model also discussed in section 2.4.1.2 was utilised to capture the solder plastic deformation in the joints of the FC assemblies (one assembly shown in fig. 3-3) which was loaded and bounded as discussed in section 3.4.3. Appropriate mesh achieved through good body sizing was used in the study. Each model consists of a total of 10,359,387 nodes and 8,386,466 elements.

The bumps were generated using parametric ANSYS' scripts that allow the change of geometry with ease. The window of a script which shows outline of all parameters and part of table of design points is depicted in figure 5-1. The input parameters as well as the output parameters with their representative name are shown. This window also shows the values of these parameters in the current design points. Full table of design points is represented in fig. 5-2. The procedure employed in generating the bump profiles has been discussed in section 3.2. A serial number 1 to 6 bump profiles of table 3-1 were used for this investigation.

-		👔 Import 🖓 Reconnect 键 Re	mesh Project 🥜 (n Points	Return	to Project	Compact Mode										
tine of a	All Parameters				Table o	f Design Poir															-
	A	В	С	D		A	В	с	D	E	F	G	н	I	J	к	L	м	N	0	Р
1	ID	Parameter Name	Value	Unit					P3				P16 - Equivalent	P17 -	P18 -	P19 -	P20 -	P21 -	P22 -	P23 -	P24 -
3	Input Parameters Geometry (A1)				1	N 💌	P1 - D01Cut	R01	h1	P4- Rarc1	P9 - PlaneHeight	P15 - D01Add 💌	Plastic 💌	Strain Energy	Equivalent Stress 2	Equiv Stress 3	Equivalent Stress 4	Equivalent Stress 5	Stress 6	Equivalent Stress 7	Strain Energy 2
4	P1	D01Cut	116.8						nı		-		Strain Maximum	Maximum	Maximum	Maximum	Maximum	Maximum	Maximum	Maximum	Maximum
5	φ P1 Φ P2	R01	58.4		2								m m^-1	J	Pa	Pa	Pa	Pa	Pa	Pa	J
5 6	φ P2 Φ P3	h1	130		3	Current	116.8	58.4	130	126	165	116.8	0.074012	2.8587E-09	3.6773E+09	1.7832E+09	4.3769E+09	3.6773E+09	3.3569E+09	8.4058E+07	2.8587E-0
7	φ P3 Φ P4	Rarc1	126		4	DP 1	131.4	65.7	126	139.34	161	131.4	1	7	4	1	1	4	1	9	1
8	φ P4 Φ P9	PlaneHeight	165		5	DP 2	146	73	120	148.82	155	146	9	7	9	1	1	9	1	9	1
9	φ P9 Φ P15	D01Add	165		6	DP 3	160.6	80.3	114	160.07	149	160.6	1	7	1	1	1	1	1	9	7
*	New input parameter	New name	New expression		7	DP 4	175.2	87.6	107	174.02	142	175.2	1	9	4	4	4	4	1	9	7
	Output Parameters	New name	New expression		8	DP 5	189.8	94.9	101	190.06	136	189.8	9	7	9	9	1	1	1	9	7
12	Static Structural (B1)				9	DP 6	204.4	102.2	94	210.27	129	204.4	1	7	1	1	1	1	1	9	7
13	P16	Equivalent Plastic Strain Maximum	0.074012	m m^-1	10	DP 7	219	109.5	88	233.24	123	219	1	9	4	4	4	4	1	9	1
14	P4 P10	Strain Energy Maximum	2.8587E-09	3	*																
15	P18	Equivalent Stress 2 Maximum	3.6773E+09	Pa																	
16	P19	Equivalent Stress 3 Maximum	1.7832E+09	Pa																	
17	P20	Equivalent Stress 4 Maximum	4.3769E+09	Pa																	
18	P21	Equivalent Stress 5 Maximum	3.6773E+09	Pa																	
9	P22	Equivalent Stress 6 Maximum	3.3569E+09	Pa																	
0	P23	Equivalent Stress 7 Maximum	8.4058E+07	Pa																	
1	P24	Strain Energy 2 Maximum	2.8587E-09	3																	
2	P₹ P25	Equivalent Plastic Strain 2 Maximum		m m^-1																	
23	P26			m m^-1																	
24	P27	Equivalent Plastic Strain 4 Maximum		mm^-1																	
25	P28	Strain Energy 3 Maximum	5.2357E-11	3														_			
26	p→ P29	Strain Energy 4 Maximum	2.5015E-11	3			_	_	_	_											
	New output	or an energy maximum		-	Chart:	No data															-
	P4 parameter		New expression																		
28	Charts																				

Figure 5-1 Parametric ANSYS script window showing outline of all parameters and parts of table of design

-] Import	ିତ୍ Rec	onnect 🤁 R	efresh Project 🥖	Update Project	🎋 Resume 💔	Update All Design	n Points 🕝 Retu	urn to Project 🧃	Compact Mode										
Ф X Та	able of	Design Poin A	s B	с	D	E	F	G	н	I	J	к	L	м	N	0	Р	Q	R	s	т	U	v
1 2 3 4	1	N 💌	P1 - D01Cut				P9 - PlaneHeight 💌	P15 - D01Add	P16 - Equivalent Plastic Strain Maximum	P17 - Strain Energy Maximum	P 18 - Equivalent Stress 2 Maximum	P19 - Equiv Stress 3 Maximum	P20 - Equivalent Stress 4 Maximum	P21 - Equivalent Stress 5 Maximum	P22 - Equivalent Stress 6 Maximum	P23 - Equivalent Stress 7 Maximum	P24 - Strain Energy 2 Maximum	P25 - Equivalent Plastic Strain 2 Maximum	P26 - Equiva Plastic Strain 3 Maximum	P27 - Equivalent Plastic Strain 4 Maximum	P28 - Strain Energy 3 Maximum	P29 - Strain Energy 4 Maximum	Exporte
5	2								m m^-1	J	Pa	Pa	Pa	Pa	Pa	Pa	J	m m^-1	m m^-1	m m^-1	J	J	
	3	Current	116.8	58.4	130	126	165	116.8	0.074012	2.8587E-09	3.6773E+09	1.7832E+09	4.3769E+09	3.6773E+09	3.3569E+09	8.4058E+07	2.8587E-09	0.071404	0	0	5.2357E-11	2.5015E-11	
7	4	DP 1	131.4	65.7	126	139.34	161	131.4	4	4	9	1	4	9	4	9	1	¥	4	4	4	4	V
8	5	DP 2	146	73	120	148.82	155	146	9	7	9	7	7	7	9	9	7	7	7	7	1	1	V
	6	DP 3	160.6	80.3	114	160.07	149	160.6	7	7	7	7	7	7	7	7	7	7	1	7	1	7	V
9	7	DP 4	175.2	87.6	107	174.02	142	175.2	1	4	4	4	7	7	4	9	7	7	7	7	4	4	
	8	DP 5	189.8	94.9	101	190.06	136	189.8	7	7	1	7	7	7	1	1	7	7	7	7	1	1	V
11	9	DP 6	204.4	102.2	94	210.27	129	204.4	1	7	4	7	9	7	1	4	7	7	1	7	4	4	V
13	10	DP 7	219	109.5	88	233.24	123	219	1	7	1	7	7	7	7	7	7	7	7	7	4	1	V
14																							
17 18																							
18 19 20 21 22 23 24 25	hart: N	io data																					
18 19 20 21 22 23 24 25 26 ch	ihart: N	io data		_	_			_															

Figure 5-2 Parametric ANSYS script window showing full table of design points

The schematics of the six sizes of the generated bumps B_i (i=1, 2 ..., 6) whose volumes are equal are shown in fig. 5-3. While fig. 5-3(a) is the front view of the bumps, fig. 5-3 (b) is the bottom view of the bumps from PCB side. The parameters used to describe the configurations of the bumps are; radius of bond pad on PCB (R_0), radius of bond pad on die (R_h), CSH, (h) and radius of arch defining the bump profile (R_{arc}). The relationship between PCB bond pad size denoted as P_i (*i* =1, 2, 3, 4, 5 and 6) and the three shape parameters are plotted in fig. 5-6. Table 5-1 contains configurations of the six sizes of PCB bond pad diameters (D_i) generated when the die bond pad diameter is constant at 146µm while the PCB bond pad diameter is varied. Table 5-2 contains the dimensions of these geometric parameters used to create the bumps. This table is an extraction from table 3-1. The fig. 5-4 depicts a magnified solder joint structure with the R_0 at height zero and the R_h at height, h. Other bump shape parameters such as CSH and R_{arc} are functions of the bond pads diameter. Fig. 5-5 shows a single bump of the FC with mesh, regions of solder and the IMCs. It also shows layer of the IMC thickness located at both the die and PCB sides of the assembly.

The assemblies of the models were subjected to the same conditions of temperature cycle load between -38°C and 157°C at 15°C/min ramp rate and 10 min dwell time at both upper and lower regions. Temperature limits of -38°C and 157°C were selected because it is within the temperature cycle test range of Mil-Std-883, method 1010 Specs [76]. The temperature ramp rate of 15°C/min and 10 min dwell time are standards of Mil-Std-883 Method 1010 Specs and JEDEC JESD22-A 104 Specs [76]. Aoki et al. [67, 68] believe that 15°C/min ramp rate is market environmental condition, an IEC 60749-25 and JEDEC JESD22-A104-B standard and reported that the ramp rate is widely used in the United States and Europe. A total of six cycles in 25 load steps amounting to 16,560 seconds of test time was employed.

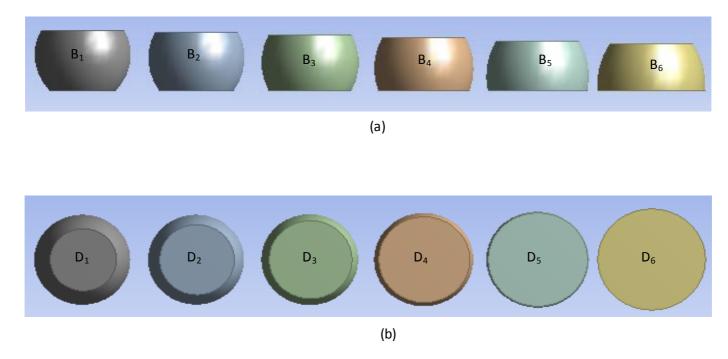


Figure 5-3 Six sizes of solder bump showing: (a) front view of solder bumps; (b) PCB bottom plan of bumps

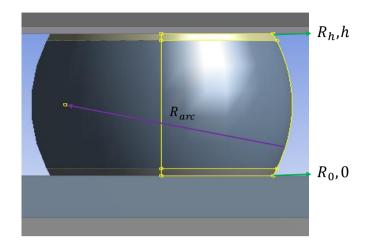


Figure 5-4 Radius of bond pads at both PCB and die sides

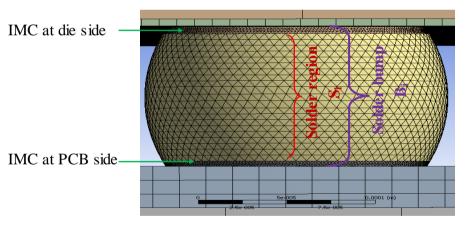


Figure 5-5 A single flip chip solder bump showing solder region contained in solder bump

PCB bond	PCB bond Pad	Change from die
pad size	diameter, D_i (µm)	bond pad diameter (%)
1	116.8	-20
2	131.4	-10
3	146.0	0
4	160.6	10
5	175.2	20
6	189.8	30

Table 5-1 Configuration of PCB bond pad diameter

Table 5-2: Configurations of solder bumps, (B_i)

Bump B _i (i=1 to 6)	$R_0 (\mu m)$	R_{h} (µm)	h (μm)	R_{arc} (µm)
1	58.4	73	130	126.00
2	65.7	73	126	139.34
3	73.0	73	120	148.82
4	80.3	73	114	160.07
5	87.6	73	107	174.02
6	94.9	73	101	190.06

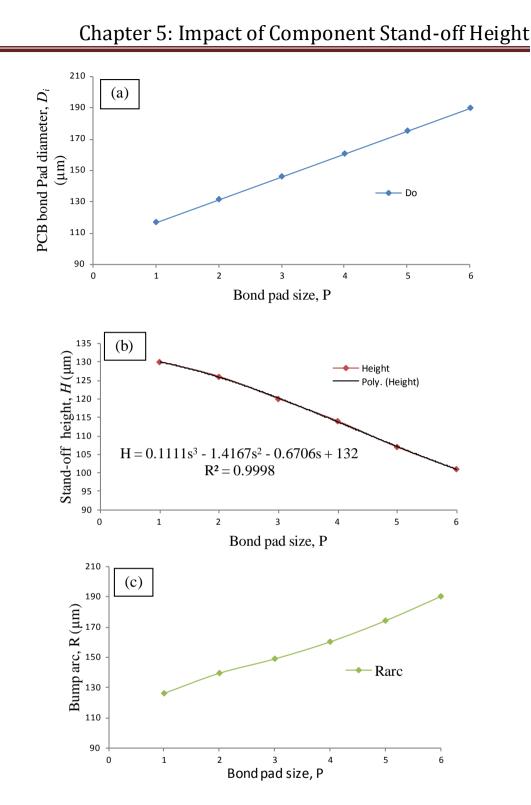


Figure 5-6 Relationship between size of PCB bond pad diameter and solder bump shape parameters, showing: (a) PCB bond pad diameter as a function of PCB bond pad size; (b) Component stand-off height as a function of PCB bond pad size; (C) Bump arc as a function of PCB bond pad size

5.3 Results and discussion

The results of this study and their discussion are presented and carried out respectively in three subdivisions. These parts are stress and strain, plastic work density and predicted fatigue life of component solder joints.

5.3.1 Study on stress and strain in FC solder joints

Plots of values of bump stress and solder stress as functions of P_i on the same graph are presented in fig. 5-7. Bump (B_i) is described as the solder joint after reflow which consists of solder region and the IMCs while solder is just the region of the bump made up of solder (fig. 5-5). The solder/solder region is denoted as S_i (i = 1, 2, 3, 4, 5 and 6). It can be seen in fig. 5-7 that while solder stress decreases from P_1 to a minimum at P_3 , the bump stress increases slightly in this range. The stress magnitudes of both bump and solder increase afterwards. The author believes that the geometry of the solder bump plays a dominant role in the magnitude of equivalent stress induced in the solder. Bump and solder stress accumulations could be explained using the physical interpretation of the Von Mises yield criterion. The deformation behaviour of the bump and solder is governed by maximum distortion strain energy of the joint which serves as the yield criterion. The relationship between equivalent stress (σ_v) and the elastic strain energy of distortion (W_D) is represented in equations (5-1) and (5-2).

$$W_D = \frac{\sigma_v^2}{6G} \tag{5-1}$$

$$G = \frac{E}{2(1+\nu)} \tag{5-2}$$

Where G is the elastic shear modulus, E is the Young modulus of elasticity and v is the Poisson ratio. Poisson ratio is a geometric parameter and it is easy to see in fig. 5-3 that bump geometry is different for different configurations, thus the difference in the response of the solder bumped joints. However, further research is needed to explain the decrease in stress magnitude of P_2 and P_3 to temperature load.

With B_3 recording the least solder stress, deviations between diameters of die bond pad in relation to the PCB bond pad increase the magnitude of stress induced at the solder region. Owing to the contribution of CSH to the induced stress, deviations culminating in decrease in CSH produce higher stress/damage than their counterparts which increase the magnitude of stand-off height. Thus, S_4 recorded higher stress than S_2 and likewise S_5 solder stress magnitude is higher than S_1 . With reference to fig. 5-7, it can be seen that stress in solder bump increases with decrease in solder bump height (CSH). Fig. 5-8 shows the plot of values of bump and solder strain over P_i . Strain values of both bump and solder were constant from P_1 up to P_4 and deviates afterwards. The interconnect of solder and IMC from P_4 to P_6 experiences plane shear force due to unequal magnitudes of plastic strain range between solder and IMC. The resulting shear force induces boundary stress which could trigger off crack nucleation and propagation at the interconnections. The schematic representations of distribution of stress and strain in critical bump and solder joints are shown in figs. 5-9 and 5-13, respectively.

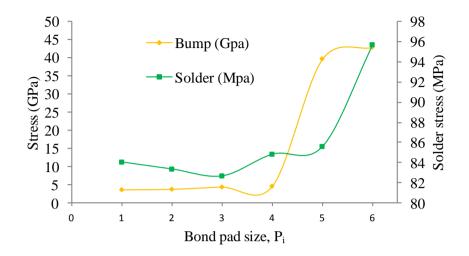


Figure 5-7 Plots of bump stress (GPa) and solder stress (MPa) as functions of bond pad size

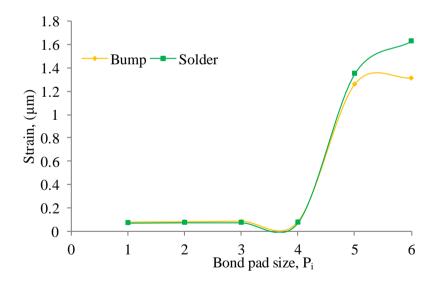


Figure 5-8 Plot of bump strain (μ m) as a function of bond pad size

The first and second columns of fig. 5-9 are the stress distribution in critical bumps and solder regions of the FC joints, respectively. The representations show that maximum stress in the B_i and S_i occurs at the boundary between IMC at die side and solder bulk except for S_3 and S_5 . In the FC assembly utilising B_3 and S_3 shown in fig. 5-10, although the critical bumps are located at the corner of the assembly, the spots of the maximum damage in B_3 and S_3 are not in the same joint and site. The maximum damage in B_3 was at the boundary of bond pad on die and solder in one bump while the maximum damage in S_3 was at the boundary of the bond pad on PCB and solder in another bump. A similarly occurrence is observed in B_5 and S_5 shown in fig. 5-11, but with a difference in the location of the critical bump. Fig. 5-11 shows that critical B_5 (fig. 5-11 (a)) is not at the corner while critical S_5 (fig. 5-11 (b)) is at the corner with fig. 5-11 (c) showing that the crack in critical B_5 extends to solder region. In P_6 , it is found that the critical B_6 and S_6 are not at the corner of the joint array (fig. 5-12). The author believes that further research is needed to explain observations in B_3 , S_3 and B_5 , S_5 of P_3 and P_5 respectively more so as it has been the general belief that the corner joints are the most suceptible to damage.

At B_5 and S_5 stress induced cracks are seen to develop at the boundary of IMC at die side and solder region, cutting both the IMC and solder bulk. The decrease in bump height may have contributed to the crack initiation. If the FC assembly (fig. 3-3) is idealised as a beam, then the fatigue loading induced in the structure occasioned by the effect of CTE mismatch (fig. 2-4) when the assembly is temperature cycled can be explained using the classic formula for determining the bending stress in a beam under simple bending:

$$\sigma = \frac{Mh}{I_x} \tag{5-3}$$

Where σ is the bending stress, *M* is the moment about the neutral axis, *h* is the perpendicular distance to the neutral axis and I_x is the second moment of area

about the neutral axis x. The height of the bump (CSH) is a direct function of h. The I_x may be defined as:

$$I_{\chi} = \frac{bh^3}{12} \tag{5-4}$$

The *b* is average of summation of the widths of component and PCB. With reference to equations (5-3) and (5-4), the induced fatigue stress in FC joints is in inverse relation to the CSH. Thus decrease in CSH is expected to increase damage in solder bumped joints. Fig. 5-13 has similar layout to fig. 5-9. The first and second columns are the strain distribution in critical B_i and S_i , respectively. The strain response of the bumps shows that B_i (*i*=2,3,4) records maximum damage at interface between solder and IMC at PCB side. In addition, the figure depicts that while the damage in B_i (*i* = 5 and 6) is maximum at the boundary between IMC at die side and solder, the position of maximum strain damage in B_i (*i* = 5 and 6) may have been caused by the shear force called into play at Pi (*i*=4, 5 and 6) by the difference in magnitude of plastic strain value of Bi and Si (*i*=5 and 6). At S_6 the crack propagates to the solder region as shown.

Bump, *B*_{*i* (*i*-1 to 6)} Solder region S_{i (i-1 to 6)} ANSY ANSYS **B**₁ ANSYS **SANSYS** Pa 16560 /2011 13:14 **B**₂ 7.4401e7 6.5437e7 5.6474e7 4.751e7 3.8547e7 2.9584e7 2.062e7 1.1657e7 **2.6934e6** B₃ \mathbf{B}_4

Stress in

Figure 5-9 to be continued

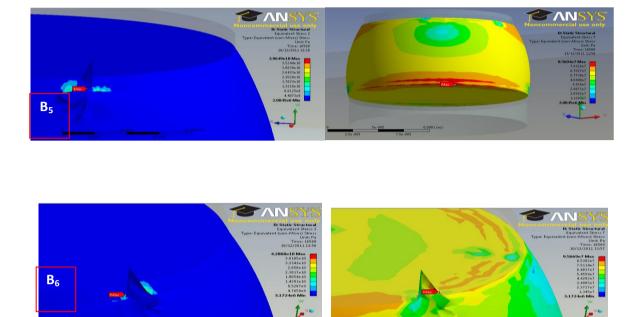
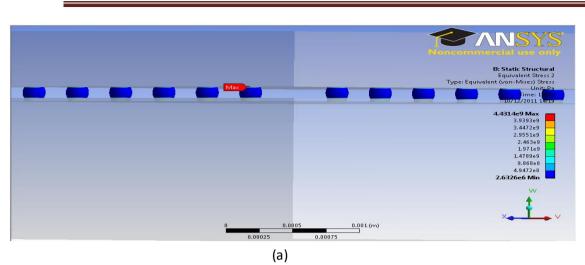


Figure 5-9 Damage in bump and solder using stress as the indicator



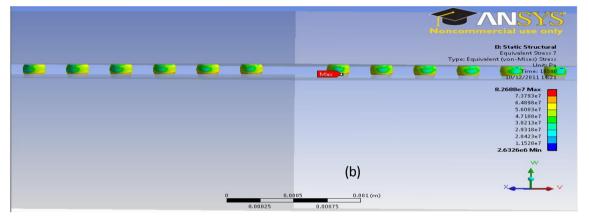


Figure 5-10 Relative position of damage in bump three (B_3) and solder region (S_3) using stress as the indicator showing: (a) critical bump (b) critical solder region

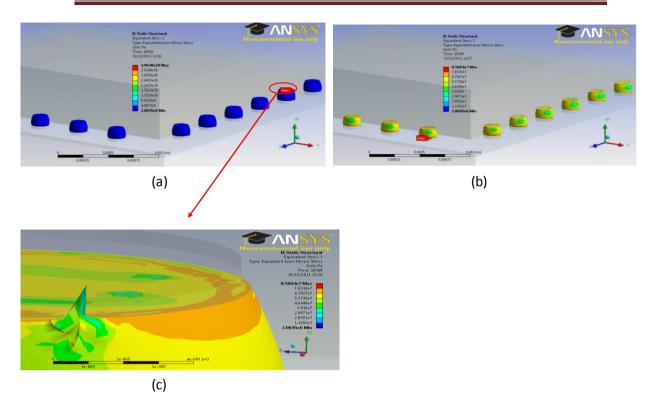


Figure 5-11 Relative position of damage in bump five (B_5) and its solder region (S_5) using stress as the indicator showing: (a) critical bump (b) critical solder region (c) solder region of critical bump

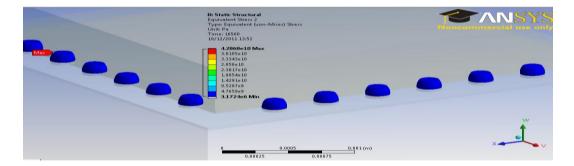


Figure 5-12 Relative position of damage in bump six (B_6) and its solder region using stress as the indicators

Strain in

Bump *B_i* (*i*-1 to 6)

Solder $S_{i(i-1 to 6)}$

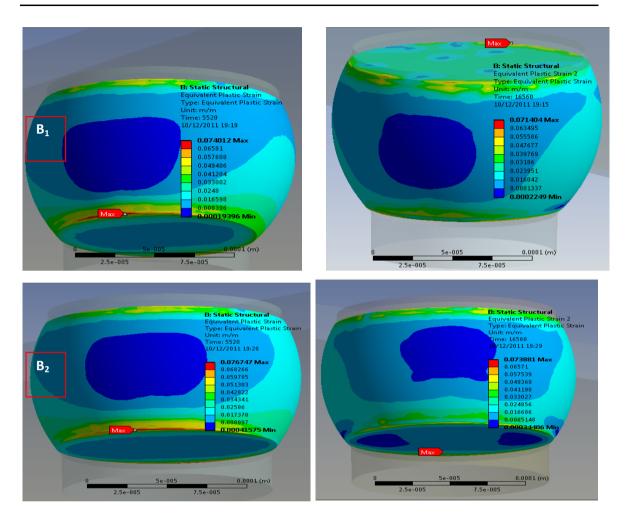
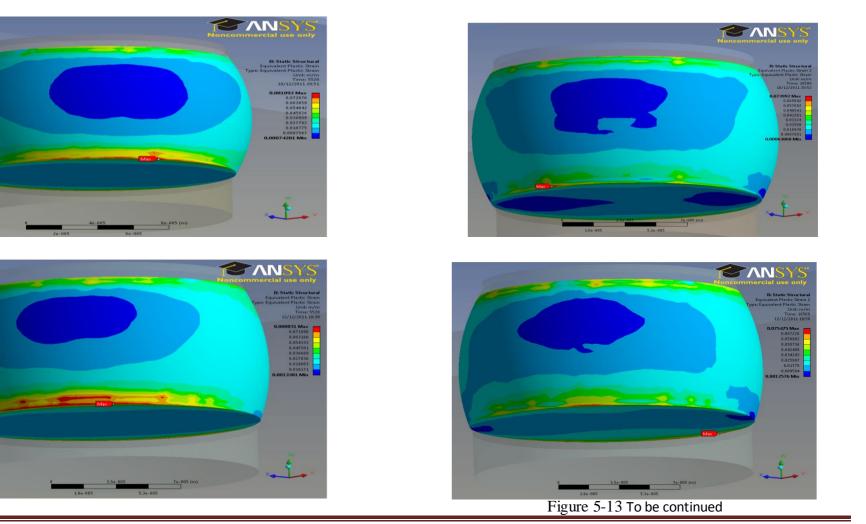


Figure 5-13 To be continued



B₃

B₄

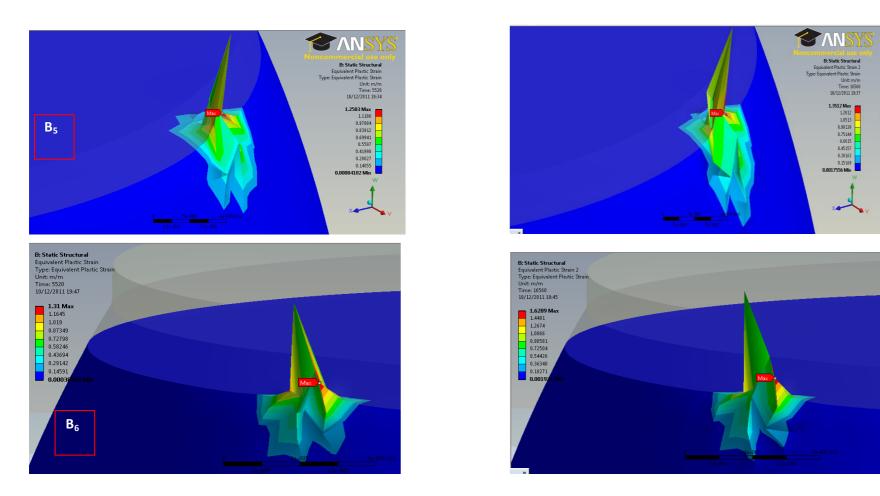


Figure 5-13 Damage in bump and solder using strain as the indicators

Many researchers including Xie et al. [27] and George et al. [69] reported similar findings from their experimental works which are comparable to the one being studied using FEM. The former reported that cross section of failed samples showed the crack in bulk solder at package side a typical failure mode found on BGA packages post thermal cycling. In fig. 5 (a), Arulvanan et al. [6] reported that the failure mode observed were more progressive and gradual with almost clear separation of the bulk solder from the inter-metallic compound at the substrate side after 3000 thermal cycles. A like, the latter reported that irrespective of the solder paste or board finish used, the failures in the 256 I/O was due to crack propagation at the solder-package interface, as shown in Fig. 5-14 (b). The correlation between these referred research works and our work in terms of indices such as assembly dimension, structure, material composition, stress loading condition, applied ATC and result is presented in table 5-3. It is important to mention that Lee and Lau [72] in their work using 27x27 and 35x35 PBGA and Zhang et al. [73] in their work using SMD package reported crack in the same location.



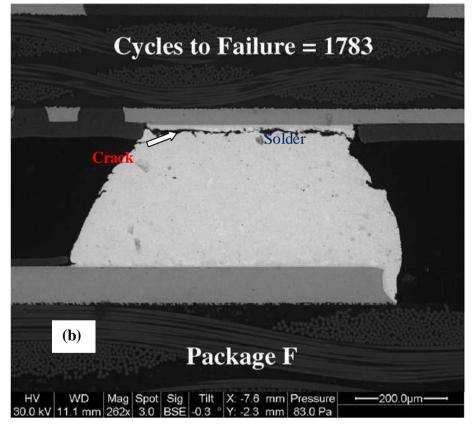


Figure 5-14: SEM image of a solder joint cracked at interface of solder and IMC at die side after being subjected to ATC (a) cracked joint (b) package side crack on (a) 256 I/O BGA (ENIG finish SAC305 solder)

Sources: (a) Arulvanan et al. [89]; (b) George et al. [69]

Tab	le 5-3 Correlation bet	ween modelled ass from liter	sembly and similar exature	perimental works
Correl	ation Index	Xie et al. [27]	George et al. [69]	Simulated assembly
Comp	onent	CVBGA package	Plastic BGA	Flip Chip
	Technology	Solder bumping	Same	Same
	Connection	Daisy chain	Same	Same
e	Bump matrix	Periphery array	Full array	Periphery array
Structure	Pitch (mm)	fine	1.0	0.4572
tru	Die size (mm)	10.5	about 100x140	6.3
S	Bump diameter (mm)	0.250	about 0.6	0.178
	Bump count (I/O)	432.0	256.0	48
	Solder alloy	Sn3.0Ag0.5Cu	SAC305/Sn3.5Ag	Sn3.9Ag0.6Cu
Material composition	Substrate material	Tg FR4 with OSP pad finish	Polyimide with Tg greater that 250°C. ENIG/High- temperature custom board finish	Tg FR4 with OSP pad finish
2	Chip	silicon die	same	Same
Stress	load condition	Component mounted on PCB and subjected to ATC	Same	Same
load		ATC	Same	Same
	One ATC duration (min)	40.0	about 159	47.22
ΤC	Range (°C)	0 to 100	-40 to 185	-38 to 157
LΑ	Ramp (°C/min)	10.0	3.5	15
	Dwell (min)	10.0	15.0	10
Resul	t	Crack in bulk solder at package side	Failure analysis revealed the failure site to be on the package side of the solder joint	Crack at boundary between IMC at die side and solder bulk

Chapter 5: Impact of Component Stand-off Height

5.3.2 Study on plastic work density in FC solder bump joints

Plastic work accumulates over time in solder joints subjected to thermal cycle. It has been reported that the accumulation of change in plastic work from one cycle to the next causes damage in the solder bumped joints. Extensive discussion on this subject in solder joint is done in section 4.3.3. The relationship between the average change in accumulated plastic work and solder region (S_i) is represented in fig. 5-15. The plot shows that accumulated damage increases as the CSH decreases. Although the configurations of B_i have a direct relationship with S_i , the latter has been used in the plot presented in fig. 5-15. The reason for its usage is because the material model used to capture solder plastic deformation is viscoplastic in nature which covers only solder region (IMC has a different material characteristic).

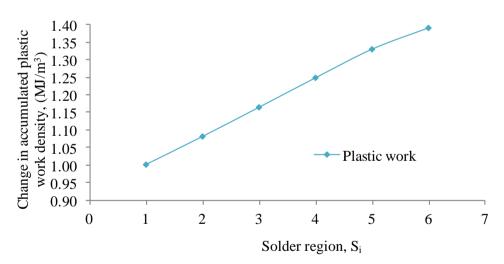


Figure 5-15 Plot of change in accumulated plastic work over solder region

5.3.3 Effect of CSH on fatigue life of FC solder joins

Prediction of fatigue life of solder joint has been discussed in details in sections 2.4.2 and 4.3.5 where Syed's model [52] given in equation (4-19) was used and its adoption and slight modification justified. The utilised Eq. (4-20) is represented again for convenience.

$$N_f = (0.00145 w_{acc})^{-1} \tag{4-20}$$

The required parameter for usage of Eq. (4-20) in this condition is the value of $W_{acc}/\Delta W_p$ for the six bumps. The simulation output values of damage from P_i (*i*=1, 2, ..., 6) are shown in table 5-4. Figure 5-16 plots the values of ΔW_p as a function of P_i and the plot of the relationship between predicted life and B_i is shown in fig. 5-17. It can be seen in fig. 5-17 that the predicted life of FC solder bumped joints decreases as the P_i increases and CSH decreases.

Table 5-4 Relationship among bond pad size, solder bump damage and
predicted life of solder joint

Bond pad size, S_i	Damage in Solder bump (MJ/m ³)	Solder joint life (cycle)
1	1.002	665
2	1.082	616
3	1.165	572
4	1.249	534
5	1.331	501
6	1.391	479

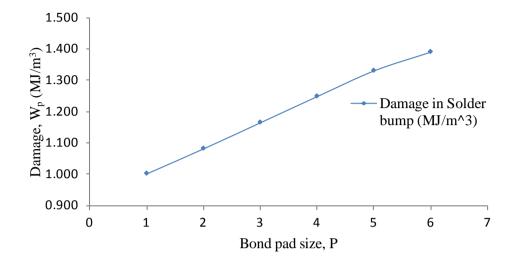


Figure 5-16 Plot of predicted assembly life over pad size

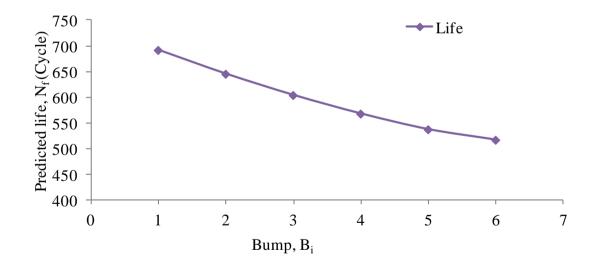


Figure 5-17 Plot of predicted assembly solder joint life over bump

5.4 Conclusions

The effects of component stand-off height (CSH) (controlled by relationship between diameter of PCB bond pad and diameter of die bond pad) on high-temperature reliability of flip chip FC48D6.3C457 lead-free solder joints is studied using FEM tool. In this study, the following conclusions are drawn based on the results of the investigation:

- The reliability of solder joints in FC assembly decreases as CSH decreases.
- The damage accumulated in lead-free solder joint and consequently the reliability of the joint at high-temperature excursions decays exponentially as the CSH decreases in a cubic function.
- Low CSH promotes fatigue cracks at interconnects between FC IMC at die side and solder region.
- The diameter of bond pad on a PCB guarded by solder mask defined (SMD) need be diameter of bond pad on die size specific.
- The diameter of the bond pad on PCB should not exceed 110% of the size of diameter of the bond pad on die for good solder joint integrity at high-temperature excursions.

CHAPTER 6

STUDY OF THE EFFECT OF THICKNESS OF INTER-METALLIC COMPOUND ON DAMAGE AND FATIGUE LIFE OF LEAD-FREE FLIP CHIP SOLDER JOINTS AT HIGH-TEMPERATURE EXCURSIONS

6.1 Introduction

Solder joint is one of the key components of an electronic assembly whose reliability concern increases at elevated temperature of device operation due to the growth of IMC which is formed at the assembly interconnects during reflow soldering of the component. Soldering is a method widely used to attach electronic chip on substrate. It is a general knowledge that solder joints contain IMC at interconnects of Sn-based solder bump and metalized copper bond pads (fig. 2-8). The thickness of IMC layer is known to impact reliability of solder joints in chip level packages.

Extensive experimental investigations are conducted to investigate and determine the reliability of BGA packages at high-temperature applications, however matching complementary numerical studies are needed to fully characterise the effects of the thickness of IMC on solder joint damage and consequently its fatigue life. The potential capabilities of solder bumping as compared to wirebonded technique in terms of electrical advantages will not be completely harnessed especially in chip level packages until thermo-mechanical behaviour of solder to transient thermal load is fully comprehended.

This chapter reports a study carried out on a realistic geometric model of FC solder joints to determine the effect of thickness of IMC on damage and fatigue life of the joints at high-temperature excursions. The whole joint and integral parts of the joint are used in the study which consists of models. The integral parts of a joint are IMC at die side, solder region (refer to chapter 5 and fig. 5-5.), IMC at PCB side. The whole joint is simply called a bump and solder region is simply called solder. The thickness of IMC in the joint is varied from 4 μ m to12 μ m at intervals of 2 μ m as proposed in the work reported by George et al. in ref. [69]. The variation produced five models. Model based on the whole joint is termed

model i bump. Similarly, model based on the solder region is termed *model i solder*. The *i* takes value from 1, 2, 3, 4 and 5. The reliability of each model was estimated using FEM to quantify the effect of the thickness of IMC. The investigation was done by numerous studies and evaluations. The plastic strain, stress and strain energy density of the models of bump and solder are analysed and compared. The concept of hysteresis loop area is employed to characterise and quantify the degree of damage in both the bump and solder models which were compared. Moreover, accumulated plastic work density in the joints of the models is evaluated and also compared. The quantified damage is utilised to predict the life of the various models.

A key contribution of the study on equivalent plastic strain is that the relationship between maximum plastic strain of bump and solder in the models is determined. The study also reveals the hierarchy and trend of accumulation of plastic strain in the models of the solder as ATC progresses. The major finding from the result of the study on equivalent stress is that the response of the models of the bump is significantly different from that of the solder to the induced thermal load. It points out that non inclusion of IMC in the geometric model employed in FEA of solder joint is not appropriate and leads to error in the result of simulation. The evaluation of accumulation of plastic work density in the models reveals that the trend behaviour of damage in the bump is inversely related to that of the models of the solder. Likewise, predicted fatigue lives of the bump of the models and solder joints follow a similar relationship. This finding also supports the earlier proposition on the contribution of IMC to reliability of solder joint.

In summary, this study has demonstrated that the thickness of IMC layer in excess of 10 μ m significantly impacts the reliability of FC solder joint. It also reveals that IMC need be included in geometric model of solder joint employed in FEA of reliability of solder joint in microelectronic assembly.

6.2 Methodology

Geometric models of the FC (fig. 3-3) were built using design modeller package in ANSYS FEM software. The models were input into FEA package and static structural analysis performed on them under the same condition. The project schematic of this structural analysis is shown in fig. 6-1. The schematic shows that the analysis employed is static structural and also that parameter set is utilised. Fig. 6-2 depicts the outline of all the parameters and some part of table of design points. The input and output parameters can be seen in the outline. In addition, a truncated table of design points is also shown. The table of design points is shown in fig. 6-3. The name current in the table is given to the particular set of design points (IMC variation solder joint 1) being simulated. The simulation output results are displayed in it.

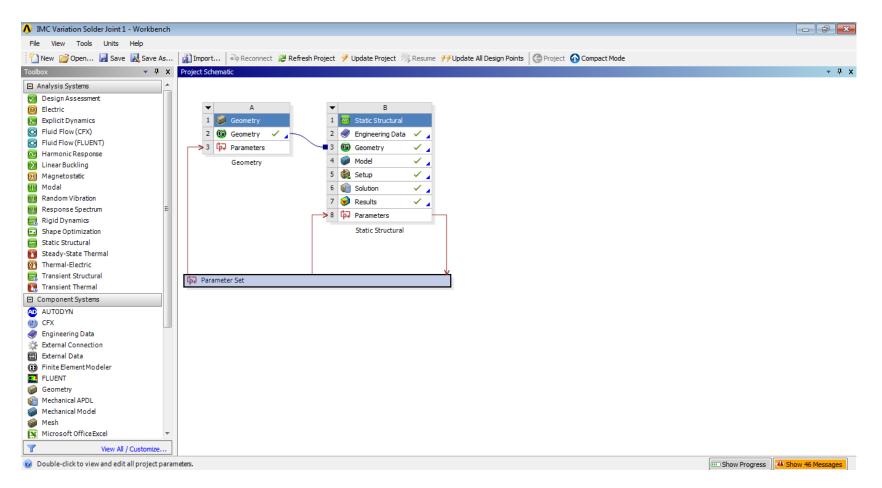


Figure 6-1 Project schematic showing that parametric design were integrated in it

		_	👌 Refresh Project 🦩 Update Project				-	ct 🕜 Compact	Mode			_	
box 🔻 🕂 🗙	Outline	of All Parameters	- - + x			f Design Poin		-	-	_		▼ 中	
Parameter Charts		А	В	L L		A	В	С	D	E	F	G	
Parameters Parallel Chart (all) Parameters Chart	1	ID	Parameter Name	Value	1	Name 💌	P1 - D01Cut 💌	P2-R01 💌	P3 - h1 💌	P4 - Rarc1 💌	P9 - PlaneHeight 💌	P15 - D01A	
Parameters Chart	2	Input Parameters Geometry (A1)			2								
	3	P1	Patert	146	3	Current	146	73	120	148.82	155	146	
	4	-	D01Cut		4	DP 3	160.6	80.3	114	160.07	149	160.6	
	5		R01	73	5	DP 6	204.4	102.2	94	210.27	129	204.4	
	6	Ср РЗ	h1	120	6	DP 7	219	109.5	88	233.24	123	219	
	7	Ср Р4	Rarc1	148.82	*								
	8	ф Р9	PlaneHeight	155									
	9	ιφ P15	D01Add	146									
	10	ф Р30	PCBIMC	4									
	11	 P31	DieIMC	4									
	*	🏟 New input parameter	New name	New expression									
	13	Output Parameters											
	14	🗉 🚾 Static Structural (B1)											
	15	P16	Equivalent Plastic Strain Maximum	0.076594									
	16	P17	Strain Energy Maximum	2.8873E-09	•								
	17	P18	Equivalent Stress 2 Maximum	3.8153E+09	Chart:	No data						1 👻	
	18	P→ P19	Equivalent Stress 3 Maximum	1.8106E+09									
	19	P20	Equivalent Stress 4 Maximum	4.4459E+09									
	20	P21	Equivalent Stress 5 Maximum	3.8153E+09									
	21	P22	Equivalent Stress 6 Maximum	3.0459E+09									
	22	P23	Equivalent Stress 7 Maximum	8.4883E+07									
	23	P24	Strain Energy 2 Maximum	2.8873E-09									
	24	P25	Equivalent Plastic Strain 2 Maximum	0.068791									
	25	P26	Equivalent Plastic Strain 3 Maximum	0	-								
	26	P27	Equivalent Plastic Strain 4 Maximum	0									
	27	P28	Strain Energy 3 Maximum	6.9901E-11									

Figure 6-2 Outline of design parameters showing input and output parameters and some part of table of design

view	Track		- Workbench																					
		Units			1.4								-											
				Impo 👔	rt	p Reconnect	🤁 Refresh Project	🍠 Update Pri	oject 🎋 Resu	me 🍠 Updat	te All Design Points	s 🔁 Return ti	o Project 🕜 Com	npact Mode										
×	able of D	Design Poin																						
		Α	В	с	D	E	F	G	н	I	J	к	L	м	N	0	Р	Q	R	S	т	U	V	х
1 2 3 4	1	N 💌	P1 - D0 1Cut	P2 - R01 💌	P3 - h1	P4 - Rarc1 💌	P9 - PlaneHeight 💌	P15 - D01Add 💌	P30 - PCBIMC	P31 - DieIMC	P16 - Equivalent Plastic Strain Maximum	P17 - Strain Energy Maximum	P 18 - Equivalent Stress 2 Maximum	P 19 - Equivalent Stress 3 Maximum	P20 - Equivalent Stress 4 Maximum	P21 - Equivalent Stress 5 Maximum	P22 - Equiv Stress 6 Maximum	P23 - Equivalent Stress 7 Maximum	P24 - Strain Energy 2 Maximum	P25 - Equivalent Plastic Strain 2 Maximum	P26 - Equiv Plastic Strain 3 Maximum	P27 - Equiv Plastic Strain 4 Maximum	P28 - Strain Energy • 3 Max	Expo
5	2										m m^-1	J	Pa	Pa	Pa	Pa	Pa	Pa	3	m m^-1	m m^-1	m m^-1	J	
6	3	Current	146	73	120	148.82	155	146	4	4	0.076594	2.8873E-09	3.8153E+09	1.8106E+09	4.4459E+09	3.8153E+09	3.0459E+09	8.4883E+07	2.8873E-09	0.068791	0	0	6.9901E	
7	4	DP 3	160.6	80.3	114	160.07	149	160.6	6	6	7	1	7	7	1	9	7	4	7	1	1	1	7	
8	5	DP 6	204.4	102.2	94	210.27	129	204.4	6	6	7	7	7	7	1	7	7	9	7	9	1	1	7	V
9	6	DP 7	219	109.5	88	233.24	123	219	6	6	7	7	7	7	7	1	9	7	1	9	9	1	7	V
10	*																							
20 21 22																								
	hart: No	o data											m					_						
21 22 23 24 25 26 27 28 * 30	hart: No	o data											17											
21 22 23 24 25 26 27 28 * 30	hart: No	o data											н									iii Show Pr	ogress 1 24 Sho	

Figure 6-3 Outline of full table of design points showing design parameter values and some generated values

Chapter 6: Effect of Thickness of IMC

Fig. 6.4 shows IMC at the chip and substrate side in one of the assembled FC joints. The thickness of IMC in the joints was varied from 4 μ m to 12 μ m at interval of 2 μ m. Five models were obtained. Fig. 6.5 depicts the relationship between the models and their IMC thickness (IMCT). Since volume constancy of the bumps is maintained, as the thickness of IMC increases from model 1 to model 5, the volume of solder in the joints decreases accordingly. The volume of solder in the bump is represented as solder region and has been shown schematically in fig. 5-5. The relationship between the volumes of the solder regions of the five models and the models is plotted in fig. 6.6. The method adopted in FEM in this work has been discussed extensively in sections 3.4 and 5.2. The assembly was modelled by adopting the methodology as discussed and the results are presented and discussed in subsequent sections.

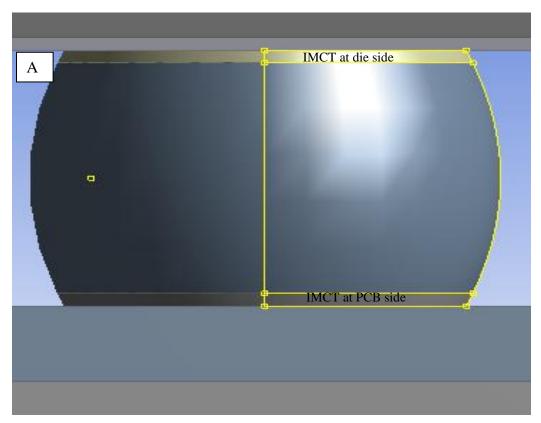


Figure 6-4 (a) Bump showing 6 µm thickness of IMC at both die and PCB sides of the FC assembly without mesh

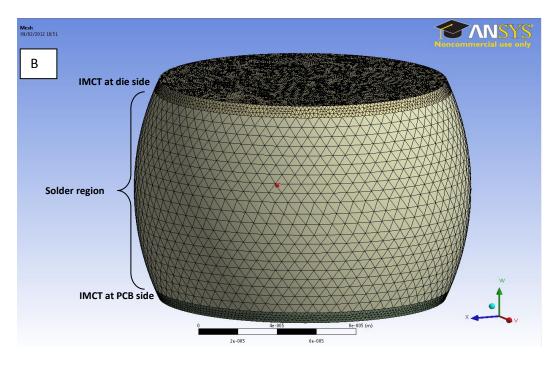


Figure 6-4 (b) Bump showing 6 μ m thickness of IMC at both die and PCB sides of the FC assembly with mesh

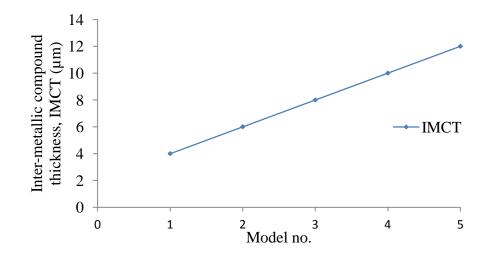


Figure 6-5 Model number plotted as a function of its IMCT

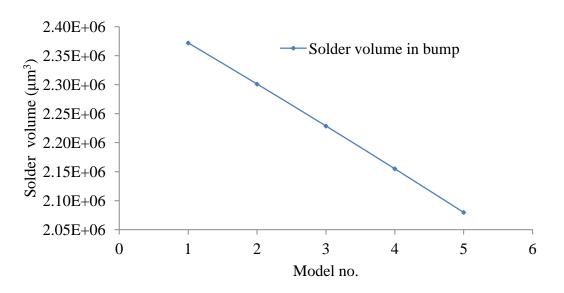


Figure 6-6 Relationship between model number and solder volume

6.3 Results and discussion

The results and their discussion are outlined in six parts. These are: study on equivalent plastic strain, study on equivalent stress, evaluation of hysteresis loop, study on strain energy, evaluation of accumulation of plastic work density and study on FC solder life prediction.

6.3.1 Study on equivalent plastic strain

The strain behaviours of the five models under the same ATC are plotted in fig. 6-7. Model 3 is plotted using the secondary axis. The figure shows in all the models that the amplitude of oscillation decreases as the cycling progresses. It also shows that strain increases from load step one and attains a fairly constant magnitude in the time range of the test. The applied temperature load is constant and supposedly imposes constant stress in the solder joint. At constant applied stress, like creep strain, visco-plastic strain has increased. It is therefore projected that with more cycles, the strain will increase very sharply. This predicted behaviour could be seen in model no. 3 in the figure. Thus, at the test range time, the solder joints operate within primary and secondary visco-plasticity/creep.

The cohesive bond of the solder alloy seems to be weakened by the applied ATC. The solder bulk is more probable to fail due to visco-plastic deformation than fatigue loading since the strain amplitude damps off as the cycle progresses. The figure also shows that solder strain increases from model 1 to 5 with the exception of model 3. The effects of plastic strain deformation on solder joints subjected to the same high ambient temperature will be more significant in smaller solder regions and bumps of the models are plotted as a function of model number in fig. 6-8. The strain magnitudes recorded in the bumps are higher than their corresponding solder values. This finding suggests that assuming the joint to be composed of solder materials only could introduce inaccuracy in the output results of modelling.

The plastic strain accumulated in the solder and the bump increases as the model number increases. The decrease in volume of solder may have been responsible for the increase in maximum plastic strain since solder is the only component of the joint that undergoes strain deformation. This is envisaged as smaller solder volume is expected to undergo more deformation than a larger volume for the same applied ATC and load support. A major deduction from this finding is that progressive miniaturisation can be challenged by reliability. The existence of inflexional maximum point in solder and nonlinearity in the bump indicate possible parameter interactions. Model 3 was excluded in fig. 6-8 as further investigation is needed to explain its extraordinary behaviour.

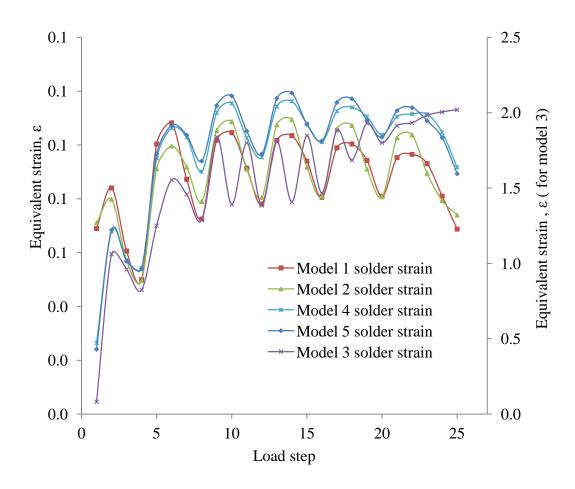


Figure 6-7 Plot of strain behaviour of the five models over load step

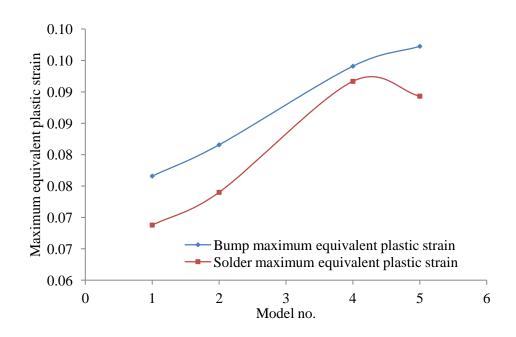


Figure 6-8 Plot of values of maximum equivalent plastic strain as a function of model number for both solder and bump

6.3.2 Study on equivalent stress

Solder and bump stresses in the FC joints are investigated and their relationships with load step are plotted in fig. 6-9 and 6-10, respectively. Although the stress in the alloy is highest in model 3 (fig. 6-9), a trend of decrease from model 1 through 2 and then 4 to 5 can be observed. It is important to note that the differences in maximum stress magnitudes among the models close up as the cycling continues. With reference to fig. 6-7, constant strain could be observed setting in at load step 12. Thus, closing up of the maximum stress magnitudes in the models as the cycling continues may be due to stress relaxation properties of solder. It is projected that, at very many ATC of the joint, the maximum value of stress in the solder in all the models may become the same in value. The deduction from this observation is that miniaturisation is a reliability issue at early stage of solder bump joint operation before the stress relaxation sets in and also at long operations. In fig. 6-10, it can be observed that the bump behaves in a contrary

manner in comparison with the solder to accelerated induced stress. Apart from model 3 whose vertical axis is the secondary, model 5 bump stress is the highest in magnitude and decreases to model 4, 2 and model 1 is the least. This figure shows that there is not much difference in maximum stress magnitude between models 1 and 2. However, model 3 has a very high value and significant difference is observed between models 4 and 5 with model 5 having the highest magnitude. It is also observed that the stress amplitude is the highest in model 5 may be because it has lowest volume of solder to cushion the effects of CTE mismatch. Similarly, it observes highest stress amplitude because it contains the smallest solder volume. The behaviour of the bumps is more realistic than that of the solder models.

A comparison of values of induced stress in solder and bump of the models is plotted in fig. 6-11. Solder stress decreases from model 1 to 5 and bump stress increases from model 1 to 2, decreases to 4 and increases to 5. The behaviour suggests that solder stress decreases with decrease in solder volume. Although the stress behaviour of the bump requires further investigation, a comparison of the two plots has many revelations. At highest solder volume, stress in solder is a maximum and stress in bump is a minimum. The minimum stress in bump is expected. Also, at solder volume lowest, the magnitude of stress in solder is a minimum and that of the bump a maximum. Again, the maximum stress value recorded by bump is anticipated considering the mismatch in CTE of the bonded materials in the assembly. Further investigation is needed to explain explicitly the behaviour of volume of solder in the joint to the accelerated thermal load. Nonetheless, as real bump contains IMC, this investigation has justified the need to include IMC in solder joint geometric models. The assumption that solder bumped joint is composed of only solder may not be correct and may have introduced inaccuracies in the modelling results previously carried out with that notion.

The concern in this situation remains that plastic damage in solder joint is captured using solder plastic deformation models (Creep/Anand) which serves as the bases for most solder joints life prediction models. IMC is a component of the joint and has contributed to bump stress. It is pertinent to recall that most joint failures occur at the interface of solder bulk and IMC at the chip/package side. Therefore, model based on stress may predict life of solder joint very differently from the ones based on plastic deformation of solder. Moreover, damage in bulk of solder may not be responsible for the fatigue life of the solder joint. The CTE mismatch between solder and IMC at their interconnects may have more influence than plastic deformation in the bulk of solder in driving solder joint failure.

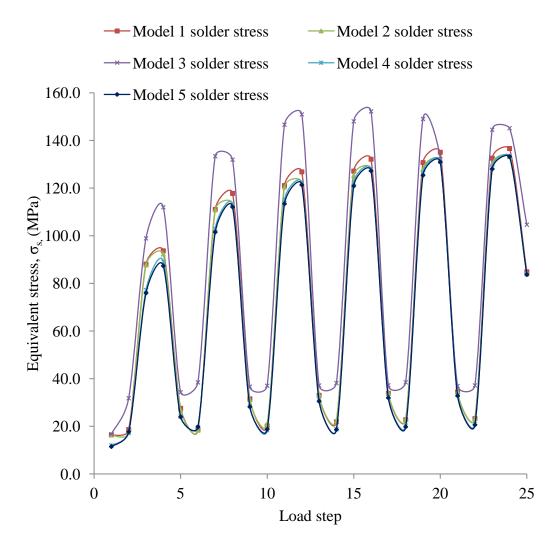
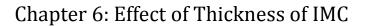


Figure 6-9 Plot of behaviour of stress in solder over load step for the models



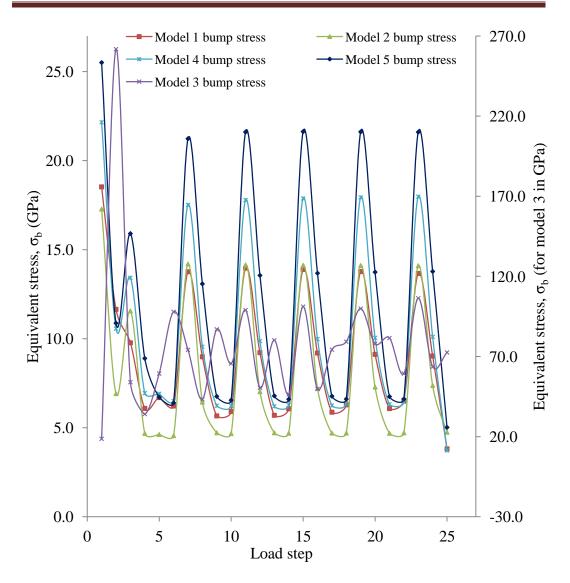


Figure 6-10 Plot of behaviour of stress in bump over load step for the five models

Chapter 6: Effect of Thickness of IMC

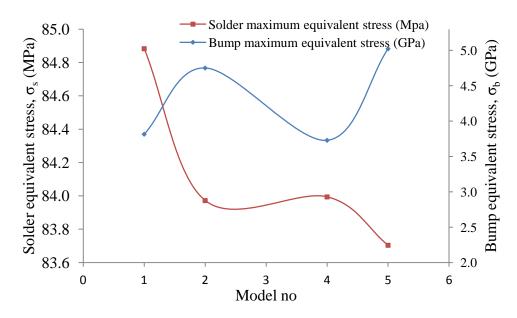


Figure 6-11 Plots of solder and bump stresses as function of model

6.3.3 Evaluation of hysteresis loop of FC bump joints

The visco-plastic response of solder bump to thermal load is captured in the plot of the relationship between solder stress and strain. A typical stress-strain plot of the most critical SnAgCu solder joint in the assembly is shown in fig. 6-12. It can be seen in the figure that as the plot continues, the trend evolves into loop. The ring so formed is called hysteresis loop. It develops because the nature of the applied temperature load is cyclic which is made up of extension and compression load strokes. The strain energy density dissipated per cycle can be calculated from the area of the loop. In addition, the loop is used to predict the state and the behaviour of solder in the bump joint. Its other significance is that it indicates stabilisation of damage in the bump.

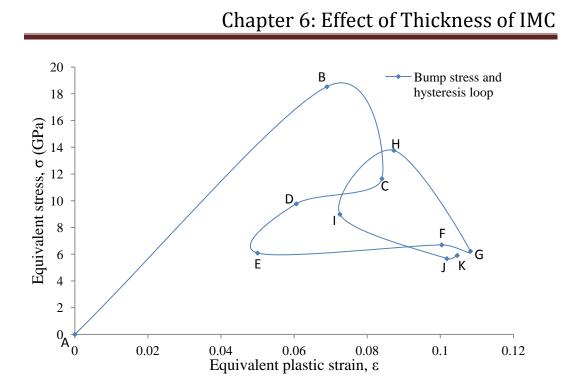


Figure 6-12 Plot of bump stress and hysteresis loop

The critical bump was initially unloaded at point A. This is the unstressed state which is the condition of the bumps in as-reflowed FC mounted on the substrate. On application of ramp up temperature load and at the end of first load step, the state of the bump is defined by the conditions at point B. This step induced the maximum stress and maximum plastic strain rate in the solder. It is recognised as the thermal shock load step. Under the influence of first high-temperature dwell region (step 2 in fig. 3-6) at which the solder alloy soaks to attain uniform temperature distribution, the stress level decreases sharply while the strain only increases marginally in comparison. Owing to the fact that the change in strain in this load step in very minimal, it is viewed that the solder is under constant applied strain. The resultant quick decrease in stress magnitude is identified as stress relaxation. Stress relaxation has been recognised as one of the properties of solder alloy particles attaining thermal equilibrium with one another. Potentially, thermal equilibrium redistributes localised stresses in the material. First ramp

down load CD (step 3, fig. 3-6), induces contraction in the solder which continues until end of lower dwell region (point E, fig. 3-6). The bump stress decreases by about 67.0% of its yield stress to a very low value at the end of this lower dwell region. Load steps 5 and 6 (fig. 3-6) corresponding to points E to G, produce very large strain at fairly constant stress. Under constant applied stress, creep strain increases. This is another very important property of solder. Since visco-plasticity was used to model the solder response, it is actually, the visco-plastic strain that increases. Similar to creep strain, under constant applied stress, visco-plastic strain increases. From point G onwards, the response of the solder to the thermal cycling changes. The response becomes a loop (points G-H-I-J-K) which is progressive and also similar in trend (figs. 6-14, 6-16 and 6-17). Point G is at stress level of 6.223GPa and point K has stress magnitude of 5.911GPa. The percentage change in thermally induced stress at these states in the loop is plotted in fig. 6-13. A comparison of the positive and negative hillocks shows that the negative mound is greater than the positive. This plot shows that the induced stress in the bump is not totally relieved at the end of the cycle and the residuals accumulate over many cycles and drive solder joint to failure.

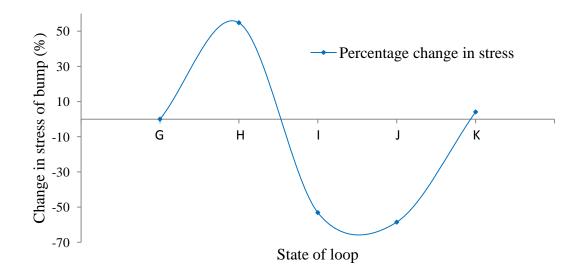


Figure 6-13 Plot of stress state of solder bump under thermal cycle (in percentage)

Fig. 6-16 shows the hysteresis loops of solder region in the most critical joints while fig. 6-17 is the hysteresis loops of the same critical bumps. The bump loop is used instead of solder loop in the hysteresis study because Amalu et al. [1] have reported that incorporation of IMC in the geometric model of solder bump joint increases the accuracy in predicting bump reliability.

The plot in fig. 6-12 is quite different from the plot of typical strain controlled cyclic stress-strain test results. Mustafa et al. [77] have reported the behaviour of SAC solder uniaxial specimen which was subjected to strain controlled cycling with strain limit of ± 0.0018 . The difference between uncontrolled and controlled strain deformation in material is mainly in the trend behaviour of the plotted readout data points.

Point G marks the onset of stabilisation of the solder bump under investigation. The area covered by the hysteresis loop represents the energy density the bump observed per cycle during the temperature cycle loading. Energy dissipation occurs during cyclic loading due to yielding and occurrence of visco-plastic deformations. The configurations of the loop of the models (excluding model 3) are presented in fig. 6-14. Model 3 is excluded because further study is required to explain its anomalous behaviour observed in this study.

To characterise and empirically model the evolution of the hysteresis loops in the models, so as to determine the area of the enclosure, a pair of empirical models is developed. The development of the models involves the partitioning of the loop into two parts as can be seen in fig. 6-14.

The function describing the trajectory of the loops is designated as $\sigma_{i(Mj)}(\varepsilon)$ and defined by the expression:

$$\sigma_{iMj\{\substack{i=1 \text{ or } 2\\ j=1,2,4,5}}(\varepsilon) = A + B\varepsilon^2 + C\varepsilon^3 + D\varepsilon^4 + E\varepsilon^5 + F\varepsilon^6. \quad \text{for } \varepsilon_{1Mj} \le \varepsilon \le \varepsilon_{2Mj}$$

where *i* indicates the trajectory. When *i* is 1, the path is compression (G-H-I) and when *i* is 2, the path describes extension process (I to G). The *j* identifies the model number. The constants (A, B, C, D, E and F) are determined by fitting the curve to the set of computer output data from modelling. Polynomial function is employed in fitting a curve to the trajectory because it gives a better approximation and a high value of correlation coefficient (\mathbb{R}^2) than all other functions tried. MATLAB version 7.11 was employed to fit the curve which was verified using Microsoft Excel. The functions and the paths they describe can be seen in fig. 6-14. If the hysteresis loop area is defined as ΔW_j then it can be evaluated using:

$$\Delta W_j = \int_{\varepsilon_1}^{\varepsilon_2} \left[\sigma_{1Mj}(\varepsilon) - \sigma_{2Mj}(\varepsilon) \right] d\varepsilon \qquad 6-2.$$

This area represents the volumetric strain energy density (J/m³) dissipated per cycle loading. There is a strong correlation between the loop area and the accumulated damage in solder joint. The loop area generated from Equation 6-2 and computer output data on solder plastic work computation are used to draw comparison on the behaviour of the two quantities. The plot of the reduced value of evolution of solder and bump hysteresis loop area with model number is shown in fig. 6-15. For the bump, the values, which are areas of the hysteresis loops, were originally, determined from the plots of the hysteresis loops before being reduced. Reduced value is used because the study is comparative. The plot shows that the bump energy density decreases from model 1 to 2 and increases afterwards while that of solder decreases monotonically from model 1 to 5. The former result indicates that the hysteresis loop size of solder region decreases with

increase in IMC in the joint. Bump exhibits a different behaviour. The dissimilar behaviour of bump in comparison with solder in solder region points out a possibility of interaction between solder volume and IMC thickness during solder joint operations. Another reason could be from computer error as a result of handling very large volume of data. For the bump, models 1 and 5 have higher area compared to 2 and 3.

To better understand and properly explain the bump and solder energy densities evolution during thermal cycling, the hysteresis loop of bumps and solder volumes of models are plotted in figs. 6-16 and 6-17.

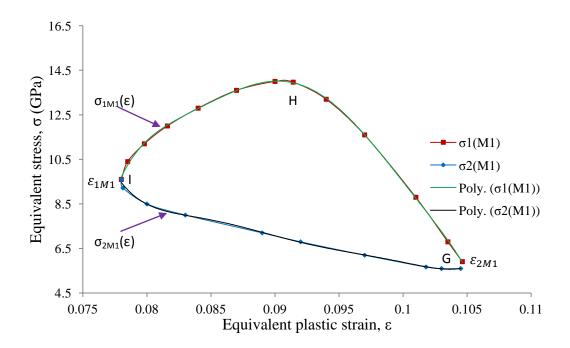


Figure 6-14 (a) Evolution of hysteresis loop in the different bump models

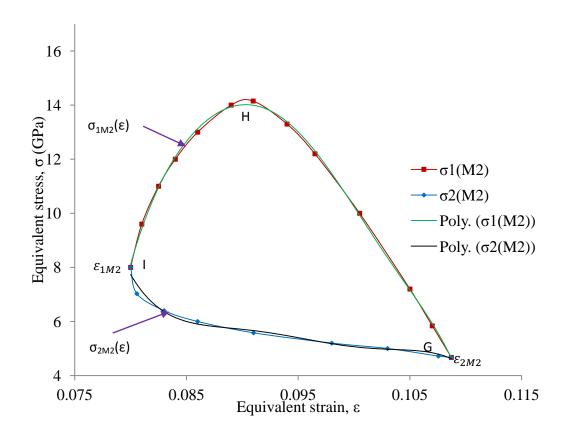
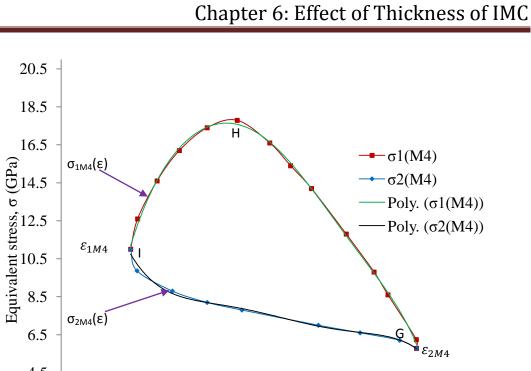


Figure 6-14 (b) Evolution of hysteresis loop in the different bump models



4.5 0.09 0.095 0.1 0.105 0.11 0.115 0.12 Equivalent strain, ε

Figure 6-14 (c) Evolution of hysteresis loop in the different bump models

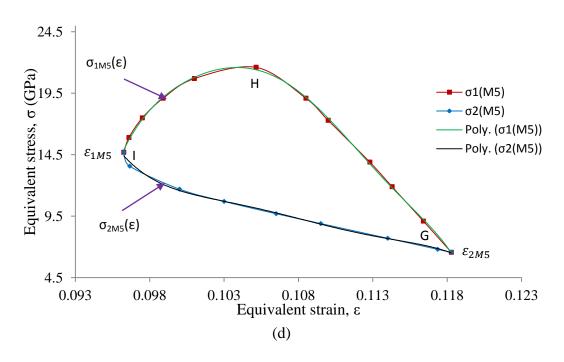


Figure 6-14 (d) Evolution of hysteresis loop in the different bump models

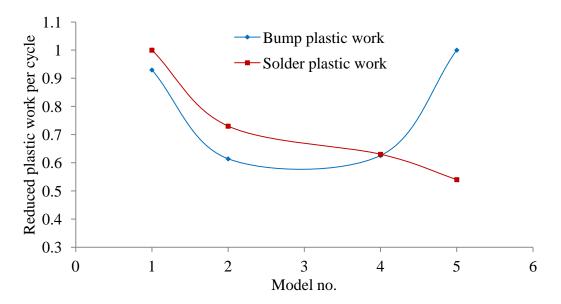
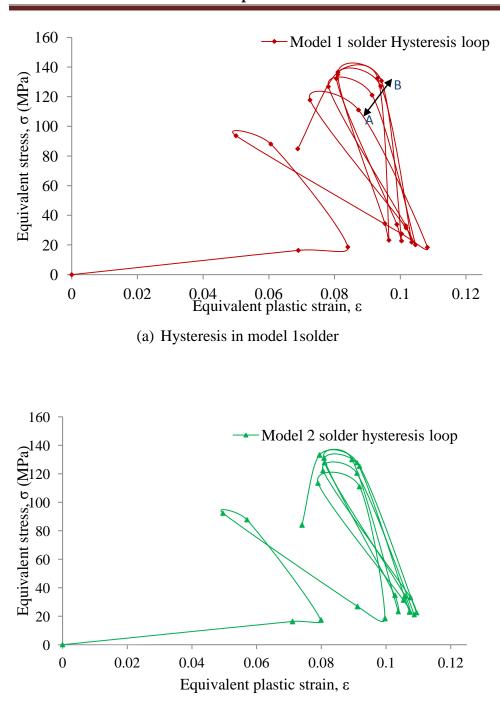


Figure 6-15 Plot of reduced plastic work of solder joint

Fig. 6-16 and 6-17 illustrate sample plots of the cyclic stress-strain behaviour of solder and bump in models, respectively. Each plot represents a particular model. The responses of solder and bump in models (1, 2, 3, 4 and 5) are plotted in figs. 6-13 and 6-14 (a, b, c, d and e) respectively. Similarly, the responses of bump in models (1, 2, 3, 4 and 5) are plotted in figs. 6-14 (a, b, c, d and e) respectively. Comparing the plots of solder response among one another, the plots demonstrate remarkable similarity in pattern but differ in location. Similarly, bump hysteresis loop plots exhibit the same behaviour. It can be observed per model (with the exception of model 3) that the maximum marginal plastic deformation of solder per thermal cycle loading closes up as cycling progresses (Range A to B in fig. 6-16 (a)). In addition, it is detected that across the models, the change in maximum plastic deformation at minimum stresses over many thermal cycles decreases as model number increases (fig. 6-22). Another finding is that the maximum deformation, at fairly constant minimum stress, increases as the model number increases (base of the loops in fig. 6-22). This finding points out that, at the same equal loading conditions, smaller volume of solder bump joint experiences higher plastic strain deformation. Solder volume is therefore a critical reliability concern

when visco-plastic damage is the interest and thus miniaturisation will impact solder joint reliability in micro HTE. The reduction of loop size in solder response suggests that damage accumulation is mitigated as IMC thickness increases and solder volume decreases. However, it is suggested that this trend is apparently due to the fact that there are drops in yield stress and ultimate strength of the solder materials with solder volume (see $S_{ol Miv}$ of fig. 6-18).

The reduction in bump loop size from model 1 to 2 and subsequent increase to model 3 and then 4 (fig. 6-15) and in comparison to bump yield stresses in fig. 6-19, seems to indicate that bump hysteresis loop area is not solely dependent on the solder yield stress. While the trend in plastic deformation of the critical bumps of the models at their yield points (fig. 6-19) is the same as that of solder models, the corresponding equivalent stress of the bumps increases much higher. In contrast to the solder models, model 5 bump is the highest followed by 4 and model 2 is the least. This finding supports the claim that increase in thickness of IMC negatively impacts solder joint reliability. The other importance of this finding is that it reinforces the author's previous report [1] that non inclusion of IMC in the geometric model of solder joint is inappropriate and introduces inaccuracy in the modelling result. It is important to note that, as the IMC percentage by composition in the bump increases from model 1 to 5 and percent volume of solder in the bump decreases accordingly (fig. 6-20), the magnitude of equivalent bump plastic strain at yield stress decreases significantly while bump yield stress increases considerably (fig. 6-21). It can be inferred that both bump yield stress and strain are strongly dependent on the volume percentage by composition of IMC in a joint. Unlike bulk solder with constant yield stress, this observation emphasises the fact that the behaviour of bulk solder in strain controlled experiments is not adequate for full quantitative damage characterisation and modelling of evolution of hysteresis loop in a FC lead-free solder joint.



(b) Hysteresis in model 2 solder

Figure 6-16 (a and b) Plot of hysteresis in solder in joint showing the hysteresis in model 1solder and the hysteresis in model 2 solder

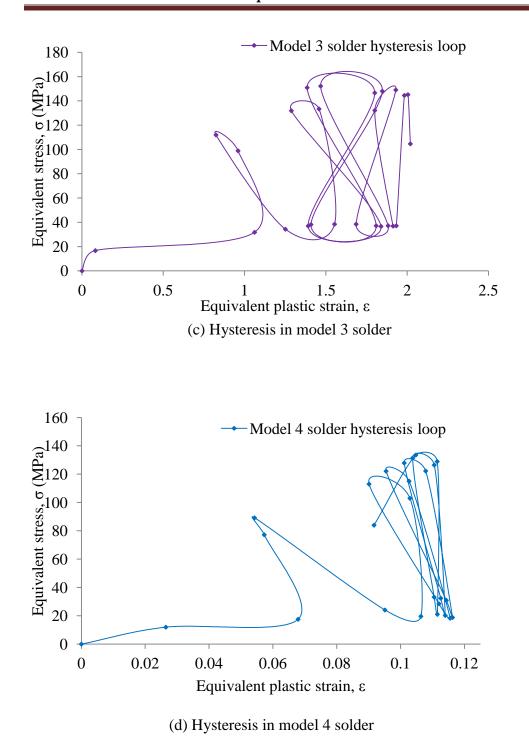
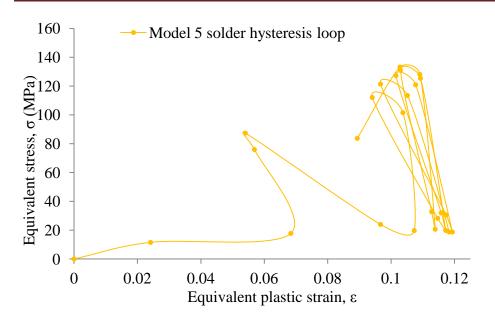
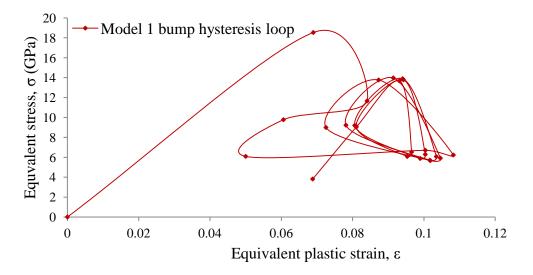


Figure 6-16 (c and d) Plot of hysteresis in solder in joint showing the hysteresis in model 3 solder and the hysteresis in model 4 solder



(e) Hysteresis in model 5 solder

Figure 6-16 (e) Plot of hysteresis in solder in joint showing the hysteresis in model 5 solder



(a) Hysteresis in model 1bump

Figure 6-17 (a) Plot of hysteresis in solder bump in joint showing the hysteresis in model 1bump

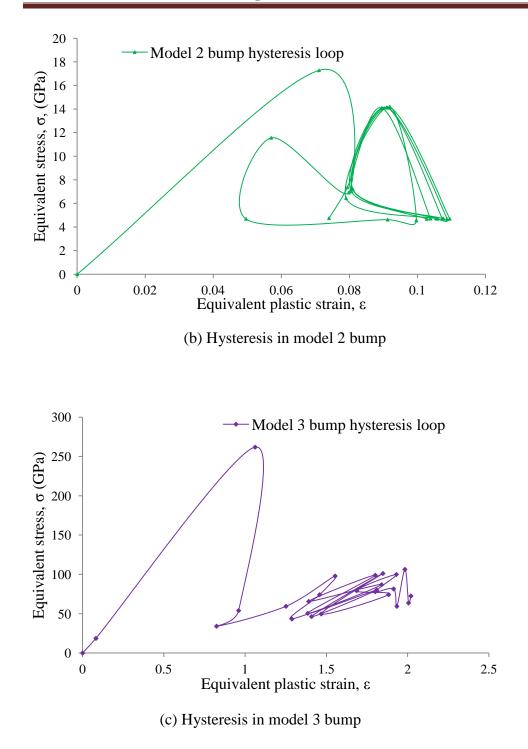
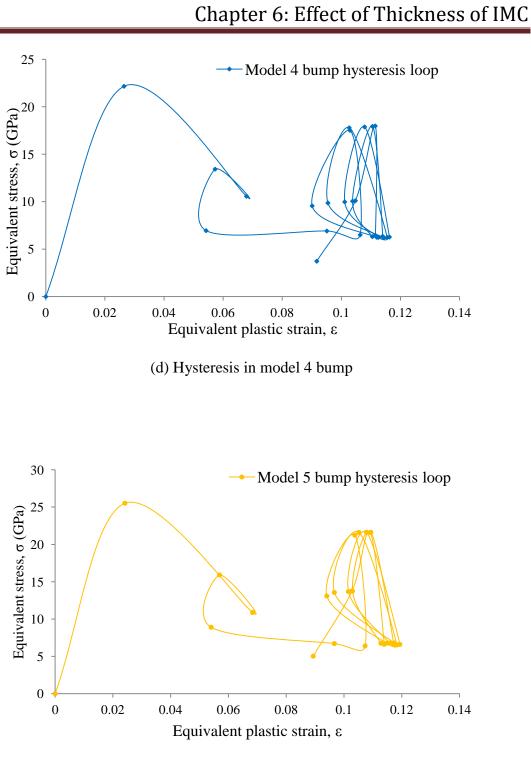


Figure 6-17 (b and c) Plot of hysteresis in solder bump in joint showing the hysteresis in model 2 bump and the hysteresis in model 3 bump,



(e) hysteresis in model 5 bump

Figure 6-17 Plot of hysteresis in solder bump in joint showing the hysteresis in model 4 bump and the hysteresis in model 5 bump

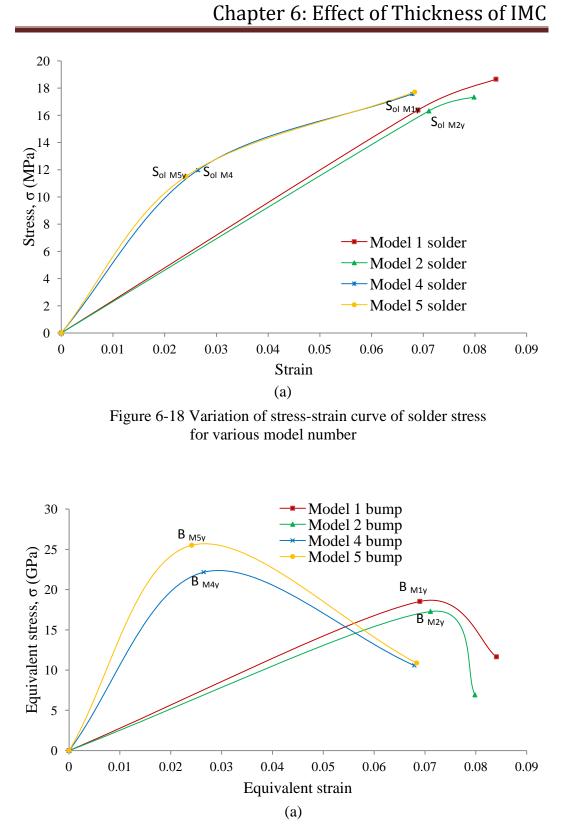


Figure 6-19 Variation of stress-strain curve of bump stress for various model number

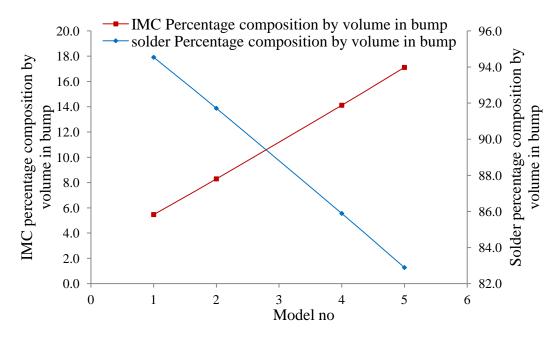
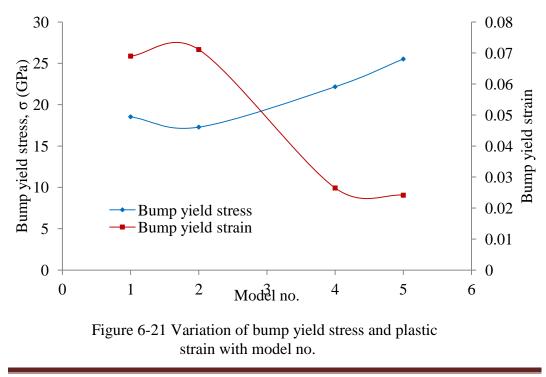
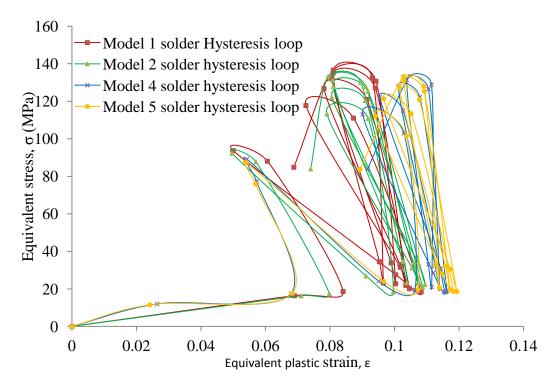


Figure 6-20 Plot of variation of percent by volume of IMC and solder in bump with models



Chapter 6: Effect of Thickness of IMC

The plot of hysteresis loops of solder and bump models on the same axes are shown in fig. 6-22. The character of damage in solder model is represented in fig. 6-22(a) and bump model in fig. 6-22(b). This plot allows a visual comparison to be made among the models. The distinctive character of accumulation of plastic work in the models can be observed. It is believed, based on the result of this work, that the size of the area of the hysteresis loop is not the critical reliability parameter but the position of the loop in the stress-strain plot. To study how the position of the loop determines the integrity of the joint, the hysteresis loop for models of solder and bump are plotted on the same axes in fig. 6-22. It is easily seen that both the plots exhibit similar lateral displacement in the positive strain axis. Contrary to decreases in stress level from model 1 to 5 in solder response, the bump increases in stress magnitude. This observation underscores the need to include IMC in the geometric model and accentuates the possibility of inaccuracy in result of model studies when IMCT is not incorporated. At the smallest solder volume and thickest thickness of IMC, maximum stress and strain are induced in the joint. It is therefore envisaged that both visco-plastic deformation and damage by stress inducement drives failure in miniaturised FC solder joint at high temperature operations.



(a) solder hysteresis loops of models 1, 2, 4 and 5

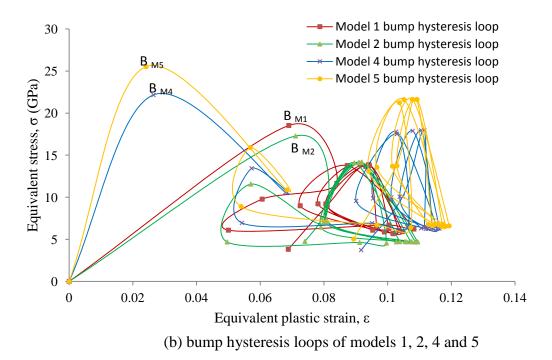
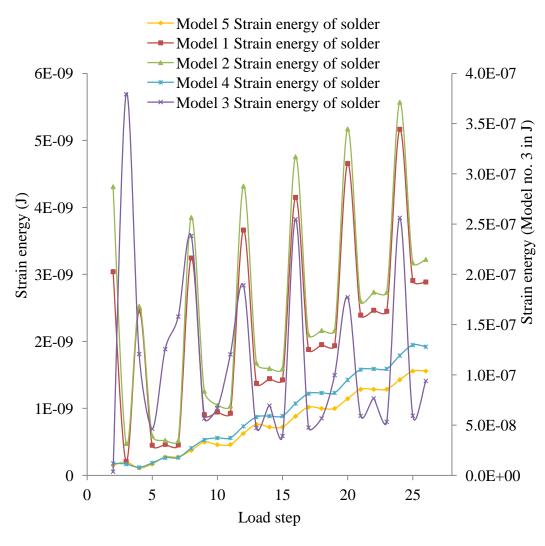


Figure 6-22 Plot of hysteresis loops of models showing the solder hysteresis loops of models 1, 2, 4 and 5 and bump hysteresis loops of models 1, 2, 4 and 5

6.3.4 Study on strain energy of FC bump joints

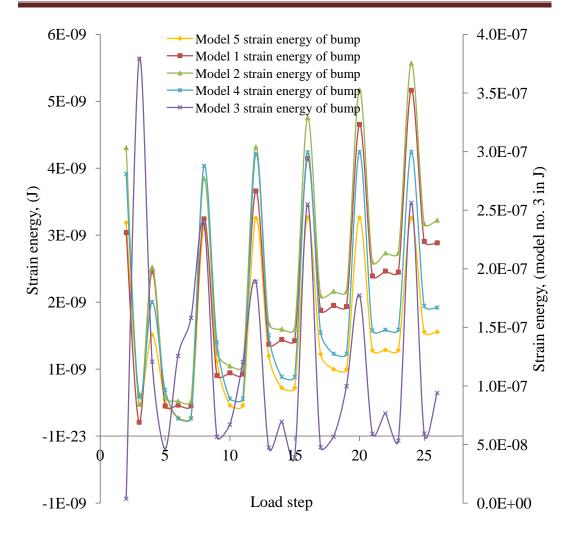
Introduction and discussions on strain energy are made in section 4.3.4. The solder and bump strain energies of the models used in the investigation in this chapter is plotted in fig. 6-23. Owing to the large strain energy values of model 3, its strain energy values are plotted with the secondary axis. Fig. 6-22 (a) shows in decreasing order of magnitude the models strain energy. The sequence is: model 2, 1, 4 and 5. It can be seen in the figure that models 1 to 3 have very high magnitude of strain energy and strain energy amplitude whilst models 4 and 5 have very low values. The inference is that while a combination of fatigue and plastic deformation drive the failure in models 1 to 3, failure of models 4 and 5 will predominantly be dominated by plastic deformation. Thus, very small solder volume of solder bumped joints assumed to consist of only solder without IMC is very unlikely to fail in high temperature excursion by fatigue derived failure mechanism. Fig. 6-23 (b) is similar to fig. 6-23 (a) except in the behaviour of models 4 and 5. The figure 6-23 (b) shows that all bump sizes in the models in addition to observing plastic deformation experience high amplitude of cyclic accumulated strain energy.



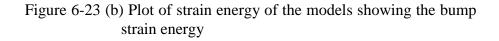
(a) Solder strain energy

Figure 6-23(a) Plot of strain energy of the models showing the solder strain energy

Chapter 6: Effect of Thickness of IMC



(b) Bump strain energy



6.3.5 Evaluation of accumulation of plastic work density in FC bump joints

The relationships between plastic work density accumulated in the joints of the models and thermal cycle number employed in the ATC are plotted in fig. 6-24 while the changes in plastic work density per cycle in the joints of the models as a function of the number of ATC are plotted in fig. 6-25. The concept of plastic work has been discussed previously in sections 4.3.3 and 5.3.2. The ANSYS software code used in computing the magnitude of the change in plastic work is given in Appendix and the basic equation is given in equation 4-18.

The models in fig. 6-24 exhibit identical linearly increasing trend behaviour as the cycle progresses, however the value of the plastic work at the data read out points are different. Model 1 has the highest value which decreases to model 2 and then 3 and model 5 recorded the lowest value. The plots in fig. 6-25 show that model 1 recorded the highest damage followed by model 2 and then 3 with model 5 the least. It can be seen from this figure that the change in the value of this parameter from model 1 to 2 is very significant and similarly, the change from model 4 to 5 is considerable too. The value of the parameter in models 2, 3 and 4 are very close – suggesting that as the IMC percentage composition by volume in bump increases linearly and the solder percentage composition by volume in bump decreases in the same progression (fig 6-20), their combined effects on joint damage is not observed in the same pattern. This finding suggests the existence of parameter interaction which can be harnessed towards the improvement of solder joint integrity and reliability.

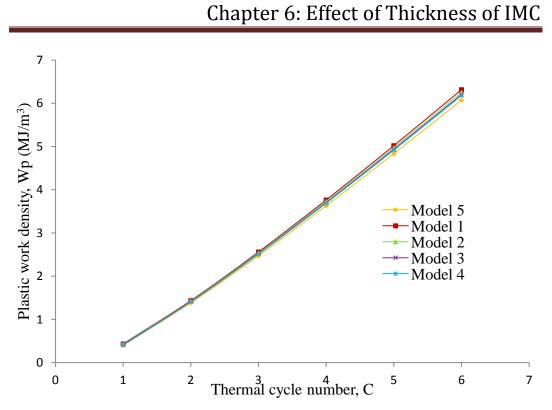
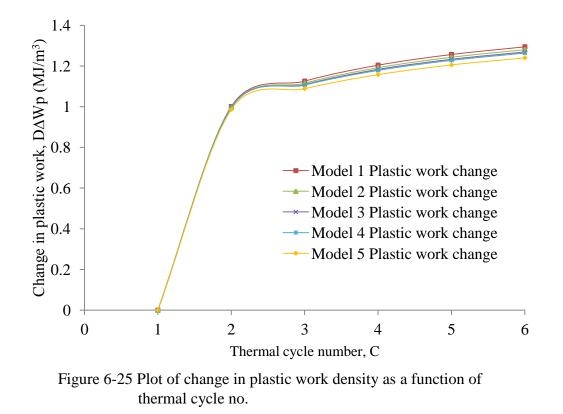


Figure 6-24 Plot of plastic work density as a function of thermal cycle no.



Chapter 6: Effect of Thickness of IMC

It is important to note that the physics of the computational model employed in the evaluation of plastic work density is based on visco-plasticity. Thus, only solder plastic work is taken into consideration. Since this computation is based on the solder, the plotted graph suggests that the lower the solder volume and in turn higher thickness of IMC, the smaller the damage in the joint. This deduction may be misleading. It may be a major flaw associated with the approach utilised to determine damage in solder joint since the parting force due to CTE mismatch between the solder and IMC has not been properly taken into consideration by the constitutive equation employed to capture the plastic deformation of the bulk of solder. Some researchers including Ma et al. [78] has expressed concern on the inadequacy of existing models in predicting accurately MTTF of solder joints subjected to ATC. In their recent study, Ma et al. [78] reported that the significance of their finding will help to explain the unsatisfactory of various current developed models based on solder joints fatigue only and give rise to new models for more accurate fatigue life prediction. The chapter points out that inclusion of IMC in the geometric model of solder joint will increase the accuracy of predicted solder joint fatigue life. However, the inclusion of IMC will demand the development of new fatigue models.

To demonstrate the contribution of thickness of IMC to damage of bump joint, the change in plastic work from cycle to cycle need to be determined. Since the existing equation 4-18 is based on solder, the only available method would be to use the hysteresis loop area. This involves determination of the change in the loop area from cycle to cycle. Owing to the fact that the determination of loop area is by approximation and the change in loop area from cycle to cycle is very small, it is extremely difficult to use hysteresis loop to compute the change and determine the damage in bump joint. Nonetheless, as an approximation, solder plastic work of fig. 6-15 and 6-26 were used to determine the value of damage in the bump. These values were generated as computer output where the code in appendix was

employed. For utilisation of this approach, it is assumed that a linear relationship exists between solder and bump damage. The reduced plastic work of solder (fig. 6-15) and its damage (fig. 6-26) were used to map the reduced plastic work of bump (fig. 6-15) into its quantitative value, plotted in fig. 6-26. The reduced plastic work of the bumps is obtained from the area of the hysteresis loop. It can be seen in the plot that damage in bump becomes critical with decrease in solder volume and increase in percentage by volume of IMC in bump joint.

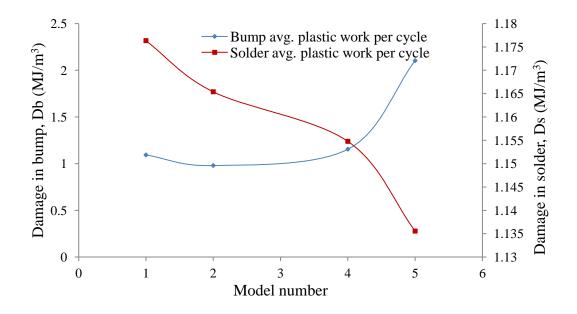


Figure 6-26 Plot of change in plastic work density as a function of model no.

6.3.6 Study on FC solder joints and bump joint life prediction

Many sections including 2.4.2, 4.3.5 and 5.3.3 have discussed the concept of solder joint life prediction models. Predicting the life of the models based on equation (4-20), the equation is recalled:

$$N_f = (0.00145 w_{acc})^{-1} \tag{4-20}$$

The read out data points in fig. 6-26 were input in equation (4-20) and the resulting values were plotted in fig 6-27. With reference to fig. 6-27, solder joint fatigue life increases monotonically as solder volume decreases. This behaviour does not truly represent the real life behaviour and this work calls for development of new models and approaches for accurate solder joint fatigue life prediction. The reduced values of plastic work in bump (fig. 6-15) were scaled up by proportion using the computer output values in the plot shown in fig. 6-26. The generated values were used to plot bump joint life in fig. 6-27. It can be seen in the plot that model 1 has the highest value but model 2 and model 5 have the lowest value of joint life. This finding indicates that the growth of IMC in a solder joint which brings about the decrease of solder volume adversely impacts solder joint reliability especially at high temperature applications and excursions of solder joint where thickness of IMC is not negligible and can grow up to 6μ m in thickness.

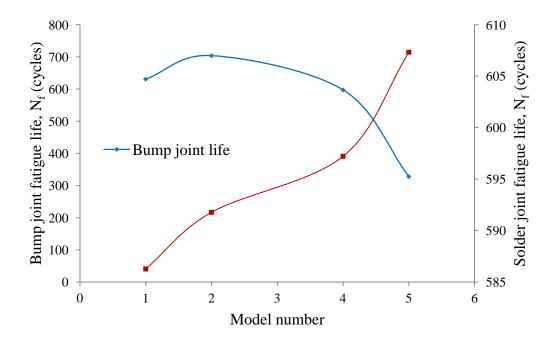


Figure 6-27 Plot of life of solder joint and bump joint as a function of model number.

6.4 Conclusions

High-temperature reliability study on a FC package has been conducted to investigate the impact of the thickness of IMC on reliability of lead-free FC48D6.3C457DC solder bump joints. Based on the results of this study, it is found that the thickness of IMC layer plays significant roles in the life of solder joints in a FC assembly. The findings signify that IMC need to be incorporated in modelling reliability study of solder joint. In addition, the following conclusions are drawn from the results:

- The IMC thickness has strong effect on loop size and thus the bump accumulated damage.
- Very thin and very thick IMC negatively impact solder joint reliability.
- The magnitude of plastic strain damage in solder bump depends on the volume of the joint, volume percent of IMC and solder region.
- A combination of fatigue damage which occurs at early period of device operation and visco-plastic damage which is accumulated during the operation of the assembly drives failure in realistic FC solder joints.
- At long operating time, damage and failure of solder joint will be majorly driven by visco-plastic damage rather than fatigue loading.
- Increase in volume percent of IMC in a joint increases the joint induced stress.
- Visco-plastic based models are insufficient to predict correctly solder joint life.
- The inclusion of IMC will demand the development of new fatigue models.

CHAPTER 7

PREDICTION OF DAMAGE AND FATIGUE LIFE OF HIGH-TEMPERATURE FLIP CHIP ASSEMBLY INTERCONNECTIONS DURING OPERATIONS

7.1 Introduction

The determination of real value of damage/plastic work density in solder joints from computer numerical modelling and its usage in fatigue life prediction models based on accumulated energy density is critical to improving the accuracy of predicted life of solder joint.

This chapter presents a study on the magnitude of accumulated equivalent stress in solder bump joints of FC components mounted on a substrate. It additionally presents an investigation on the magnitude of damage in the realistic FC joints which it compares with the unrealistic model of the same joints assumed to be made of only solder (without IMC). Basically, this investigation extends the study reported in chapter 4 and chapter 6. While the study in chapter 4 deals with plastic work and strain energy density in both the realistic and unrealistic bump joint and the investigation reported in chapter 6 studies the effect of thickness of IMC on damage and fatigue life of the realistic joint, it is one of the aims of this chapter to utilise hysteresis loop concept to explain the damage mechanism in both the realistic and unrealistic solder bump joint. Further presentation in the chapter focuses on the effect of number of thermal cycles on the magnitude of damage accumulated in the FC joints. The trend behaviour of accumulated damage and fatigue life per cycle over many ATCs are also studied. The study on the equivalent stress of the joints was carried out to provide better understanding of the magnitude and amplitude of stress accumulation on the materials of the joints. A deeper understanding will be useful to predict accurately the site of failure. It will be a valuable tool in knowing and explaining the mechanism of failure of a joint. The investigation on the nature of hysteresis loop of the realistic and unrealistic interconnects strengthens the findings reported in chapters 4 and 6.

The number of cycles utilised in ATC varies according to researchers. The degree of damage accumulated in a solder joint depends on the cycle number utilised in the ATC. The magnitude of damage input to an accumulated energy density fatigue model determines the N_f or MTTF which the model will yield. Six ATCs were simulated using FEM and a projection to 30 cycles was made by fitting in a function to the six ATCs. This function was used to determine the effect of cycle number on the magnitude of accumulated damage in the most critical joint.

The commercial ANSYS software based on three-dimensional FEA was employed in this study. The solder bumps deformation is modelled using Anand's visco-plasticity (see sections 2.4.1.2) and performance of all other materials in the assembly was captured with appropriate material models. It was observed that difference in stress magnitude and amplitude between IMC at the die side and solder bulk was highest and the presence of IMC in the joints increases bump damage which occurs in three stages during temperature cycle loading. These results indicate that while IMC impacts solder joint reliability, the bond at interconnect between IMC at the die side and solder bulk is most vulnerable to fatigue crack initiation and propagation. A new methodology to find accurate solder joint damage is presented. The findings show that average of damage from cycle of hysteresis loop stabilisation to cycle of onset of tertiary damage demonstrates potential of being adequate in determining magnitude of the solder joint damage. However, considering that damage evolution is in three-phase, the researcher propose the use of polynomial function to estimate plastic work damage in FC solder joints.

7.2 Background

The ICs are used to build crucial complex control systems that must be operational in high-temperature harsh environment typically found in many sectors which include aerospace, automotive, oil and gas well-logging and defense [5]. The demand on thermal cycle life of sensors and control devices which

operate in these systems is huge due to high safety critical requirement of these sectors. Characteristic oil well operates at about 150°C. Parmentier et al. [79] reported that 80% of oil-wells operate below 150°C with 95% of the wells functioning under 175°C ambient temperature. In the same paper, they also reported that operations such as traditional wire line logging last for two to six hours, measurement while drilling (MWD) last up to 500 hours and greater operating period of more than 40,000 hours is possible for permanent gauges and intelligent completions. In automotive applications, the under-the-hood HTE and specifically on-engine HTE can observe ambient temperature in the rage of -40 °C to +150 °C [6]. Usually, high melting point solders (HMPs) are deemed suitable for interconnects of components in HTE. These HMPs are expensive and have a limited supplier group. Consequently, they are rarely employed in the manufacture of HTE devices which operate in the ambient temperature range of 125 °C to 175°C. A good substitute has been SnAgCu alloy solder with melting point of about 217 °C. This solder is used in the manufacture of FC. Owing to the fact that lead-free adoption and usage in solder bumping technology is still new, investigations documented in literature on SnAgCu solder alloy behaviour at elevated temperature is scarce and not complete. Although George et al. [69] have reviewed literature on thermal cycle test standards utilised in ATC and also extended this review to the response of lead-free solder alloys in different packages/chips to applied temperature loads, it can be seen that not much work is done on solder joint in FC assembly at high-temperature excursions.

The increase in application of electronic device with FC as a constituent to sectors where operating ambient conditions of temperature is above 150°C raised the frequency of fatigue failure of its solder joints. The reliability of a system is measured by the performance of its weakest component. In microelectronic systems, product reliability is a direct function of solder joint reliability since solder joint has been identified as the most susceptible to inevitable cyclic

temperature loading in field usage conditions. These performance threatening conditions also arise during power on/off and in severe cases none operating and then operating in high-temperature shift conditions. It is pertinent to mention that high-temperature reliability of microelectronic chip on board is influenced significantly by the CTEs of bonded materials in its solder joint [25, 47, 80-82]. Owing to the large expansion mismatch between silicon die and PCB in CTE, the solder bumps undergo large visco-plastic deformation under cyclic thermal loading conditions. Thermal strain is induced in the joint and the magnitude influences the solder bump response to the induced stress.

The lead-free solder used in FC manufacture contains Sn3.9Ag0.6Cu alloy materials [59]. Alam et al. [44] reported that Ho et al. [83] reported that above 0.5 wt. % Cu in solder, Cu₆Sn₅-based IMC forms at interconnects of the solder and bond pad. Therefore, the Cu-Sn based IMC was used in this investigation. Fig. 7-1 (a) shows a meshed quarter model of a FC assembly and fig. 7-1 (b) is a schematic of a solder bump with IMC sandwiched between solder region and bond pads.

Since the useful lifetime of electronic devices has been reported to decrease significantly due to large thermal stresses that occur especially at bonded material interfaces of their solder joints [34, 84, 85] which get critical at high-temperature excursions, further study will be helpful to provide more information on solder joint damage. This investigation aims to study regional stress induced in lead-free solder joints in a FC assembly at such severe operating condition. In addition, the hysteresis loop of each region was also studied to provide insights into the stability response of the system to cycle dependent damage indicators. The objectives of the research presented in this study are to obtain accurate damage value of FC solder joint, to predict with high accuracy the fatigue life of the

critical joint and to identify the failure site and mechanism of the lead-free solder joint at elevated temperature operations.

7.3 Methodology

FEM discussed in section 3.4 was employed in the investigation. Anand's viscoplastic model also discussed in section 2.4.1.2 was utilised to capture the solder plastic deformation in the joints of the FC assembly (fig. 3-3) which was loaded and bounded as discussed in section 3.4.3. The bumps were generated as discussed in section 3.2. Serial number 3 bump profile of table 3-1 was used for this investigation.

7.3.1 Finite element modelling

FEM methods have been used widely to study and predict the reliability of FC solder joints in field operations. Determining the behaviour of the system via simulation complements experimental investigation especially in solder joint reliability analysis where plastic work, strain energy and strain energy density magnitudes need to be generated from numerical modelling and fed into fatigue life model. This section is presented in three sub-divisions. These parts are: model and methodology, materials and properties; and loads and boundary conditions.

7.3.1.1 Model and method

A three-dimensional representative solid model of the FC assembly after reflow is built into finite element analysis code, ANSYS v13. The bump profile is generated using a methodology encompassing the use of truncated sphere theory, the forced-balanced analytical method and ANSYS software design modeller (DM) systematically [1]. A quarter of the realistic model with mesh is presented in fig. 7-1 and table 3-2 contains the details of its architecture. The advantage of symmetry of the structure was harnessed and only a quarter of the device was modelled. The model has adequate mesh consisting of a total of 10,359,387 nodes and 8,386,466 elements.

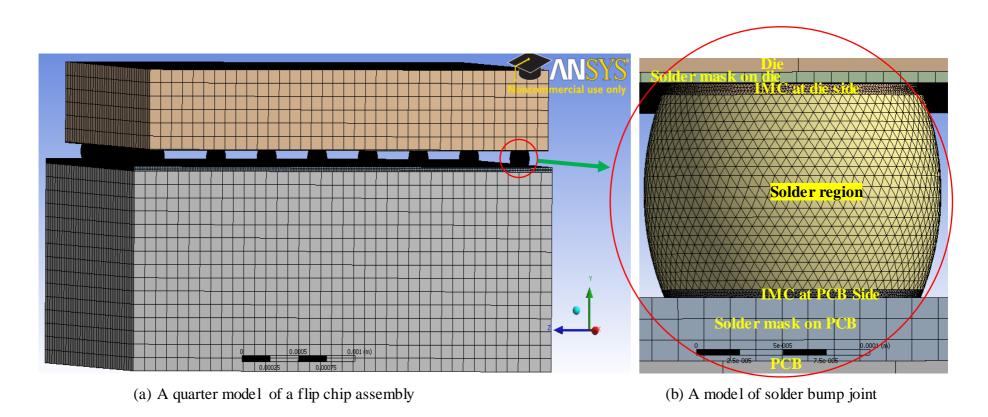


Figure 7-1 A flip chip architecture with mesh

7.3.1.2 Materials and properties

The materials and their properties used in the investigations are tabulated in table 3-3 for the silicon die, copper bond pad, solder mask, SnAgCu solder, IMC and PCB. All the materials are modelled as linear elastic and isotropic except solder and PCB which are modelled as temperature dependent visco-plastic and orthotropic materials, respectively. Thermo-mechanical response of the solder to thermal fatigue loading is modelled with Anand's visco-plasticity not just because many previous studies [12, 31, 73, 86-88] have employed the same model in investigations of similar nature. The reason for adoption of the Anand's model has been discussed and presented in table 2-4) describes the deformation of the solder using no explicit yield condition and no loading/unloading criterion [70]. The flow equation of plastic strain rate has also been given in equations 2-4 to 2-6.

7.3.1.3 Loads and boundary conditions

Guided by other previous works in reliability modelling of solder joints [69, 59, 31 24, 29] and in a desire to explore the system behaviour over relatively long duration of temperature loading, six complete thermal cycles between -38°C and 157°C in 25 load steps were used in the simulation. The loading started from 22°C (room temperature), ramped up at 15°C/min to 157°C where it dwelled for 10 minutes and ramped down to lower dwell region at the same rate where it also rested for 10 minutes. The temperature cycle history is shown in fig. 3-6. The FC architecture (fig. 7-1(a)) was simply supported and its conditions at the supports are:

at symmetric surfaces (-x,z), $u_{(-x)} = u_{(z)} = 0$ (7-1)

at PCB base,
$$y = 0$$
 and $u_{(y)} = 0$ (7-2)

such that the assembly observed plane volumetric deformation. Assumptions which aided simplification of this structure for FEA include:

- The assembly was at stress free state at room temperature of 22°C which was also the starting temperature of the thermal loading.
- The assembly is at homogeneous temperature at load steps.
- Initial stresses (may be from reflow soldering process) in the package were neglected.
- All contacting surfaces were assumed to be bonded with perfect adhesion.

7.4 Results and discussion

The research results and their discussion are presented in four sections. These are study on equivalent stress, study on hysteresis, assembly solder joint fatigue life prediction and effect of thermal cycle number on accumulated damage and predicted life of solder joint.

7.4.1 Study on equivalent stress

The solder joints of fig. 7-1 deform plastically under the applied temperature cycle load (fig 3-6). The visco-plastic deformation of solder under this condition induces thermal stresses which is critical at the assembled materials interfaces due to the materials mismatch in CTE. The response of structural elements to the induced stress over time was observed. The results indicate a maximum stress of 4.67 GPa on die copper pad and a minimum of 6.20 kPa on die. The stress magnitudes and amplitudes of critical solder joint at read out data points at the end of each load step are plotted in fig. 7-2.

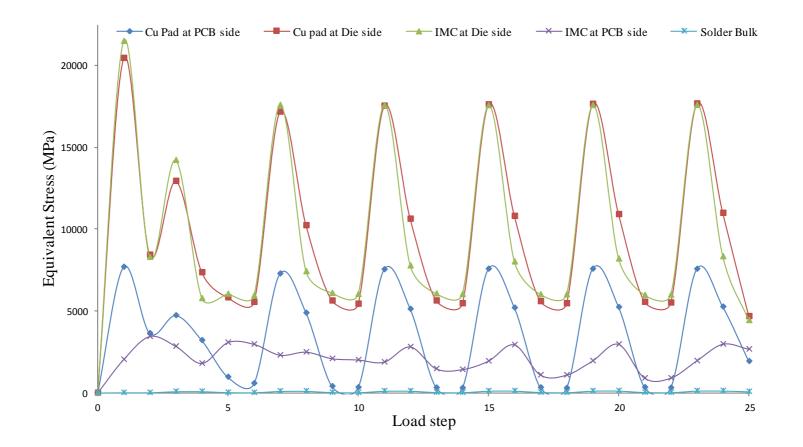
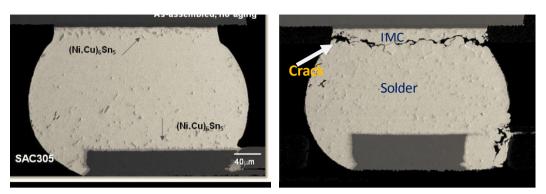


Figure 7-2 Plot of equivalent stress of joint member as a function of temperature load step

It is observed in fig. 7-2 that the stress magnitude and amplitude of IMC at die side and die Cu Pad are approximately equal and are highest. Solder region records lowest stress amplitude and magnitude. The highest stress level attained by solder is 133MPa on load step 24. The difference in stress amplitude and magnitude between IMC at die side and solder impacts the integrity of the interconnection at boundary between them. Thus, this boundary is usually the favoured site of failure by crack initiation and propagation mechanism.

George et al. [69] reported that, in BGA packages, the failure site was at the package-solder interface because it is the narrowest section in a solder joint with PCB that has non-solder mask defined pads and hence has the maximum stress. While this report gave a reason for the crack site, the FEA in this study is able to advance this finding to identify the specific location to be at the interface between IMC at the die side and solder region. It also augments the reason given by ref. [69]. The boundary between IMC at the die side and solder region accumulates large damage from both the mismatch due to thermal expansion of IMC and plastic deformation of solder and also fatigue stress set up by the differences in amplitude of bonded IMC and solder. The CTE mismatch between IMC at die side and solder introduces damage by shear stress and strain along the interface connectivity. In addition, the difference in cycling energy amplitudes between the two bonded materials is believed to cause delamination between them which usually manifests in the form of crack along the interface boundary. It can therefore be inferred that the bond at interfaces of IMC at die side and solder is the most susceptible to failure by fatigue crack. At the PCB side of the interconnection, greater stability is achieved. The ref. [69] reported that since the solder paste extends along the periphery of the nonsolder mask defined pads at the board side, it provides additional adhesion of solder along the circumference, known as the anchorage effect [89, 90]. In investigation involving SMD pads, it is common to observe solder spreading on solder mask on PCB although without the two bonding together. Structurally, the phenomenon strengthens the assembly.

In our investigation involving SMD pads, the same scenario of greater stability was observed. The lower difference in magnitude of stress level and amplitude between the IMC at the PCB side and solder region accounts for the greater stability of interconnect between them. The failure site in the critical joints investigated in this research is similar to those reported in the literature for similar investigations which employed ATC. Many researches including Xie et al. [27], Lee and Lau [72], Zhang et al. [73] and Meilunas et al. [91] in a related research involving thermal cycling at lower temperature reported similar observation. At high-temperature thermal cycling loading, the observation report of George et al. [69] was not different. Fig. 7-3 shows three scanning electron microscope (SCM) images of a good joint with $(Ni, Cu)_6 Sn_5$ IMC, the same joint cracked along the interface between the IMC and the solder bumps after being subjected to ATC and another solder joint cracked at the same site due to high-temperature excursions.







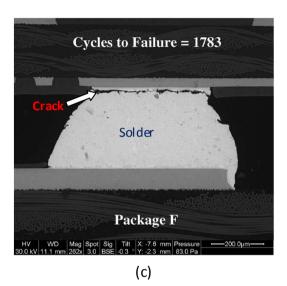


Figure 7-3 SEM images of solder bump, showing :(a) SEM image of a good solder joint; (b) solder joint cracked at interface of solder and IMC at die side due to low-temperature cycling (c) solder joint cracked at interface of solder and IMC at die side due to high-temperature cycling

Sources: (a and b) Xie et al. [27]. (c) George et al. [69]

The schematic representations of distribution of stress at the bump and regions of the bump are shown in fig. 7-4 (a - f). It is observed that, when only solder region is considered, the maximum stress concentrates at the interface between IMC at PCB side and solder bulk as shown in fig. 7-4 (a). In the contrary, when the bump is considered, the maximum stress concentrates at the boundary between IMC at

die side and solder bulk in the bump (fig. 7-4 (b)). It is a general knowledge that a realistic solder bump joint contains IMC. Thus, the interconnection between the IMC at die side and solder region in the bump is the site for crack initiation and propagation. The reason for the susceptibility of this interconnect to failure has earlier been given. Figs. 7-4 (c to f) demonstrate that stress concentrates at the periphery of these models. In addition, a study of figs. 7-4 (e) which is the stress distribution on IMC at the die side and fig. 7-4 (f) which is the stress distribution on IMC at the PCB side show that there is a difference in stress magnitude across the longitudinal axis of the bump.

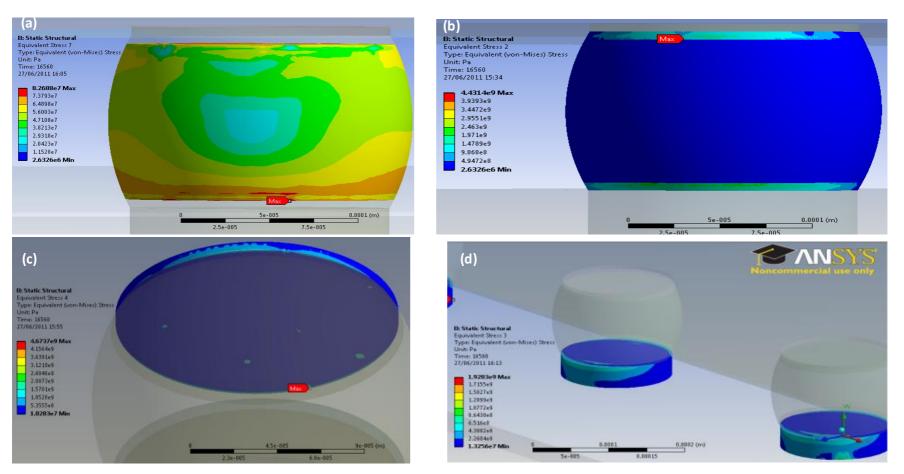


Figure 7-4 Stress distribution at solder bump. Showing: (a) Location of maximum stress on solder region; (b) Location of maximum stress on solder bump; (c) Stress on Cu pad on die; (d) Stress on Cu pad on PCB

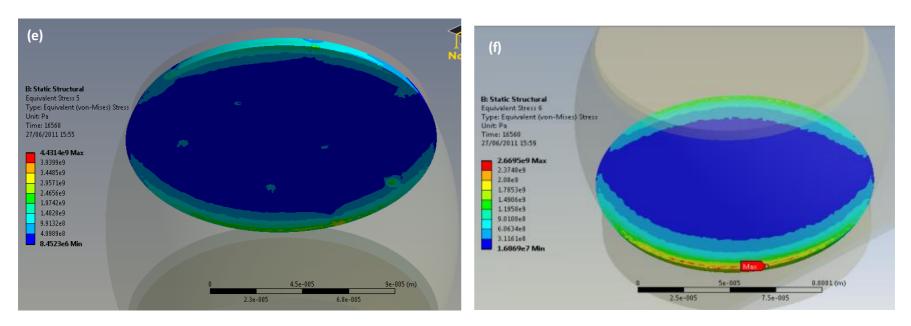
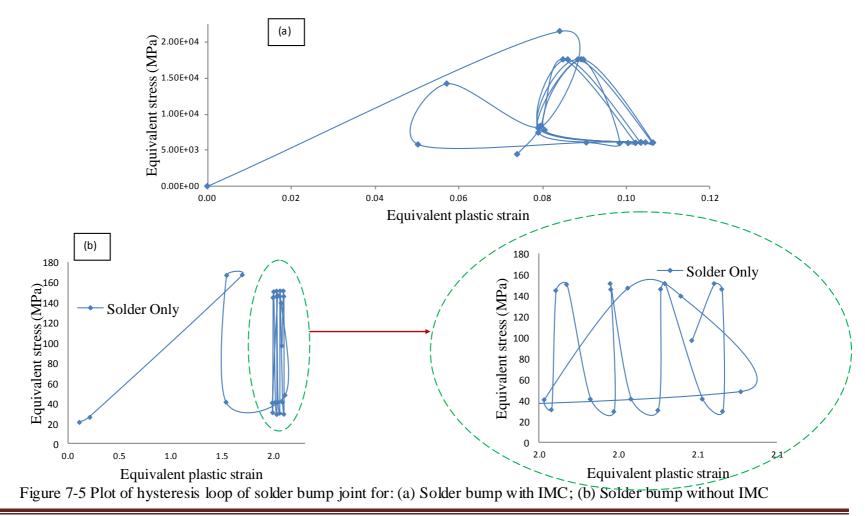


Figure 7-4 Stress distribution at solder bump. Showing: (e) Stress on IMC at die side; (f) Stress on IMC at PCB side

7.4.2 Study on hysteresis loop of the solder joint

The plot of stress magnitude as a function of strain magnitude is known as hysteresis loop. It is used to study the stabilisation and determine the magnitude of induced accumulated plastic work per cycle in solder joints subjected to multiple temperature cycle loads. The stabilisation of solder joint is captured at stabilisation of the hysteresis loop. The area enclosed by a loop represents the magnitude of induced accumulated plastic work per cycle. Fig. 7-5 shows two hysteresis loop plots for two models of solder bump joint. The plot in fig. 7-5 (a) is for a realistic model and fig. 7-5(b) is the unrealistic bump of the same. These plots show that solder bumps with IMC has greater loop area than the other. This means that damage accumulated in solder bump with IMC is more than that in solder joint without IMC – implying that more damage value is recorded when IMC is part of the joint as against when the joint is assumed to consist of only solder. The area enclosed by loop of fig. 7-5 (a) is approximately 148MPa.

Although it can be seen in fig. 7-5 that both bumps stabilise at cycle three, however the nature of their loop is different. Unlike solder with IMC bump which has closed loops, solder only bump exhibits more entropy and has closed loop in cycle three which became open for the rest of the cycle. It is the view of the author that IMC in solder joints aids joints stabilisation by decreasing the volume of solder in the joints. This could be disadvantageous as more volume of solder may be desirable to cushion the effects of assembled materials CTEs mismatch on static structural integrity of the joints. In addition, it can be seen that the presence of IMC in the joints increases the joints damage due to thermal cycle loading. Nonetheless, it is pertinent to note that perfect stability was not achieved and the system merely reached fairly steady state damage at cycle three. Detailed study of effect of IMC on reliability of solder joint which observes high-temperature excursions is reported in chapter 6.



7.4.3 Assembly solder joint fatigue life prediction

Discussions on the methodology to predict fatigue life of solder bump joint has been presented in many sections which include: 2.4.2, 4.3.5, 5.3.3 and 6.3.6. The same approach is adopted in this section. The expression for average value per unit volume per cycle of plastic work density, $\Delta W_{p,avg}$, is given in Eq. 4-18. The plots of read-out data points of plastic work over the six cycles are shown in fig. 7-6(a). It can be seen from the graph that $\Delta W_{p,avg}$ increases as the cycle progresses. However, since the nominal value of $\Delta W_{p,avg}$ does not damage the joint but its change from one cycle to the next $(D\Delta W_{p,avg})$, there is a need to observe the relationship between $D\Delta W_{p,avg}$ and cycle over a long time. The need is imperative because the N_f in Syed's prediction model is a function of $D\Delta W_{p,avg}$. To understand the relationship over a longer time, the output data was used to interpolate a parabolic function:

$$f(W_{p,avg}) = 0.034C^2 + 0.9293C - 0.5549 \tag{7-4}$$

which has the best correlation coefficient of 0.9998. The parameter "*C*" in equation (7-4) is the cycle number. This approach is necessary to reduce both the computation time, amount of disc space and computer memory that otherwise would have been needed for computations involving very many cycles. Such simulation would have inadvertently made the computation cumbersome. The plot of this function up to 30 cycles is shown in fig. 7-6 (b) and the plot of $D\Delta W_{p,avg}$, over cycle is depicted in fig. 7-6 (c) - which shows that the system stabilises and reaches a fairly steady state condition at cycle three. Since the joints fail under the influence of steady state condition, data points of cycle three to six (steady state condition) were used to interpolate a polynomial function:

$$f(D\Delta W_{p,avg}) = abs(-0.0098C^2 + 0.1427C + 0.7761)$$
(7-5)

which describes the relationship between steady state $D\Delta W_{p,avg}$ and number of cycles. The plot of this function is shown in fig. 7-6 (d) for 30 cycles. In the plot, absolute value of $D\Delta W_{p,avg}$ increased to 1.295MJ/m³ at cycle seven, then decreased to 0.0504MJ/m³ at cycle 19 and increased rapidly in the rest of the cycle. Fig. 7-6 (e) is the plot of nominal ($\Delta W_{p,avg}$), accumulated visco-plastic damage ($D\Delta W_{p,avg}$) of the critical solder bump and their functions on the same graph. The plot while showing that nominal damage value increases as cycle progresses, also shows that the accumulated damage continues to build up until solder joint fails. In addition, the plot shows how accurate the functions of $\Delta W_{p,avg}$ and $D\Delta W_{p,avg}$ were in projecting the trends of their representative output data. The character of damage accumulation in the bump is shown in fig. 7-6 (f).

Three stages of damage can be observed. The trend of this plot is comparable to that of generally known creep damage. In the primary stage, the accumulated damage decreases with increase in cycle/time. Primary visco-plasticity is a period of mainly transient vicso-plastic deformation in which the resistance to viscoplasticity increases until the secondary stage occurs. This stage is observed to be longer than the secondary stage. The secondary visco-plastic stage has roughly constant damage rate associated with it. Secondary stage is referred to as steady state visco-plasticity. It is viewed as the stage at which the solder bump strain hardens before yielding due to local high stress concentration. It is seen to have the shortest period in the plot. Nucleation of local high stress concentration culminates in crack initiation at onset of the tertiary stage. The tertiary stage is characterised by rapid increase in damage until rupture. Crack initiation and propagation across the interface boundary between IMC at die side and solder and de-bonding of the two materials account for the sharp rise in its damage value in this stage. Unlike the plot of creep damage over time, which usually has a comparatively long secondary stage, the plot of visco-plastic damage over cycle/time observed in this study has a short secondary stage and a long primary stage. This finding demonstrates that creep models will predict solder joint damage differently from visco-plastic ones. Further research is needed to evaluate the difference which may arise from the utilisation of the two models. A sixth order polynomial (Eq. 7-6) describes the accumulated damage profile.

$$D\Delta W_{p,avg} = -1 \times 10^{-6} C^{6} + 0.000 C^{5} - 0.0041 C^{4} + 0.0589 C^{3} - 0.399 C^{2} + 2.468 C - 2.0219$$
(7-6)

The value of $D\Delta W_{p,avg}$ used in this study was computed using:

$$\frac{1}{17} \sum_{C=3}^{C=19} f(D\Delta W_{p,avg}) = \frac{1}{17} \sum_{C=3}^{C=19} abs(-0.0098C^2 + 0.1427C + 0.7761) = 0.931MJ/m^3$$
(7-7)

The summation started from cycle three and ended in cycle 19 because they are the start of stabilisation and end of secondary damage respectively. To compute the damage to life of the FC assembly, the strain based prediction model by Syed (Eq. 2-8) [52] is employed. The sufficiency of this model has been discussed in section 2.3.2. The values of the constants W' and W_{acc} for SnAgCu solder were generated from Syed [52] as 0.0015 and 0.5683 respectively. The author of [52] determined W' using some set of packages. Stoyanov et al. [59] used the value of W' as 0.0014 and ΔW_p or w_{acc} as 1.32. Similarly, these values of W' and ΔW_p were generated by fitting a linear regression model to a set of experimental data. In this work, with $w_{acc} = \Delta W_p = D\Delta W_{p,avg}$, as an estimation, Eq. 2-8 was used where creep damage was substituted for visco-plastic damage. Plastic work density value was generated from our modelling work and the value of W' were determined by interpolating with values generated from Syed and taken from Stoyanov. Consequently, the value of W' used in this study was determined by interpolating between values of parameters (W', $D\Delta W_{p,avg}$) of Stoyanov (0.0014, 1.32) and Syed (0.0015, 0.5683) at value of (W', 0.931) from this work. The computation produced W' = 0.00145 as the result. Substituting values of W' (0.00145) and $D\Delta W_{p,avg}$ (0.931) in Eq. 2-8 yields FC joint predicted life of 740.8 cycles at approximately 568 hours.

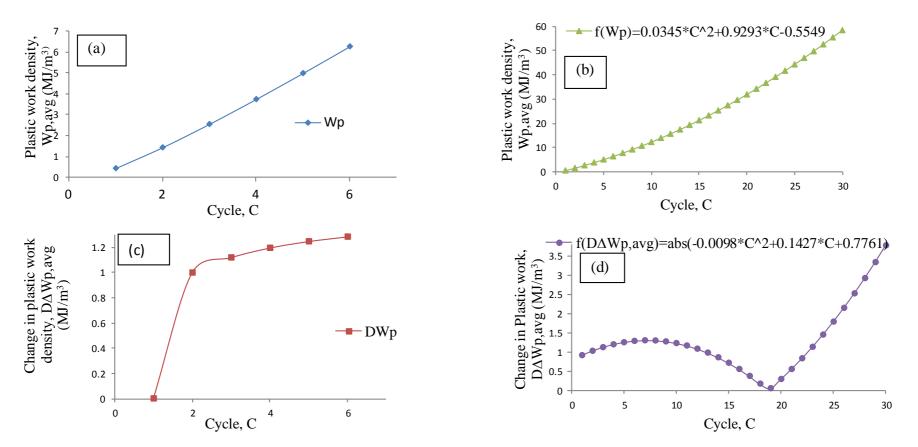


Figure 7-6 Visco-plastic damage in critical solder bump joint showing: Plastic work density per cycle; (b) Plot of function describing plastic work density per cycle; Change in plastic work density from cycle to cycle; (d) Plot of function describing the change in plastic work density from cycle to cycle.

Chapter 7: Damage and Fatigue Life Prediction

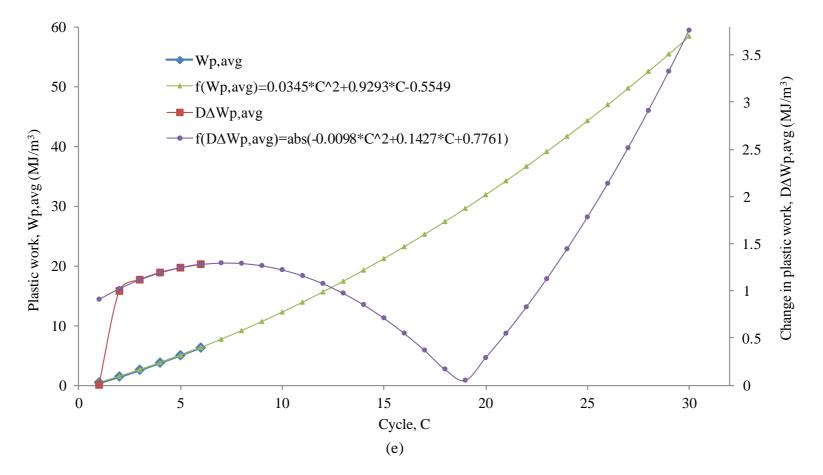


Figure 7-6 Visco-plastic damage in critical solder bump joint showing: (e) Plot of figs (a to d).

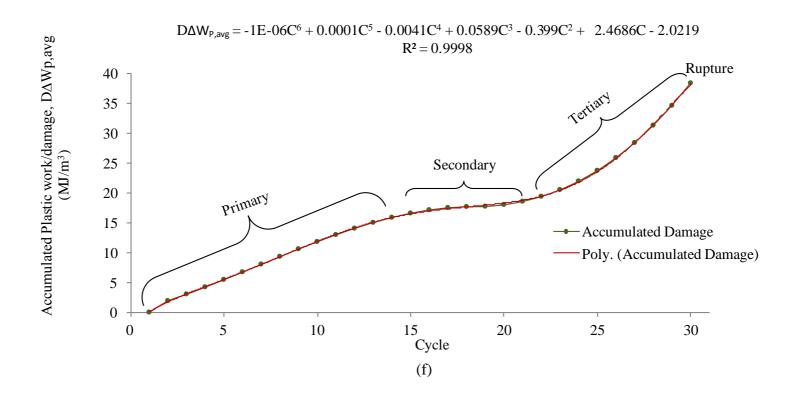


Figure 7-6 Visco-plastic damage in critical solder bump joint showing: (f) Plot of accumulated plastic work damage over thermal cycles.

7.4.4 Effect of thermal cycle number on magnitude of accumulated damage and predicted life of FC solder joints

To determine the consequence the number of thermal cycle employed in ATC has on the magnitude of damage accumulated in the solder joint and also its predicted life, fig. 7-7 was plotted. The figure shows two plots on the same axis. It depicts average accumulated damage in the critical joint at cycle number plotted as a function of the cycle number. This plot has its vertical axis as the primary axis. The average damage at cycle number is computed using:

$$D\Delta W_{p,avg} @ cycle number = AD\Delta W_{p,avg} = \frac{1}{c} \sum_{C=1}^{C=C} f(D\Delta W_{p,avg})$$
(7-9)

where the parameters retain their meanings earlier defined. It can be seen in the plot that the highest change in average damage occurred from cycle one to two. The trend behaviour of the plot becomes sinusoidal after cycle two. A maximum value is recorded at cycle 10 within the region of primary and secondary visco-plastic damage. The plot of accumulated plastic work damage over thermal cycles is repeated on the same axis to aid explanation.

At the primary ordinate axis, the magnitude of accumulated damage (0.931MJ/m^3) is indicated and projected with dots which run parallel to the abscissa. This projection intercepts the sinusoidal plots of the AD Δ Wp,avg in two points shown as *A* and *B*. Point *A* is approximately at cycle 19. With reference to the plot of D Δ Wp,avg, which marks off cycle 19 as onset of tertiary damage, it can be argued that 19 ATCs are sufficient to determine accurate damage in solder joint in FC48D6.3C457 assembly. This result demonstrates that different cycle number of the same ATC will accumulate different damage magnitude in the same solder joint. Similarly, since the life prediction model depends on the value of solder joint damage, the effect of number of ATC used will be parallel.

The magnitude of the solder damage in the joint using the proposed average of cycle 3 to 19 is compared with averages of the other cycle numbers and the outcome is shown as a column in fig. 7-8. The values at cycle 19 compares well. In like manner, the predicted solder joint life using the proposed average of cycle 3 to 19 is compared with averages of the other cycle numbers and the results is depicted in fig. 7-9. Again, the values of life at cycle 19 are the closest.

Chapter 7: Damage and Fatigue Life Prediction

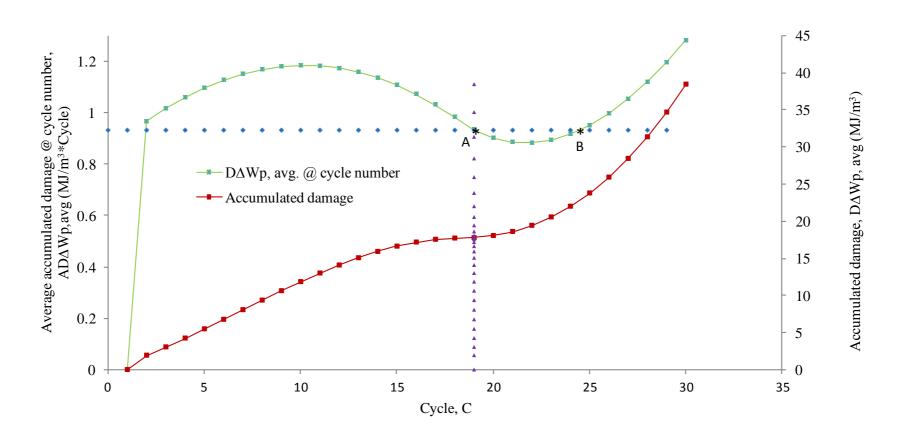


Figure 7-7 Plot of accumulated damage and average accumulated damage of solder joint @ cycle number as functions of temperature cycle number

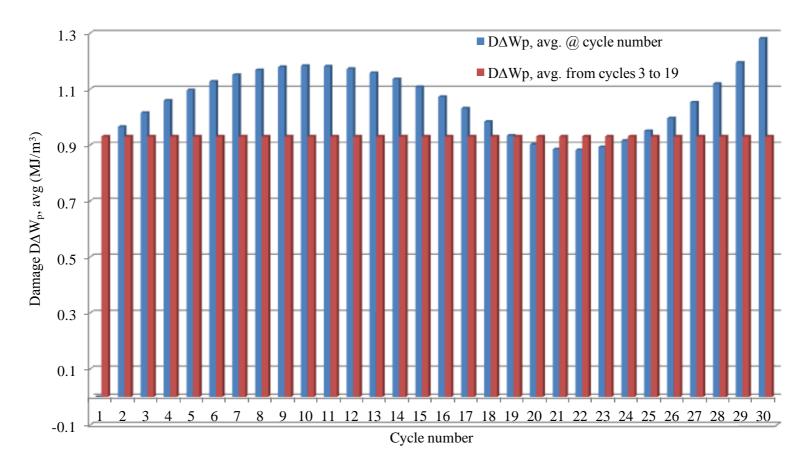
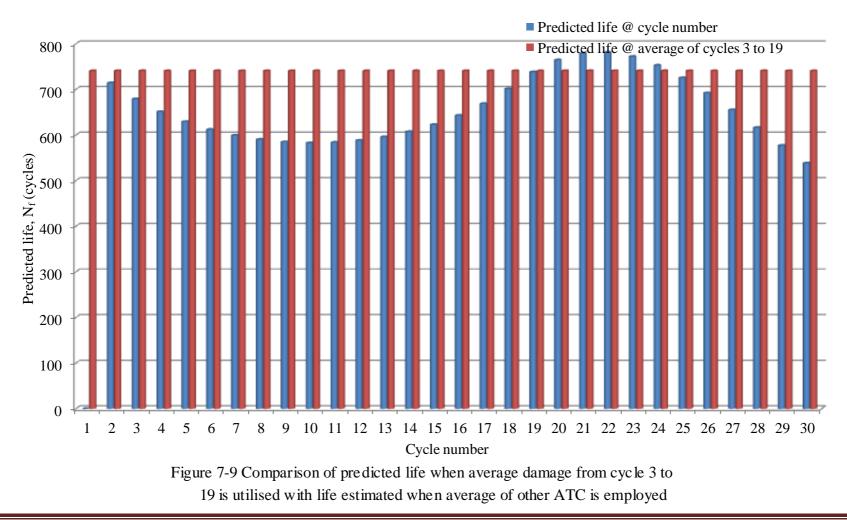


Figure 7-8 Comparison of average damage from cycle 3 to 19 with average of other ATC



Chapter 7: Damage and Fatigue Life Prediction

To validate the magnitude of predicted solder joint damage and its fatigue life used in this investigation, results of its experimental investigation need be generated and compared with the simulation output. This is not currently available as this research is still on-going. Owing to the need to disseminate the preliminary findings, an alternative approach to model validation was sought. The results of this study were compared with related investigations documented in literature [4, 10, 22]. Table 7-1 presents this comparison. It can be seen in this table that the predicted values compared well with other predicted values in literature which have been validated with experiments. The slight deviations observed arise from the discrepancy in the control parameters among the studies. It is a general knowledge that the magnitude of accumulated damage and subsequently the predicted life of solder joint depend on many factors. These constraints include but not limited to component type, array type, the number of I/O, solder alloy type, substrate type, the model used to capture the plastic deformation in the solder, component technology (solder bumping, wire bonding, wafer level), ATC number, ATC range and the life prediction model.

Study	Component	I/O and array	Solder	Substrate	Solder model	Technology	No. of ATC	ATC range	Life prediction model	Predicted life (Cycle)	Experimentally determined life (Cycle)
George et al.[69]	BGA	256 full	SAC305	FR4	Engelmaier	Solder bumping	N/A	-40 to 185	Engelmaier	619*	405 to 551**
George et al.[69]	BGA	144 full	SAC305	FR4	Engelmaier	Solder bumping	N/A	-40 to 185	Engelmaier	904*	475 to 715**
Stoyanov et al [59]	Flip chip	112 Periphery	Sn3.9Ag0.6Cu	organic	Sinh law	Stud bumping	2	-25 to 125	Syed, 2004	542	N/A
Zhang et al. [73]	WL-CSP	48	SnPb	FR4	Anand	Wafer level	N/A	-40 to 125	Modified Darveaux	745*	856*
Current	Flip chip	48 Periphery	Sn3.9Ag0.6Cu	FR4	Anand	Solder bumping	19	-38 to 157	Syed, 2004	741	N/A
Current	Flip chip	48 Periphery	Sn3.9Ag0.6Cu	FR4	Anand	Solder bumping	5	-38 to 157	Syed, 2004	629	N/A
Current	Flip chip	48 Periphery	Sn3.9Ag0.6Cu	FR4	Anand	Solder bumping	6	-38 to 157	Syed, 2004	612	N/A

Table 7-1 Comparison of literature values of solder joint fatigue life with our current results

Key: * *Cycle to failure of 50% of the package;* ** *Cycle to failure of 1% of the package; N/A not available*

7.5 Conclusions

A numerical study on the reliability of FC lead-free solder joints at hightemperature excursions has been conducted. The investigation used a 3-D model built in FEA to study the stress and hysteresis in the solder bumps and also predict the fatigue life of the assembled FC48D6.3C457 on a PCB. The use of 19 thermal cycles is found to give better approximation to the accurate value of accumulated damage in the FC solder joints. The magnitude of accurate damage is the average damage from cycle of hysteresis loop stabilisation to the damage at cycle of onset of tertiary damage.

However, owing to the huge demand on computer disc space, memory, and computational time, it is ideal to use at most six ATC and fit in a curve which is projected for many cycles. The projected function will help to identify the cycle of loop stabilisation and onset of tertiary damage. Based on the results of this research work, the following conclusions and recommendations may be made:

- The difference in stress magnitude and amplitude between flip chip IMC at die side and solder bulk is highest in the assembly and it accounts for the maximum susceptibility of the bond between them to damage by fatigue crack mechanism.
- The use of average of damage from cycle of hysteresis loop stabilisation to the onset of tertiary damage is recommended for modelling study to determine damage and predict fatigue life of solder joints in flip chip assembly.
- The average accumulated visco-plastic damage of solder joint over thermal cycles should be computed from cycle of bump stabilisation to the cycle at the end of secondary damage.

• The author proposes that accumulated damage be a polynomial function of temperature cycle number and not just one average value.

The magnitude of damage and fatigue life predicted for a flip chip solder joints is a function of the number of accelerated temperature cycle used in the modelling.

This model of flip chip can be used in applications which function at 150°C for about 400hours. Thus, it can reliably operate in traditional wire line logging at 150°C and MWD at 150°C for up to 400 hours.

Chapter 8: Conclusions and Recommendations

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 Introduction

This chapter presents, in two sections, the conclusions from the work completed in this thesis and recommendations for further work arising from work which could not be completed within the time duration of this research. The specific recommendations are discussed under four sub-headings.

8.2 Conclusions

The successful application of the Anand's visco-plastic, Syed fatigue life and appropriate material models have been demonstrated in modelling study on reliability of lead-free solder bump joints in a flip chip assembly at hightemperature excursions. The following conclusions can be drawn from this study:

- (i) IMC layer thickness was successfully integrated in the solder bump joints of a geometric model of FC assembly. The incorporation of IMC in the joints, employed to predict its number of cycle to failure, improves the accuracy of the fatigue life model from $\pm 25\%$ which is currently generally accepted to $\pm 23.5\%$ and also increases the accuracy of the predicted fatigue life of the critical bump by 1.5%.
- (ii) In the study on damage mode of realistic and unrealistic solder joints which were subjected to accelerated thermal cycle, the results demonstrate that the failure mechanism of solder bump which consists of IMC is different from the one which does not contain IMC. A combination of fatigue damage, which occurs at the early period of device operations and visco-plastic damage which is accumulated over prolonged operations and which is caused by plane plastic shear strain

Chapter 8: Conclusions and Recommendations

at the boundary between IMC at the die side and solder bulk, majorly drive failure in bumps with IMC. Plastic deformation driven by shear damage in bulk solder is a key failure mechanism in bumps without IMC.

- (iii) Maximum damage is found at the interconnect boundary between the IMC at die side and solder region in a FC assembly. It is shown in this study that this interface connectivity frequently fails by mechanism of fatigue crack initiation and propagation because the difference in stress magnitude and amplitude between the two bounded constituents is highest in the joint assembly. The accumulated damage was also found to increase as the component stand-off height decreases. Specifically, the integrity of the solder joints becomes considerably critical when the diameter of SMD bond pad on its PCB exceeds 110% of the size of diameter of SMD bond pad at its die side at hightemperature operations.
- (iv) The thickness of IMC has been shown to have strong effect on the loop size and thus the accumulated damage in the solder joints such that very thin and thick IMC negatively impact the joint reliability by decreasing the area of the hysteresis loop of the joint. Since viscoplastic/creep based models do not take into account the presence of IMC, they are arguably inadequate to predict accurate solder joint life.
- (v) The magnitude of damage and fatigue life predicted for a FC solder joints is demonstrated in this work to be a function of the number of ATC used in the modelling. This study also shows that average of damage from cycle of hysteresis loop stabilisation to the onset of tertiary damage is sufficient for modelling study to predict damage

Chapter 8: Conclusions and Recommendations

and fatigue life of solder joints in a flip chip assembly. It further outlines how six ATC is a minimum requirement and the methodology which it employed to demonstrate these.

- (vi) This investigation demonstrates that the solder joints of flip chip model FC48D6.3C457DC can reliably operate in applications which function at 150°C for about 400hours. Thus, it can be used to assemble modules which operate in traditional wire line logging at 150°C and measurement while drilling (MWD) at 150°C for up to 400 hours.
- (vii) A combination of analytical method and construction geometry has been employed to develop a model and method to predict the solder bump architecture. The utilisation of this model and method demonstrate capacity for ease of incorporation of IMC in the geometric model of solder joint as evident in the model of the bumps created.

8.3 Recommendations for further work

With reference to the findings of this research work, there are a number of recommendations for further research work. These suggestions are presented in two sub-headings:

8.3.1 General recommendations

Computer and numerical modelling approaches have been employed in this research study although experimental studies from literature have been used,

where appropriate, to validate the research findings. It would be highly beneficial to also re-validate the results by carrying out designed experiment utilising the already set down modelling parameters and materials in this desertion. By so doing, it is believed that the results of this work can be improved.

8.3.2 Specific recommendations

The specific recommendations are presented in four sub-headings as follows:

(i) Utilisation of the derived solder bump model

The use of the derived bump model involves the determination of values of some of its parameters. The determination of this value is somewhat by trial and error method. An excel spreadsheet was used but it is recommended that a computer algorithm be developed to solve the model represented in equation 3-10.

(ii) Improvement of the discrepancy between predicted and experimentally determined solder joint fatigue life

The 1.5% improvement demonstrated in this study, which leads to change from the generally accepted $\pm 25\%$ to $\pm 23.5\%$, in the discrepancy between predicted and experimentally determined solder joint fatigue life, can still be improved upon. The data used in the determination of this improvement figure were extracted from published literature. It is therefore suggested that the modelled study parameters and materials be employed in a designed experiment to validate the result from it. The belief is strong and positive that the 1.5% can be improved upon.

(iii) Fatigue life prediction model

At present, based on the researcher's knowledge, the existing fatigue life prediction models for lead-free alloy solder has been based on creep constitutive relations. This research study has adapted the creep fatigue life model for SnAgCu solder where creep damage in life prediction model has been approximated as visco-plastic damage. However, there is confidence that if a life prediction model based on lead-free solder visco-plasticity is developed, its implementation will definitely improve the result presented in this thesis.

(iv) Accumulated damage in solder joint

Numerically, most determination and measurement of damage in solder joint has been done with models based on creep and visco-plastic deformation of solder in joint. Unfortunately, fatigue load is a contributing factor as has been found in this study. The development of a new model based on both fatigue loading and visco-plastic/creep strain will be good as it is anticipated that when employed, it will produce better results than the ones presented in this study.

Moreover, as the results in this study have shown that determining accumulated damage in solder joint using solder alone is inappropriate, the development of a new model which will take into account the damage in IMC in solder joint will be very helpful.

The area of the loop of hysteresis plot is used to determine the damage of solder joint. One major concern in this concept is that it does not take into

account the position of the loop on the co-ordinate axis. Different loops in different positions with the same area connote equal damage. The concern of the researcher is that this may not be right. It is therefore recommended that solder damage be calibrated as a function of area and relative position of the hysteresis loop in the coordinate axis.

REFERENCES

- [1] Amalu, E.H. and Ekere, N.N., High temperature reliability of lead-free solder joints in a flip chip assembly. Journal of Materials Processing Technology, 2011. 212: p. 471-483.
- [2] Liao, E. B., Tay, A. A. O., Ang, S. S. T., Feng, H. H., Nagarajan, R and Kripesh, V., Fatigue and bridging study of high-aspect-ratio multicopper-column flip-chip interconnects through solder joint shape modeling. IEEE Transactions on Advanced Packaging, 2006. 29 (3): p. 560-569.
- [3] Pinardi, K., Lai, Z., Vogel, D., Kang, Y. L., Liu, J., Liu, S., Haug, R. and Willander, M., Effect of bump hight on the strain variation during the thermal cycling test of ACA flip-chip joints. IEEE Transactions on Advanced Packaging, 2000. 23, (3): p. 447-451.
- [4] Tsai, C.-C., The effects of geometric parameters variation on lead-free flip-chip package under temperature cycling test. MSc Thesis in Mechanical and Electro-Mechanical Engineering, National Sun Yat-Sen University, 2006. Kaohsiung 80424 ,Taiwan. p. 90.
- [5] Amalu, E.H., Ekere, N.N. and Bhatti, R.S., High temperature electronics: R&D challenges and trends in materials, packaging and interconnection technology. In 2nd International Conference on Adaptive Science & Technology, 14-16 December 2009. Accra, Ghana. pp. 146-153.
- [6] Johnson, R. W., Evans, J. L., Jacobsen, P., Thompson, J. R. and Christopher, M., The changing automotive environment: high-temperature electronics. IEEE Transactions on Electronics Packaging Manufacturing, 2004. 27(3): p. 164-176.
- [7] Li, J. Packaging needs for high temperature and harsh environments. Advanced Packaging Online Article [cited 2011 21.03]; Available from: http://www.sengenuity.com/news/adv_pack_jli_032007.
- [8] Normann, R.A., First high-temperature electronics products survey 2005. Sandia National Laboratories, 2005. California. p. 1-43.
- [9] Braun, T., Becker, K. F., Koch, M., Bader, V., Aschenbrenner, R. and Reichl, H., High-temperature reliability of flip chip assemblies. Microelectronics and Reliability, 2006. 46(1): p. 144-154.
- [10] Amalu, E.H., Ekere, N.N., Bhatti, R.S., Mallik, S., Takyi, G. and Ibhadode, A. O. A., Numerical investigation of thermo-mechanical behaviour of ball grid array solder joint at high temperature excursion.

Advanced Materials Research Scientific.net; Trans Tech Publications, Switzerland 2012. 367: p. 287-292.

- [11] Amalu, E.H., Ekere, N.N. and Aminu, G., Modeling high temperature reliability of flip chip Pb-free solder joint at varying bond pad diameter. In AES-ATEMA' 2011International Conference on Advances and Trends in Engineering Materials, 01-05 August 2011. Montreal, Canada. pp 385-393.
- [12] Amalu, E.H., Ekere, N.N., Bhatti, R.S., Mallik, S., Takyi, G. and Ibhadode, A. O. A., Numerical investigation of thermo-mechanical behaviour of ball grid aray solder joint at high temperature application. In 3rd International Conference on Engineering Research & Development: Advances in Engineering Science & Technology 7-9 September 2010. Benin City, Nigeria. pp. 1242-1251.
- [13] Amalu, E.H., Ekere, N.N. and Aminu, G., Effects of intermetallic compound on high temperature reliability of flip chip interconnects for fine pitch applications. In 3rd International Conference on Adaptive Science and Technology (ICAST 2011), 24-26 November 2011. Abuja, Nigeria. pp. 208-214.
- [14] Amalu, E.H., Ekere, N. N. and Mallik, S., Evaluation of rheological properties of lead-free solder pastes and their relationship with transfer efficiency during stencil printing process. Materials & Design, 2011. 32: p. 3189-3197.
- [15] Amalu, E. H., Lau, W. K., Ekere, N. N., Bhatti, R. S., Mallik, S., Otiaba, K. C. and Takyi, G., A study of SnAgCu solder paste transfer efficiency and effects of optimal reflow profile on solder deposits. Microelectronic Engineering, 2011. 88: p. 1610-1617.
- [16] Takyi, G., Amalu, E. H. and Bernasko, P. K., Effect of solder joint integrity on the thermal performance of a tec for a 980 nm pump laser module. Soldering & Surface Mount Technology 2011. 23(2): p. 115-119.
- [17] Otiaba, K. C., Ekere, N. N., Bhatti, R. S., Mallik, S., Alam, M. O., Amalu, E. H., Thermal interface materials for automotive electronic control unit: trends, technology and R&D challenges. Microelectronics Reliability, 2011. 51(12): p. 2031 – 2043.
- [18] Amalu, E.H., Lui, Y. T., Ekere, N. N., Bhatti, R. S. And Takyi, G. Investigation of the effects of reflow profile parameters on lead-free solder bump volumes and joint integrity. In International Conference on Advances in Materials and Processing Technologies (AMPT2010); 24th -

27th, October 2010. Paris, France: American Institute of Physics. pp. 639-644.

- [19] Otiaba, K. C., Ekere, N. N., Bhatti, R. S., Mallik, S., Alam, M. O., Amalu, E. H., Thermal management materials for electronic control unit: trends, processing technology and R&D challenges. Advanced Materials Research, 2012. 367: p. 301-307.
- [20] Amalu, E.H. and N.N. Ekere, Prediction of damage and fatigue life of high-temperature flip chip assembly interconnections at operations. Revised manuscript submitted to Journal of Microelectronics Reliability, January, 2012.
- [21] Ekere, N.N. and G. Nnanna, Developing local capability for automotive manufacture in Nigeria, in Businessday Newspaper. 2009: Nigeria.
- [22] Li, J., Packaging needs for high temperature and harsh environments. Advanced Packaging online Article, 2007.
- [23] Li, J.M., Packaging design & manufacture of high temperature electronics module for 225°c applications utilizing hybrid microelectronics technology. Vectron International, 2004: Hudson.
- [24] Bailey, C. and Stoyanov, S., Reliability of flip-chip interconnect for fine pitch applications. In International Conference on the Business of Electronic Product Reliability and Liability, 27-30 April 2004. Bangkok, Thailand. pp. 187-191.
- [25] Zhang, Z., Park, S., Darbha, K. and Master, R. N., Impact of usage conditions on solder joint fatigue life. In Electronic Components and Technology Conference. 1 4 June, 2010. Las Vegas, Nevada. pp. 14-19.
- [26] Lyon, Flip-Chip Packages accounted for 13% of all integrated circuit (IC) packages by the end of 2010 2011, Yole Développement Report: Lyon, France.
- [27] Xie, W., Lee, T. -K., Liu, K. -C. and Xue, J., Pb-free solder joint reliability of fine pitch chip-scale packages. In Electronic Components and Technology Conference. 1- 4 June, 2010. Las Vegas, Nevada. pp. 1587-1590.
- [28] Hsu, Y. and Chiang, K., Double layers wafer level chip scale package (DL-WLCSP) solder joint shape prediction, reliability and parametric study. In Inter Society Conference on Thermal Phenomena. 2004: Las Vegas. p. 310-316.

- [29] Reichl, H., Schubert, A. and Topper, M., Reliability of flip chip and chip size packages. Microelectronics Reliability, 2000. 40: p. 1243-1254.
- [30] Libres, J. and Arroyo, J. C., Investigation of bump crack and deformation on Pb-free flip chip packages. In Electronic Components and Technology Conference, 1 - 4 June, 2010. Las Vegas, Nevada. pp. 1536-1540.
- [31] Yang, J. and Ume, C. I., Thermomechanical reliability study of flip-chip solder bumps: using laser ultrasound technique and finite element method. In Electronic Components and Technology Conference. 27-30 May, 2008. Lake Buena Vista, Florida, USA. pp. 611-622.
- [32] Ladani, L.J. and Razmi, J., Interaction effect of voids and standoff height on thermomechanical durability of BGA solder joints. IEEE Transactions on Advanced Packaging, 2009. 9(3): p. 348-355.
- [33] Li, X. and Wang, Z., Thermo-fatigue life evaluation of SnAgCu solder joints in flip chip assemblies. Journal of Materials Processing Technology, 2007. 183(1): p. 6-12.
- [34] Mallik, S., Ekere, N., Best, C. and Bhatti, R., Investigation of thermal management materials for automotive electronic control units. Applied Thermal Engineering, 2011. 31(2-3): p. 355-362.
- [35] Ridout, S. and Bailey, C., Review of methods to predict solder joint reliability under thermo-mechanical cycling. Fatigue & Fracture of Engineering Materials and Structures, 2007. 30(5): p. 400-412.
- [36] Lo, C.C., Numerical prediction & experimental validation of flip chip solder joint geometry for MEMS Applications, PhD Thesis in Mechanical Engineering, 2008. Hong Kong University of Science and Technology, Hong Kong. p. 179.
- [37] Shen, J. and Chan, Y. C., Research advances in nano-composite solders. Microelectronics Reliability, 2009. 49(3): p. 223-234.
- [38] Salam, B., A study of intermetallic compound formation and growth in Sn-Ag-Cu lead-free solder joints. PhD Thesis in Engineering Systems, 2005. University of Greenwich, United Kingdom. p. 267.
- [39] Vianco, P.T., Solder materials. In AWS soldering handbook. 1999 American Welding Society: Miami.
- [40] Hwang, J.S., Solder paste in electronic packaging. 1989., New York

- [41] Xu, L., Pang, J. H. L., Prakash, K. H. P. and Low, T. H., Isothermal and thermal cycling aging on IMC growth rate in lead-free and lead-based solder interface. IEEE Transactions on Electronics Packaging Manufacturing, 2005. 28(3): p. 408-414.
- [42] Chi, C. -S., Chang, H. -S., Hsieh, K. -C. and Chung, C., Interfacial microstructure of Pb-free and Pb-Sn solder balls in the ball-grid array package. Journal of Electronic Materials, 2002. 31(11): p. 1203-1207.
- [43] Grilletto, C., Arroyave, C. M., Govind, A. and Salvaleon, E. R., Growth prediction of Tin/Copper intermetallics formed between 63/37 Sn/Pb and OSP Coated Copper Solder Pads for a flip chip application. IEEE Transactions on Electronics Packaging Manufacturing, 2002. 25: p. 78-83.
- [44] Alam, M.O. and Chan, Y. C., Effect of 0.5 wt % Cu in Sn-3.5% Ag solder balls on the solid state interfacial reaction with Au/Ni/ Cu bond pads for ball grid array (BGA) applications. Chemistry of Materials, 2005. 17(9): p. 2223-2226.
- [45] Sakuma, K., Sueoka, K., Kohara,S., Matsumoto, K., Noma,H., Aoki, T., Oyama, Y., Nishiwaki,H., Andry, P. S., Tsang, C. K., Knickerbocker, J. U. and Orii, Y., IMC bonding for 3D interconnection. In Electronic Components and technology Conference (ECTC) 1 - 4 June, 2010. Las Vegas, Nevada. pp. 864-871.
- [46] Wu, J. -S., Yu, S.-P., Peng, I. -H., Wang, J. -l. and Chung, B., Board-level reliability of lead-free SnAgCu solder joint. In 4th International Symposium on Electronic Materials and Packaging 4-6 December, 2002. pp. 282-286.
- [47] Hung, S.C., Zheng, S.H., Ho, S.H., Lee, S.C., Chen, H.N. and Wu, J.D., Board level reliability of PBGA using flex substrate Microelectronics Reliability, 2001. 41: p. 677-687.
- [48] Alam, M. O., Lu, H., Bailey, C. and Chan, Y. C., Fracture mechanics analysis of solder joint intermetallic compounds in shear test. Computational Materials Science, 2009. 45(2): p. 576-583.
- [49] Laurila, T., Vuorinen, V. and Kivilahti, J., Interfacial reactions between lead-free solders and common base materials. Materials Science and Engineering, 2005. 49(1-2): p. 1-60.

- [50] Alam, M.O., Chan, Y. C. and Tu, K. N., Elimination of Au-embrittlement in solder joints on Au/Ni metallization. Journal of Materials Research, 2004. 19(5): p. 1303-1306.
- [51] Schubert, A., Dudek, R., Auerswald, E., Gollbardt, A., Michel, B. and Reichl, H., Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation in Electronic Components and Technology Conference, 27-30 May, 2003. New Orleans, Louisiana, USA. pp. 603 - 610.
- [52] Syed, A., Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints. In Electronic Components and Technology Conference. 1- 4, June, 2004: Las Vegas, Nevada, USA. p. 737-746.
- [53] Wiese, S., Meusel, E. and Wolter, K. -J., Microstructural dependendence of constitutive properties of eutectic SnAg and SnAgCu solders. In Electronic Components and Technology Conference, 27-30 May, 2003 New Orleans, Louisiana, USA. 197 - 206.
- [54] Zhang, Q., Dasgupta, A. and Haswell, P., Viscoplastic constitutive properties and energy-partioning model of lead-free Sn3.9Ag0.6Cu solder alloy. In Electronic Components and Technology Conference, 27-30 May, 2003. New Orleans, Louisiana, USA. pp. 1862-1868.
- [55] Morris, J.W., Song, H. G. and Hua. F., Creep properties of Sn-rich solder joints. In Electronic Components and Technology Conference. 27-30 May 2003. New Orleans. pp. 54–57.
- [56] Help, A.m., Theory Reference and Bibliography, Ansys Inc.
- [57] Anand, L., Constitutive equations for hot-working of metals. International Journal of Plasticity, 1985. 1: p. 213-231.
- [58] Brown, S.B., K Kim, K.H. and Anand, L., An internal variable constitutive model for hot working of metals. International Journal of Plasticity, 1989. 5: p. 95-130.
- [59] Stoyanov, S., Bailey, C. and Desmulliez, M., Optimisation modelling for thermal fatigue reliability of lead-free interconnects in fine-pitch flip-chip packaging. Soldering & Surface Mount Technology, 2009. 21(1): p.11-24.
- [60] Chiang, K. and Yuan, C., An overview of solder bump shape prediction algorithms with validations. IEEE Transactions on Advanced Packaging, 2001. 24(2): p. 158-162.

- [61] Sidharth, R.B. and Natekar, D., Solder joint shape and standoff height prediction and integration with FEA-based methodology for reliability evaluation. In Electronic Components and Technology Conference. 28-31 May, 2002. San Diego, CA. p. 1739-1744.
- [62] Yeung, B.H. and Lee, T. T., Evaluation and optimization of package processing and design through solder joint profile prediction. IEEE transactions on advanced packaging, 2003. 26(1): p. 68-74.
- [63] Heinrich, S.M., Schaefer, M., Schroeder, S.A. and Lee, P.S., Prediction of solder joint geometries in array-type interconnects. ASME Journal of Electronic Packaging, 1996. 118: p. 114-121.
- [64] Zahn, B.A. Impact of ball via configurations on solder joint reliability. In Electronic Components and Technology Conference, 28-31 May 2002. San Diego, CA. pp. 1475-1483.
- [65] Nguyen, T.T., Lee, D., Kwak, J.B. and Park S., Effect of glue on reliability of flip chip BGA packages under thermal cycling. Microelectronics Reliability, 2010. 50(7): p. 1000-1006.
- [66] High Performance FR-4 for Multi-layered PWB High Performance FR-4 for Multi-layered PWB Copper Clad Laminates. 2009 17 December [cited 2011 29th March]; Available from: www.mgc.co.jp/eng/products/lm/btprint/lineup/fr4.html.
- [67] Aoki, Y., Tsujie, I. and Nagai, T., The effect of ramp rate on thermal fatigue testing of solder joints. follow-up to Report No. 25, 2007, Espec Technology Report.
- [68] Aoki, Y., Tsujie, I and Nagai, T., The effect of ramp rate on temperature cycle fatigue in solder joints. 2007, Espec Technology Report No.25. p. 4-13.
- [69] George, E., Das, D., Osterman, M. and Pecht, M., Thermal cycling reliability of lead-free solders (SAC305 and Sn3.5Ag) for hightemperature applications. IEEE Transactions on Device and Materials Reliability, 2011. 11(2): p. 328-338.
- [70] Muralidharan, G., Kurumaddali, K., Kercher, A. K. and Leslie, S. G., Reliability of Sn-3.5Ag solder joints in high temperature packaging applications. In Electronic Components and Technology Conference, 1- 4 June 2010. Las Vegas, Nevada. pp. 1823-1829.

- [71] Darveaux, R., Effect of simulation methodology on solder joint crack growth correlation. In Electronic Component and Technology Conference, 21-24 May, 2000. Caesars Place, Las Vegas, Nevada. pp. 1048-1058.
- [72] Lee, S.W.R., and Lau. D., Computational model validation with experimental data from temperature cycling tests of PBGA assemblies for the analysis of board level solder joint reliability. In 5th International Conference on Thermal and Mechanical Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE2004. 2004. France. pp. 115-120
- [73] Zhang, L., Sitaraman, R., Patwardhan, V., Nguyen, L. and Kelkar, N., Solder joint reliability model with modified Darveaux's equations for the micro SMD wafer level-chip scale package family. In Electronic Components and Technology Conference. 27-30 May, 2003. New Orleans, LA., pp. 572–577.
- [74] Rodgers, B., Punch, J., Ryan, C., Waldron, F. and Floyd, L., Experimental and numerical evaluation of SnAgCu and SnPb solders using a microBGA under accelerated temperature cycling conditions. In International Mechanical Engineering Congress and Exposition (IMECE2004), 13-19 November 2004. Anaheim, California, USA. pp. 153-159
- [75] Lau, D. and Lee, S.W.R., Computational analyses on the effects of irregular conditions during accelerated thermal tests on board level solder joint reliability. In Electronics Packaging Technology Conference, 8-10 December2004: Singapore. pp. 516-521.
- [76] siliconfareast.com. Temperature Cycle Test (TCT). [cited 2011 9th December]; Available from: http://www.siliconfareast.com/TCT.htm.
- [77] Mustafa, M., Cai, Z., Suhling, J.C. and Lall, P., The effects of aging on the cyclic stress-strain behavior and hysteresis loop evolution of lead free solders. In Electronic Components and Technology Conference (ECTC), 31 May -3 June 2011. Lake Buena Vista, FL, USA. pp. 927-939.
- [78] Ma, H., Ahmad, M. and Liu, K.-C., Acceleration factor study of lead-free solder joints under wide range thermal cycling conditions. In Electronic Components and Technology Conference, 1-6 June, 2010: Las Vegas, Nevada, United States. p.1816-1822.
- [79] Parmentier, B., Vermesan, O. and Beneteau, L., Design of high temperature electronics for well logging applications. In International Conference on HITEN, 8-11th July, 2003. Oxford, U.K.

- [80] Shaw, M.C., High performance pack of power electronics. In MRS Bulletin, 2003. p. 41-50.
- [81] Liu, X., Haque, S. and Lu, G. -Q., Three-dimensional flip-chip on flex packaging for power electronics applications. IEEE Transactions on Advanced Packaging, 2001. 24: p. 1-9.
- [82] Lu, H. and Bailey, C., Modelling the performance of lead-free solder interconnects for copper bumped flip-chip devices. In International Electronic Packaging Technical Conference and Exhibition, 6-11 July, 2003. Hawaii, USA. pp. 1-6.
- [83] Ho, C. E., Tsai, R. Y., Lin, Y. L. and Kao, C. R., Effect of Cu concentration on the reactions between Sn-Ag-Cu solders and Ni. Journal of Electronic Materials, 2002. 31(6): p. 584-590.
- [84] Schelling, P.K., Shi, L. and Goodson, K.E., Managing heat for electronics. Materials Today, 2005. 8(6): p. 30-35.
- [85] Pecht, M. and Gu. J., Health assessment and prognostics of electronic products - an alternative totraditional reliabilityprediction methods. 2009 [cited 2010 21st August]; May 2009:[Available from: www.electronicscooling.com.
- [86] Chen, S., Lin, Y. and Cheng, C., The numerical analysis of strain behavior at the solder joint and interface in a flip chip package. Journal of Materials Processing Technology, 2006. 171(1): p. 125-131.
- [87] Geisler, K.J.L. and Holahan, M.M., Thermomechanical modeling and evaluation of the impacts of BGA warpage. In Electronic Components and Technology Conference, 1-4 June, 2010. Las Vegas, Nevada. pp. 106-113.
- [88] Zhai, C.J., Sidharth, and Blish II, R., Board level solder reliability versus ramp rate and dwell time during temperature cycling. IEEE Transactions on Device and Materials Reliability, 2003. 3: p. 207-212.
- [89] Arulvanan, P., Zhong, Z. and Shi, X., Effects of process conditions on reliability, microstructure evolution and failure modes of SnAgCu solder joints. Microelectronics Reliability, 2006. 46(2-4): p. 432-439.
- [90] Lim, A.C.P., Kheng, L.T., Alamsjah, A. and Happy, H., The effect of ball pad designs and substrate materials on the performance of second-level interconnects. In Electronics Packaging Technology Conference (EPTC 2003), 10-12, December 2003. pp. 563–568.

[91] Meilunas, M., Primavera, A. and Dunford, S., Reliability and failure analysis of lead-free solder joints. In IPC Conference. 2-3 November 2002. New Orleans, LA.

APPENDIX

ANSYS CODE USED TO COMPUTE PLASTIC WORK IN THE SOLDER JOINTS

Commands inserted into this file will be executed immediately 1 after the Ansys /POST1 command. Active UNIT system in Workbench when this object was created: 1 Metric (m, kg, N, s, V, A) !CALC AVG PLASTIC WORK FOR CYCLE 1 set, 4, last, 1 etable, vtable, volu etable,vsetable,nl,plwk smult, pwtable, vtable, vsetable ssum *get,sumplwk,ssum,,item,pwtable *get, sumvolu, ssum, , item, vtable wavg1=sumplwk/sumvolu !CALC AVG PLASTIC WORK FOR CYCLE 2 set, 8, last, 1 etable, vtable, volu etable,vsetable,nl,plwk smult, pwtable, vtable, vsetable ssum *get,sumplwk,ssum,,item,pwtable *get, sumvolu, ssum, , item, vtable wavg2=sumplwk/sumvolu !CALC AVG PLASTIC WORK FOR CYCLE 3 set,12,last,1 etable, vtable, volu etable, vsetable, nl, plwk smult, pwtable, vtable, vsetable ssum *get,sumplwk,ssum,,item,pwtable *get, sumvolu, ssum, , item, vtable wavg3=sumplwk/sumvolu !CALC AVG PLASTIC WORK FOR CYCLE 4 set, 16, last, 1 etable, vtable, volu etable,vsetable,nl,plwk smult, pwtable, vtable, vsetable ssum *get,sumplwk,ssum,,item,pwtable *get,sumvolu,ssum,,item,vtable wavg4=sumplwk/sumvolu !CALC AVG PLASTIC WORK FOR CYCLE 5 set, 20, last, 1 etable, vtable, volu etable,vsetable,nl,plwk smult, pwtable, vtable, vsetable ssum *get,sumplwk,ssum,,item,pwtable *get, sumvolu, ssum, , item, vtable wavg5=sumplwk/sumvolu !CALC AVG PLASTIC WORK FOR CYCLE 6 set, 24, last, 1 etable, vtable, volu etable, vsetable, nl, plwk smult, pwtable, vtable, vsetable

ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg6=sumplwk/sumvolu
!CALC DELTA AVG PLASTIC WORK
dwavg1=wavg2-wavg1
dwavg2=wavg3-wavg2
dwavg3=wavg4-wavg3
dwavg4=wavg5-wavg4
dwavg5=wavg6-wavg5