Electric-thermal Modelling of Power Electronics Components

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Declaration

I certify that the work contained in this thesis, or any part of it, has not been accepted in substance for any previous degree awarded to me, and is not concurrently being submitted for any degree other than that of Doctor of Philosophy (PhD) being studied at the University of Greenwich. I also declare that this work is the result of my own investigations, except where otherwise identified by references and that the contents are not the outcome of any form of research misconduct.

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Dedication

This thesis is dedicated to my father as well as my family members including my mother, my brother Mamun, my sister Ruma. Thanks for their sincere love and great mental support throughout the years. It is also dedicated to my beloved friends, who have supported and encouraged me unconditionally all the times, and my flatmates, for the happiness that they bring into my life.

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Abstract

Electro-thermal modelling of power electronics system is considered to be one of the most important design techniques for the development of compact and high-power density power electronics systems for the future. For handling inevitable heat generation due to non-ideal nature of components both active and passive, electro-thermal modelling should be seriously emphasized in earlier design stages to prevent premature failure of the components and to avoid over-design or under-design issues so that all the components can operate within permissible thermal limits. Earlier consideration of electro-thermal issues in achieving high power dense and compact power electronics system design will ensure the reliability of the component and help to optimise the design in terms of design constraints and performances such as the thermal limits, reliability, power density, weight and costs etc.

Traditional electro-thermal modelling methods model the power electronic components using the parameters based on steady state temperature and seldom take into account the thermal effect in power loss modelling of the component and thermal coupling between the components. However, these electric-thermal dependencies are important, particularly for applications where components stay proximity to each other in a converter and share the same substrate and cooling system. Integrated electro-thermal modelling is a method which combines the thermal model and temperature-dependent power loss model can be employed at the early design stage to predict the temperature.

The aim of this work is to develop an integrated electro-thermal framework and demonstrate its benefits in carrying out electro-thermal analysis of power dense power electronics systems where component interactions must be taken into account.

The integrated electro-thermal analysis framework that has been developed in this work combines the Finite Element Analysis (FEA) method and circuit-based thermal network method. In this framework, the circuit simulator PLECS is used to predict the power losses in the components and the results are used in FEA thermal analyses to predict the transient thermal responses of power electronics systems. These results are then used to extract compact thermal model parameters using a curve fit approach. The resulting combined electro-thermal compact model is analysed using PLECS again to obtain temperature profile for various loading conditions.

By using the proposed modelling framework, the component thermal interaction has been studied for the three applications which include a boost converter, a three-phase voltage source inverter and an IPT based dual interleaved bidirectional boost converter. The variation of temperature due to thermal coupling has been found significant in all these applications. The result in the first application suggests that if thermal interactions are not taken into account, the estimated junction temperature would result in errors of 17% and 26.7% for IGBT & diode in the first application, i.e. the boost converter, respectively. For the second application, the predicted errors in the temperatures at the junction, at the solder, at the baseplate solder and at the baseplate in the IGBT would be 2.42°C, 2.59°C, 2.56°C and 2.63°C respectively, if the component interactions are not included in the analysis. Furthermore, it has been found that thermal grease layer has great impact on the temperature in power electronics components. If the thermal grease layer is not included in the simulation, temperatures would be underestimated by about 9.8°C, 12.16°C, 12.14°C and 11.8°C respectively at the junction, at the chip solder interface, at the baseplate solder and at the baseplate respectively. In the FET switch application, by taking into account component interaction, the junction temperature is increased by 6°C. It can be concluded that by taking into account the thermal coupling and by extracting RC parameters from FEA thermal analysis results, temperature can be predicted more accurately than using lumped parameter thermal network model alone.

The benefits of proposed electro-thermal model can be exploited by power electronics design engineers. It will help accurately predict temperature at the critical locations of the components under varying electric loading conditions and eliminate the errors in temperature prediction. It will significantly speed up the design process and help analyse real long mission profiles. The integrated framework will also help save time and cost in power electronics system design eliminating the need of test rig for temperature measurement and help to assess the electrical and thermal performance of the converter applications.

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Glossary

IGBT-Insulated-gate Bipolar Transistor

MOSFET- Metal-Oxide Semiconductor Field-effect Transistor

FWD-Freewheeling Diode

FET- Field-effect Transistor

IPT-Interphase transformer

TLPS-Transient Liquid Phase Sintering

HSST-Hybrid Silver Sintering Technology

DC-Direct Current

AC-Alternating Current

DCB-Direct Copper Bonding

CTE-Co-efficient of Thermal Expansion

SMD-Surface Mount Design

MTBF-Mean Time between Failures

AF-Acceleration Factors

IPEM-Integrated Power Electronics Module

MPIPPS-Metal Post Interconnected Parallel Plate Structure

HTC-Heat Transfer Component

MSE-Modified Steinmetz Equation

GSE-Generalized Steinmetz Equation

DF-Dissipation Factor

PWM-Pulse Width Modulation

PCB-Printed Circuit Board

EMC-Electromagnetic Compatibility

EMI-Electromagnetic Interference

ESL-Equivalent Series Inductance

ESR-Equivalent Series Resistance

PDE- Partial Differential Equations

FEA-Finite Element Analysis

FDM-Finite Difference Method

FVM-Finite Volume Method

CFD-Computational Fluid Dynamics

GMRES- Generalised Minimal Residual Method

PSPICE- Personal Computer Simulation Program with Integrated Circuit Emphasis

PLECS- Piecewise Linear Electrical Circuit Simulation

PSO-Particle Swarm Optimization

List of Symbols

$P_{conduction}(t)$	Conduction losses
$V_{CE}(t)$	Instantaneous voltage drop
$i_{CE}(t)$	Instantaneous collector current
E_{on}	Turn-on Energy
E_{off}	Turn-off Energy
E_{sw}	Switching loss
E_{swref}	Reference switching loss
I	Current
I_{ref}	Reference current
V_{CC}	Supply Voltage
V_{CCref}	Reference Supply Voltage
K_i	Exponent of current dependency (IGBT~1; FWD~0.5 ... 0.6)
K_v	Exponent of voltage dependency (IGBT~1.2 ... 1.4; FWD~0.6)
TC_{sw}	Temperature coefficient of switching losses (IGBT~0.003; FWD~0.005 ... 0.006)
T_j	Chip temperature
T_{jref}	Reference chip temperature
P_{cM}	MOSFET Conduction losses
I_d	The RMS drain current in the MOSFET
$r_{DS(on)}$	On-resistance of the device for a given drive voltage and junction temperature
D	Duty ratio
Q_g	Total gate charge
V_{GS}	The peak driver gate voltage for the MOSFET (V)
f_s	Frequency of MOSFET switching (KHz)
P_{swM}	MOSFET Switching Loss
E_{onM}	MOSFET Turn-on Energy
E_{offM}	MOSFET Turn-off Energy
P_{swI}	IGBT Switching Loss
E_{onI}	IGBT Turn-on Energy
E_{offI}	IGBT Turn-off Energy
V_{CE0}	On-state zero-current collector-emitter voltage
I_{cav}	Average IGBT current value
r_C	Collector-emitter on-state resistance
I_{crms}	RMS IGBT current value
P_{cD}	Diode Conduction losses
V_{D0}	On-state Diode voltage
I_{Dav}	Average diode current value
r_D	Diode on-state resistance
I_{Drms}	RMS diode current value
P_{swD}	Diode Switching Loss
E_{onD}	Diode Turn-on Energy
E_{offD}	Diode Turn-off Energy

P_o	Output Power
V_o	Output Voltage
V_{in}	Input voltage
ΔI_o	Output current ripple
L	Inductance
I_{con}	On-time collector current
I_{coff}	Off-time collector current
I_{cav}	Average collector current
I_{crms}	RMS collector current
I_{Dav}	Average diode current
I_{Drms}	RMS diode current
$P_{copper\ loss}$	Copper Loss
I_w	Current through winding
R_w	Winding resistance
P_C	Core loss
P_h	Hysteresis loss
P_e	Eddy current loss
k_h, k_e	Material parameters
B	Magnetic field
f_{eq}	Equivalent frequency
f_r	repetition rate
ESR	Equivalent series resistance
σ	dielectric's bulk conductivity
ε	The lossless permittivity of the dielectric
ω	Angular frequency of the ac current
C	Capacitance
δ	loss angle
DF	Dissipation factor
Q	Quality factor
X_C	Reactance of the capacitor in ohms
I_{Crms}	Capacitor RMS current
Q	Heat flux
k	thermal conductivity of the barrier
A	Area
d	thickness of the barrier
T_f	Temperature of moving fluid
T_∞	Cold Surface Temperature
c_p	the specific heat capacity
dm	the mass of the volume
dV	volume element
ρ	the density of the material
$\frac{\partial T}{\partial t}$	The partial derivative of the temperature with respect to time
Q	heat generation
h	convection coefficient
T_f	Fluid temperature at surface
T_∞	Constant temperature of the free fluid at a distance
Q_{rad}	Radiative heat transfer

ε	Emissivity
σ	Stefan-Boltzmann constant
T	Body Temperature
H_{st}	Storage rate of thermal energy
c_p	Specific heat capacity
R_{th}	Thermal resistance
C_{th}	Thermal capacitance
$T_j(t)$	Time dependent Junction temperature
T_{ref}	Reference temperature
$Z_{th}(t)$	Time dependent transient thermal impedance
$T_{j.Diode}$	Diode Junction temperature
$T_{j.IGBT}$	IGBT Junction temperature
T_s	Sink temperature
T_c	Case temperature
T_a	Ambient temperature
R_{thjc}	Thermal resistance from junction to case
R_{thcs}	Thermal resistance from case to heatsink
R_{thsa}	Thermal resistance from heatsink to ambient
P_{IGBT}	IGBT total power loss.
P_{diode}	Diode total power loss.
$R_{winding}$	Electrical resistance of winding
$R_{T_{ref}}$	Electrical resistance of winding at reference temperature
T_w	Winding Temperature
$ESR_{(T)}$	Equivalent series resistance in the capacitor at operating temperature
$ESR_{T_{ref}}$	Equivalent series resistance in the capacitor at reference temperature
ΔI_{ripple}	Input Current ripple
r	Ripple ratio
I_{in}	Input current
I_{Lmax}	Maximum Inductor current
I_{Lmin}	Minimum Inductor current
B	Magnetic flux density for the core
J	current density
K_u	copper fill factor
B_{max}	maximum flux density
l_w	The length of the wire
ρ	the resistivity of the conductor material
$A_{winding}$	Wire bare area
δ	Skin depth
μ	Permeability
R_{ac}	AC resistance
R_{dc}	DC resistance
Δ	penetration ratio
Δ'	modified penetration ratio:

η_w	The porosity factor
Fr	Resistance Factor
h_c	core window size
d_w	The thickness of the foil
l_g	Air-gap length
W_m	Energy stored in inductor
A_P	Core area product
A_c	Cross-sectional area
t_d	Dielectric layer thickness
t_m	Metallisation thickness
k_d	Dielectric layer thermal conductivity
k_m	Metallisation layer thermal conductivity
r_{in}	Input radius of the roll
r_{out}	Output radius of the capacitor
h_c	Capacitor height
t_c	Thickness of the can
k_{Al}	Aluminium thermal conductivity
R_{axial}	Axial thermal resistance of the capacitor
R_{radial}	Radial thermal resistance of the capacitor
$R_{can-side}$	Can to side thermal resistance
$R_{can-bottom}$	Thermal resistance of the can to bottom
R_{cc}	core-can thermal resistance
R_{thc}	Capacitor Thermal resistance
ρ_{air}	Density of air
c_{air}	Thermal capacitance of air
V	Volume flow through the heatsink $[\frac{m^3}{s}]$
A_{eff}	Effective convective surface area
η	Fin efficiency
t	Fin thickness
L	Heat sink length
c	Fin height
s	Spacing between two consecutive fluid flow channel
λ_{hs}	Thermal conductivity of heatsink material
$R_{th,S-a}$	Sink-ambient thermal resistance
$R_{th,d}$	Baseplate thermal resistance
$R_{th,conv}$	Convection thermal resistance
d_h	Hydraulic diameter of the heat sink channel
n	Number of fluid flow channel
$fRe_{\sqrt{A}}$	Friction factor Reynolds product function
Z_{11} , Z_{22}	Self-heating impedance of IGBT and diode
Z_{12} , Z_{21}	Cross-heating Impedance of IGBT and diode
$Z_{th(m-n)}^{self}$	Self-heating impedance between two consecutive nodes
$Z_{th(m-n)}^{cross}$	Cross-heating impedance between two consecutive nodes
Z_{thI}^{j-cs} , Z_{thD}^{j-cs}	Self-heating impedance of IGBT and diode between junction and chip solder
Z_{thI}^{cs-bs}, Z_{thD}^{cs-bs}	Self-heating impedance of IGBT and diode between chip solder and baseplate solder

$Z_{thI}^{bs-b}, Z_{thD}^{bs-b}$	Self-heating impedance of IGBT and diode between baseplate solder and baseplate
$Z_{thI}^{b-h}, Z_{thD}^{b-h}$	Self-heating impedance of IGBT and diode between baseplate and heatsink
$Z_{thI-D}^{j-cs}, Z_{thD-I}^{j-cs}$	Cross-heating impedance of IGBT-diode and diode-IGBT between junction and chip solder
$Z_{thI-D}^{cs-bs}, Z_{thD-I}^{cs-bs}$	Cross-heating impedance of IGBT-diode and diode-IGBT between chip solder and baseplate solder
$Z_{thI-D}^{bs-b}, Z_{thD-I}^{bs-b}$	Cross-heating impedance of IGBT-diode and diode-IGBT between baseplate solder and baseplate
$Z_{thI-D}^{b-h}, Z_{thD-I}^{b-h}$	Cross-heating impedance of IGBT-diode and diode-IGBT between baseplate and heatsink
$Z_{thI}^{j-cs}, Z_{thD}^{j-cs}$	Self-heating impedance of IGBT and diode between junction and chip solder
$Z_{thI}^{cs-bs}, Z_{thD}^{cs-bs}$	Self-heating impedance of IGBT and diode between chip solder and baseplate solder
$Z_{thI-D}^{bs-b}, Z_{thD-I}^{bs-b}$	Cross-heating impedance of IGBT-diode and diode-IGBT between baseplate solder and baseplate
$Z_{thI-D}^{b-h}, Z_{thD-I}^{b-h}$	Cross-heating impedance of IGBT-diode and diode-IGBT between baseplate and heatsink
I_{trms}	RMS MOSFET current
R_{ds}	MOSFET Drain to source resistance
i_g	MOSFET gate current
V_{gs}	Gate to source voltage for MOSFET
Q_{plt}	MOSFET gate to drain Miller plateau charge
Q_{th-p}	MOSFET threshold to plateau gate charge
V_{plt}	MOSFET plateau voltage
Q_{rr}	MOSFET reverse recovery time
t_{rr}	MOSFET reverse recovery time
Z_{drv}	Gate drive impedance
R_g	MOSFET internal gate resistance
P_{rr}	Loss in MOSFET due to diode reverse recovery
P_c	MOSFET conduction loss
P_{sw}	MOSFET switching loss

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Chapter 1 Introduction

1.1 Motivation

Power electronics has become an essential electric energy conversion technique from renewable energy sources such as solar, wind and tidal power etc. It is regarded as the key technology for the efficient use of energy resources to mitigate the rising energy costs due to dwindling fossil energy reserves. The applications of power electronics are finding increased use in many areas such as electric drives, railways, the automotive industry, hybrid electric vehicles, aerospace and the renewable energy sector. An increasing demand for reduced size in power electronics products has shifted design trends towards high power density, compact design and low cost and weight. The factors that influence power electronics system design for future purposes are shown in Figure 1.1. As the power densities for power electronics systems increase, thermal issues are becoming a prevalent design constraint because they are important for product reliability [1].

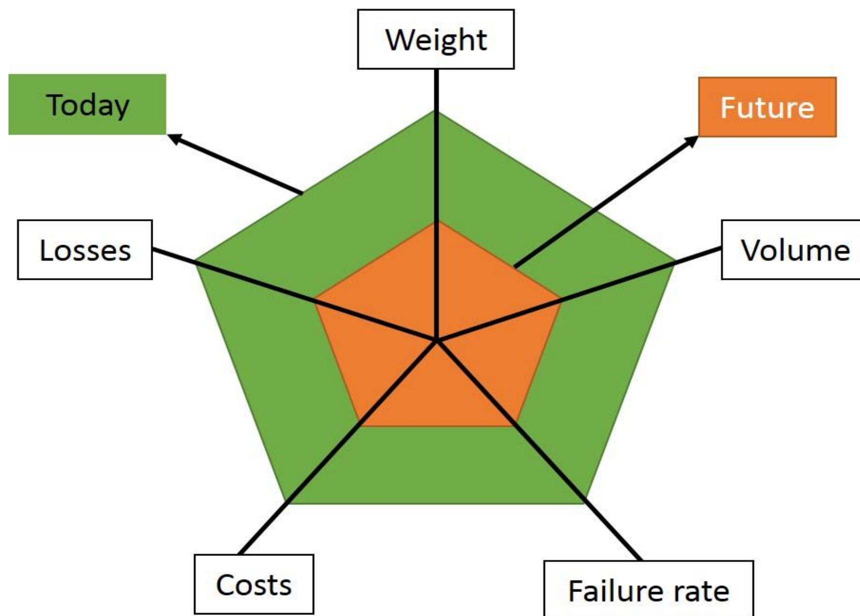


Figure 1.1 Important performance figure of merit of power electronics systems and future design trends.

Power electronics systems are often exposed to stringent operating stressors such as moisture, vibration, dust, chemicals and high voltage and temperature. In particular high temperature causes thermo-mechanical stress which leads to fatigue failure. For example, in the IGBT

(insulated-gate bipolar transistor) power module a failure mechanism happens in the form of bond-wire lift-off and solder interconnect fatigue. Temperature-induced failures are accelerated as the temperature increases and ultimately it limits the reliability of the components. To tackle thermal issues in power electronics systems and to increase reliability, the temperature should be taken into account at the very early stages of the design processes so that the system can operate smoothly in-service without experiencing any failure.

Power electronics systems are often subjected to different harsh operating conditions such as temperature cycling, power cycling and other environmental loading conditions. As shown in Figure 1.2, the percentage of failures due to temperature related issues of electronic components is as high as 55% [2]. Failure distribution among power electronics components is shown in Figure 1.3. It is reported that the capacitor is more vulnerable than the semiconductor [3]. It is also noted that the failure rate accelerates twice for every 10°C rise in operating temperature [4]. It is worth noting that the most affected components in the power electronics systems are capacitors, power semiconductor modules, solder joints, gate drives and connectors. Therefore, the focus of this research is to model the components in terms of electro-thermal interaction.

During the operation of power electronics systems under varying electrical loading conditions temperature induced failure mostly happens in the IGBT power semiconductor module due to thermal stress generation. Thus, it affects the solder joint and wire bond connection interface. The effect of elevated temperature causes serious damage and fatigue to the power semiconductor component. Moreover, due to long-term exposure to the excessive junction temperature than a permissible value leads to the permanent destruction of the components. During high power operation, repetitive tensile and compressive stress generated in the adjacent layers such as the silicon die, solder and substrate etc. also lead to the fatigue of the component. The repetitive thermal stress due to temperature fluctuations is induced by the power cycling [5]. Therefore, accurate electro-thermal modelling of the power electronics system is highly important to be carried out at the very beginning of the design cycle so that it can perform well with high reliability and with a long lifetime [6]. Without prioritising electro-thermal analysis at early design cycles may lead to either over design or under design which results in an increased cost of maintenance and sheer wastage of time. To handle the thermal issues accurately, development of the modelling methodology is required for the analysis of the electro-thermal behaviour of power electronics systems.

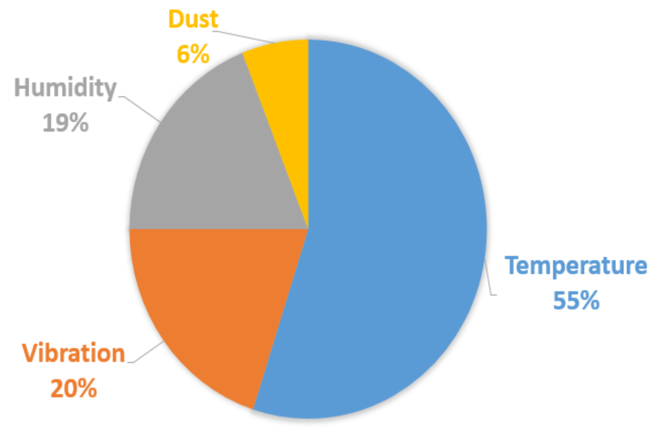


Figure 1.2 Failures of electronic components [2].

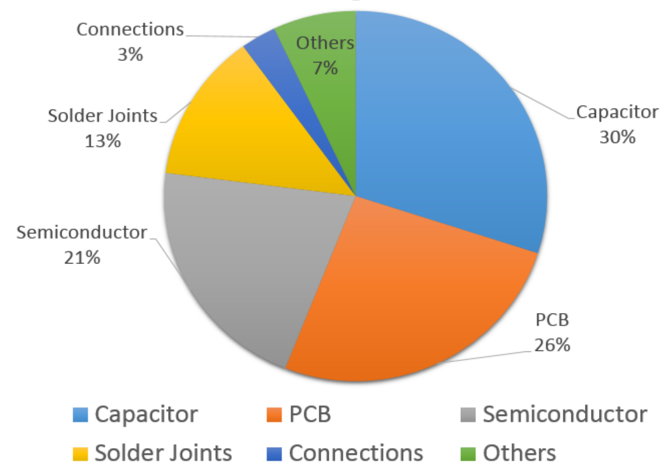


Figure 1.3 Failure root cause distribution for power electronics systems [3].

1.2 Aims & Objectives

There are several design challenges to fulfil the task of achieving a compact and power dense power electronics system. Power electronics systems are often required to operate with high reliability in increasing high-temperature applications. Furthermore, power electronics system design lacks the formulation of an integration approach of multi-domain physics interaction. Three physical domains (electrical, thermal and magnetic) are highly interactive and dominant in designing power dense electronics systems. Mere design of power electronics products in the light of electrical domains is not adequate in operating at high temperatures. Therefore, interactive or concurrent electro-thermal analysis of the power electronics components is highly important at the early system-level design to prevent thermally-induced

failure and increase the reliability performance of the power dense and compact power electronics system.

In this research, a modelling methodology will be developed to address the concurrent electro-thermal behaviour in a power electronics system. Familiar power electronic converter topology will be investigated. The prime target is to develop the electro-thermal model of each component employed in the converter. Furthermore, a temperature dependent loss model interaction will be investigated and the electro-thermal behaviour will be studied at system level integrated power electronics systems design. Throughout the assessment, the modelling approach will be developed to demonstrate the component interactions and non-linear behaviours.

The research challenges and questions in relation to the electro-thermal analysis of integrated power electronics systems design to be addressed are as follows:

1. How to meet the electro-thermal modelling challenge of system-level integrated power electronics design?
2. How should the electro-thermal model be applied to lead to an accurate system-level design?
3. How to take into account the non-linearity of the component in the electro-thermal model?
4. How to obtain the thermal network parameters from the FEA (Finite element analysis) model and export to a circuit simulator?
5. How to create an interactive modelling frame work to run a concurrent electro-thermal simulation?
6. Will the proposed modelling approach be able to solve thermal problems in integrated power electronics systems?

The goal of this research is thus to develop a concurrent electro-thermal modelling framework which will solve thermal problems due to the integration of components in a specified volume of power electronics systems. Using computer simulations, the following works will be carried out.

Plan of work:

- Develop an electro-thermal model of power electronics systems using circuit simulation.

- Develop an electro-thermal model of power electronics systems using FEA analysis.
- Compare FEA results with behavioural model results.
- Develop novel methods for the extraction of parameters for lumped parameter heat transfer analysis.
- Complete the integration of the tools in the electro-thermal analysis of the power electronics systems, demonstrate the novelty and advantage of the method and validate the method and use the integrated approach for the optimisation of power converters.
- Demonstrate the capability of modelling the interactions between components and nonlinear behaviours.
- Set up the link between integrated design framework and Powerlife for power electronics reliability analysis.

By applying the developed electro-thermal modelling framework, the electro-thermal analysis of component-interaction of known converter topologies will be demonstrated and the benefits of the framework will be explored.

1.3 Contributions of this Study

Electro-thermal analysis is governed by power electronics topology, magnetic components, capacitor and cooling systems etc. in an integrated power electronics system. Losses generated from these components contribute to thermal energy. As a consequence thermal energy changes the electrical characteristics of the components. It is challenging to fit the electrical model into the temperature-dependent model. In addition, component interaction in a high-power density power electronics system is inevitable. Designing component in an isolated electrical and thermal domain cannot accurately capture the temperature effect on the power loss model of each component. Without considering the electro-thermal interaction of the components at the early system-level design will face an elevated temperature due to non-linear electro-thermal phenomena in high power density applications. Previously research attempts were focused on individual component design both in the electrical and thermal domains. The major challenge in this regard is the integration of this model into the system-level electro-thermal modelling framework. On top of that, extracting an electrical equivalent RC thermal network parameter for each component in the integrated system is challenging. The conventional approach of extracting RC thermal network parameters is based on using the data either derived from the manufacturer or from the experimental test. The manufacturer-provided parameters are simplistic and useful in predicting average junction

temperature. The demerit of using the manufacturer-provided RC parameters is that it cannot describe the thermal coupling between components sufficiently. On the other hand, RC parameters extracted from the experimental testbed-based method deal with the thermal coupling problem in detail. The disadvantage of the latter method is that the requirement of an experimental set up makes the design process lengthy, complicated and more importantly adds cost. In this study, detailed electro-thermal interactions of components in the high-power density power electronics system are demonstrated for three power converter applications. These applications include a DC-DC boost converter topology, three-phase voltage source inverter and an IPT (Interphase transformer) based dual interleaved boost converter. DC-DC boost converter has been chosen for its simplicity which finds wide applications in solar energy systems and fuel-cell based systems. Converters used in these systems often require conversion of source voltage into a much higher DC output voltage. Another reason is that the converter consists of a discrete IGBT and discrete diode and both share the same heatsink. To study the component interaction between two discrete components that are mounted on the same heatsink in a power converter, DC-DC boost topology has been taken as modelling example. The second application considers a half-bridge IGBT power module that is part of a high power (7.8kW), three-phase voltage source inverter. In a multichip power module, both IGBT and diode are mounted onto the same substrate and share the same cooling system. To study thermal influence between the chips, the selected half-bridge power module has been modelled considering the non-linear issues that have been neglected in previous research studies. The non-linear issues include temperature dependent material properties, thermal grease layer, convection boundary conditions and variation of ambient temperatures etc. The third application has been selected to investigate the performance and accuracy of the proposed modelling against the experimentally measured temperature results. The research achievements of this work are listed below:

- An integrated coupled electro-thermal analysis technique has been implemented for the analysis of the component interaction between the IGBT and diode in a DC-DC boost converter and a three-phase voltage source inverter and for thermal coupling analysis between active switches in an IPT-based dual interleaved boost converter.
- By using electro-thermal analysis, RC thermal network parameters have been extracted and further integration with a circuit simulator has been demonstrated
- Electrical and thermal design of both the inductor and capacitor has been achieved.
- A modelling framework has been developed with software interfacing by C# script.

All the objects have been met and are described in the thesis. Novel aspects and contribution to knowledge in this work are outlined below:

1. Novel compact thermal model

A novel RC lumped thermal network has been proposed to be used in circuit simulators for fast and accurate prediction of temperatures in critical locations on the chip surface and solder layers. The effects of geometries, materials, thermal coupling effects, temperature dependent material properties and boundary conditions effects etc. are included in the thermal network. The proposed thermal model is effective, easy to use and integrate into a circuit simulator. It can be used to predict temperature and to analyse the thermal coupling effects in real loading profiles. The thermal model parameters are extracted from FEA simulations. This links the parameters to physical structural dimensions and material properties. This is important because it allows the designers to optimise the packaging design of electronic systems.

2. The impact of components interaction

The effects of component interaction have been analysed and it has been found significant in all three cases. These cases include IGBT-diode interaction in a boost converter, IGBT-diode interaction of the power module in a three-phase voltage source inverter and interaction between switches in an IPT-based dual interleaved bidirectional boost converter. The result in the case 1 suggests that the not taking into account coupling effect results in errors of 17% and 26.7% in the estimation of the junction temperature of the IGBT and diode respectively. The IGBT temperature in case 2 differs by 2.42°C, 2.59°C, 2.56°C and 2.63°C respectively at the junction, at the solder, at the baseplate solder and at the baseplate respectively. When the thermal grease layer is included a high variation is noticed in predicted temperatures. The discrepancy is about 9.8°C, 12.16°C, 12.14°C and 11.8°C respectively at the locations such as at the junction, at the chip solder, at the baseplate solder and at the baseplate respectively. The discrepancy of 6°C is observed compared to a non-coupled model at the FET switch, T2 in case 3. This highlights the need for including the thermal interactions in thermal models and it also provides important information for power electronics product design engineers about the accuracy of traditional thermal modelling methods that are based on the manufacturer-provided datasheet.

3. Modelling of thermal interaction in different layers of the power module

Thermal coupling effects between different points on the chips and different layers beneath the chips have been identified and characterised for the IGBT power module. Based on chip

locations, thermal maps of the coupling between the chips are identified for several chip positions on the substrate. The coupling resistance can be expressed as a function of chip-chip distance. This can help the designer to optimise the temperature reduction.

4. The temperature at critical locations

The temperatures cannot be measured at some critical locations such as the interfaces between the chip and chip solder. In reliability analysis, however, these temperatures are very important for accurate prediction. In the traditional compact thermal modelling method, these temperatures are not normally available because the power module manufacturers do not provide information that is detailed enough. The method that is proposed in this work can address this problem by defining nodes at any location of interest.

5. Development of Software tool interface

The proposed method involves an FEA simulator, circuit simulator and general computing environment MATLAB. To integrate these tools so that designers can efficiently exploit the new methods, a user interface in C# has been written. In this interface, multi-domain modelling can be carried out to predict electric power losses and based on these predicted losses heatsinks can be selected in the thermal analysis and RC parameters can be extracted to build a compact thermal model automatically.

1.4 List of Publications

Different parts of this work have already been published or are being published in international journals or conference proceedings. These publications are listed below:

Three conference papers have been published at International conference.

- M. Shahjalal, H. lu and C. Bailey, "A review of the computer based simulation of electro-thermal design of power electronic devices" *Proceedings of the 20th IEEE International Workshop on Thermal investigations of ICs and Systems (THERMINIC), pp.1-6, 2014.*
- M. Shahjalal, H. lu and C. Bailey, "Electro-thermal Modelling of Multichip Power Modules for High Power Converter Application" *Proceedings of the 18th IEEE International Conference on Electronic Packaging Technology,2017.*
- M. Shahjalal, H. lu and C. Bailey, "An Investigation of Component Interaction and Analysis of its Impact on Electro-thermal Behaviour in a Power Dense Boost Converter Topology" *Proceedings of the 24th IEEE International Workshop on Thermal investigations of ICs and Systems (THERMINIC), 2017.*

One journal paper has been prepared to be submitted to IEEE Transactions on Power Electronics.

- M. Shahjalal, H. lu, C. Bailey, M. Rishad and A. Forsyth "An Analysis of the Thermal Interaction Between Components in Power Converter Applications" in preparation to be submitted to *IEEE Transactions on Power Electronics.*

1.5 The Structure of the Thesis

Chapter 1 presents the introduction and motivation of the thesis, where a detailed background, motivation and objectives of the thesis are also included.

Chapter 2 studies an overview of the integrated power electronics system design and its manufacturing trend for high power density power electronics systems. Power electronics systems and its building block components as well as the application of power electronics and its potential market are discussed. Technical challenges of power electronics packaging technology and overview of power electronics systems packaging are also analysed. Failure modes and mechanisms of power electronics and their reliability issues of integrated power electronics are covered. Finally, the technical barriers to manufacturing high power density converter systems are discussed and the potentiality of a wide band gap semiconductor device in the design of high power density converters are summarised.

Chapter 3 explains the electro-thermal phenomenon and the state–of –the art research methodology employed in power electronics systems design. The generic electro-thermal interactions, component loss models both in active and passive components are first addressed. The concepts of electro-thermal modelling approaches are discussed and the use and applications of these approaches are identified. The limitations of the existing models in the design process of integrated power electronics design preparation are also presented in this chapter.

In Chapter 4, an extensive study is devoted to developing the electro-thermal modelling framework for designing power electronics systems including non-linearity and component

interaction. For this reason, analytical loss characterisation of the topology is compared to the loss profile obtained from the circuit simulation. Later the concept of a component loss model is introduced within a node connected to the thermal network represented either from an initially datasheet-derived lumped or later-refined lumped parameter network through the FEA parameter extraction process. Finally, the application of the framework to analyse a DC-DC boost converter including the non-linearity and cooling system integration is also included in this chapter. The performance of the integrated framework is further investigated using the DC-DC boost converter topology. Both the electrical and thermal effects on the electro-thermal analysis of the converter design applications are studied by using the framework, which is also presented in this chapter.

In Chapter 5, further study focuses on the study of the component interaction between IGBT and diode of a half-bridge IGBT module in a three-phase voltage source inverter. Initially, the basics of the thermal modelling and detailed structure of the IGBT module considered are discussed where the model formulation and operating conditions and challenges are explained. Then, the parameter extraction process is described including self-heating and cross-heating. Then, the assumption of linearity of the thermal model is verified. Then, the robustness of the thermal model is checked again. Furthermore, the impact of boundary conditions on the thermal model parameters is also discussed. Finally, the performance of the developed thermal model is verified by the FEA simulation derived results under real loading conditions in a three-phase voltage source inverter.

In Chapter 6, the evaluation of the modelling performance of the thermal interaction of the IPT-based (interphase transformer) boost converter by using the proposed framework is investigated. Further study is focused to evaluate the performance of integrated electric-thermal analysis. Finally, the significance of the integrated analysis is discussed.

In Chapter 7, the conclusions and contributions of the thesis as well as potential suggestions for future work are provided.

Chapter 2 Overview of Integrated Power Electronics System Design & its Manufacturing

2.1 Introduction

Before going into detail, it is important to know what "electro-thermal modelling" is. Heat generation in compact power electronics systems is inevitable and it is caused by the electric current flow in conductors, the magnetisation of magnetic components as well as the change of direction of electric fields in dielectric materials [7-8]. Arbitrary placement of the components in the integrated system may worsen the thermal issues. These thermal energy need to be minimised and managed. Electro-thermal modelling is a method that can be employed at the initial design stage to tackle this problem.

Components that come in to proximity in a compact power electronics system undergo the issue of shrinkage of the heat transfer path. Heat flow hindered by the limited surface of the components results in increased thermal resistance which ultimately affects the thermal performance of the systems. Thus, reduction of thermal resistance by employing an appropriate cooling mechanism becomes a critical aspect of the design processes. Furthermore, most failures in power electronics components happen directly or indirectly due to the elevated temperatures. Therefore, an accurate electro-thermal design and analysis must be considered carefully for improving component reliability performance.

2.2 Power Electronics Systems and Components

Power electronics is the application of power semiconductor devices for the control and conversion of electric power. All ratings of current, voltage, frequency can be dealt with and the power rating can be converted from milli watts into megawatts. A simplified basic power electronics system is shown in Figure 2.1. It consists of power processor hardware called a converter which acts like as a rectifier (AC to DC), inverter (DC to AC), buck or boost converter (DC to DC) and frequency converter (AC to AC) [9].

Power electronics systems consist of many basic building blocks such as control system, active components, power semiconductor switches, IGBT modules, passive components (such as capacitors, inductors, and transformers etc.), thermal management, packaging, protection devices and enclosures [9]. The use of high switching frequency in making power converters dense, compact and efficient is on the rise. Due to high switching frequency operation converters usually experience the generated electromagnetic interference (EMI).

This EMI also affects other components placed in proximity in the compact converter. For maintaining the stringent EMI standard limit in high switching frequency operation, EMI suppression components such as an input EMI filter and output EMI filter (Figure 2.2) are also considered as essential parts of the power electronics systems [10]. EMI filter is used at both the input and output end to control and minimise EMI emission.

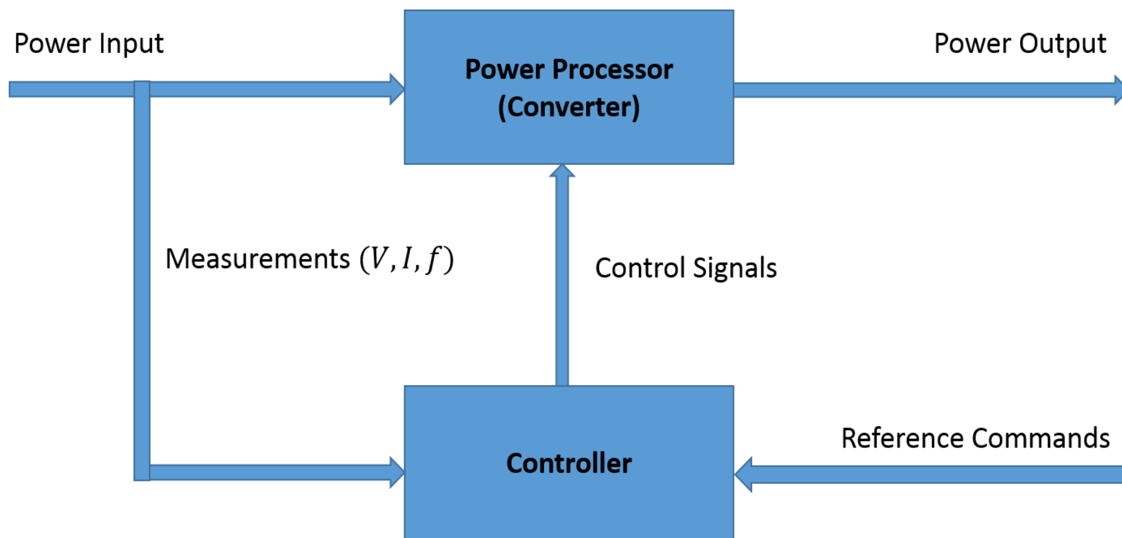


Figure 2.1 Basic building block diagram of a power electronics system [9].

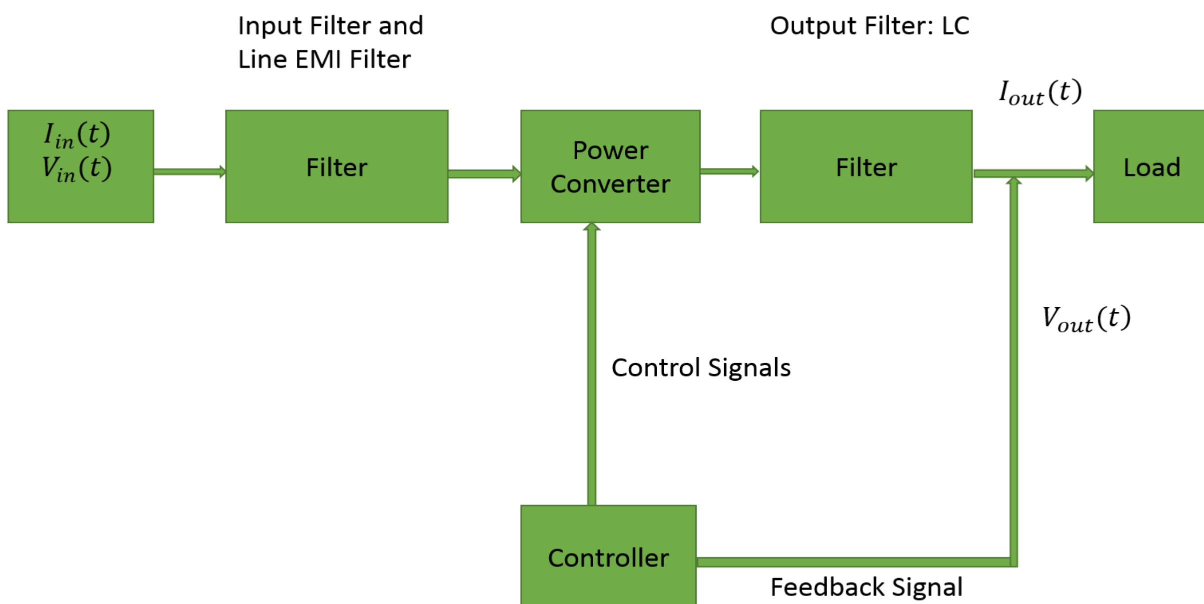


Figure 2.2 Basic block diagram of power electronics system using EMI filter [10].

2.3 Application of Power Electronics System and its Markets

Power electronics plays a vital role in almost every sphere of everyday life and with recent advances in power semiconductor devices, it is influencing many key industrial sectors as well [11]. The significant advent of the manufacturing and packaging of low cost high power semiconductor devices has boosted the use of power electronics products in application areas such as aero-space shuttle power supplies, satellite power systems, aircraft power systems, industrial, residential, telecommunication-battery chargers, power supplies, transportation-battery chargers, traction control of electric vehicles, electric locomotives, electric drives and variable speed drives etc. [12] (see Figure 2.3). Electric power conversion, transmission and distribution in a smart grid can also be enabled by power electronics [13] (see Figure 2.4).

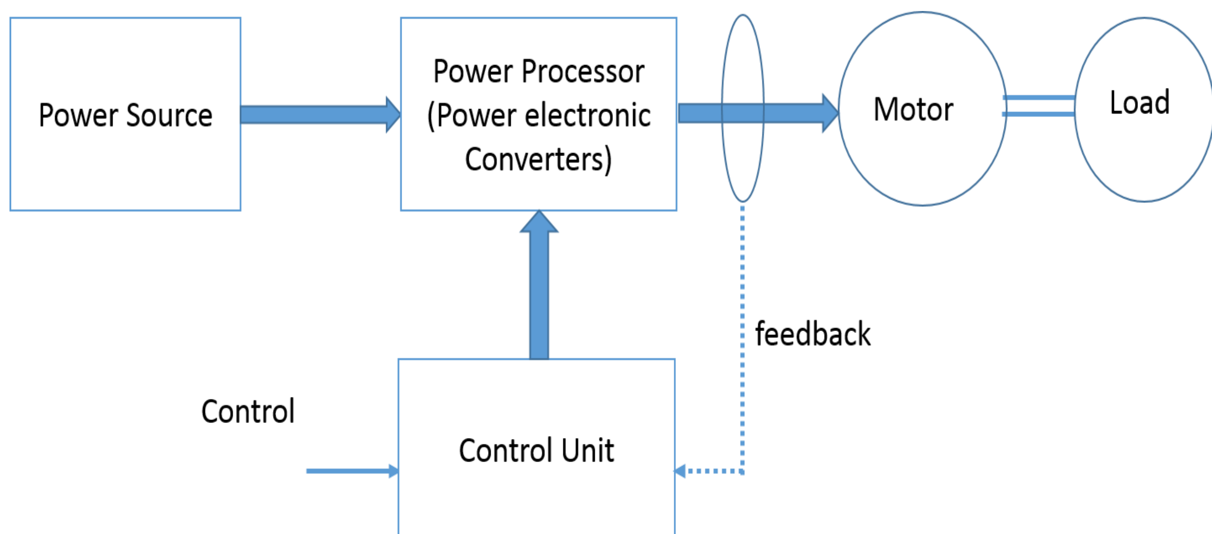


Figure 2.3 Modern electric drive system employing power electronics converters [12].

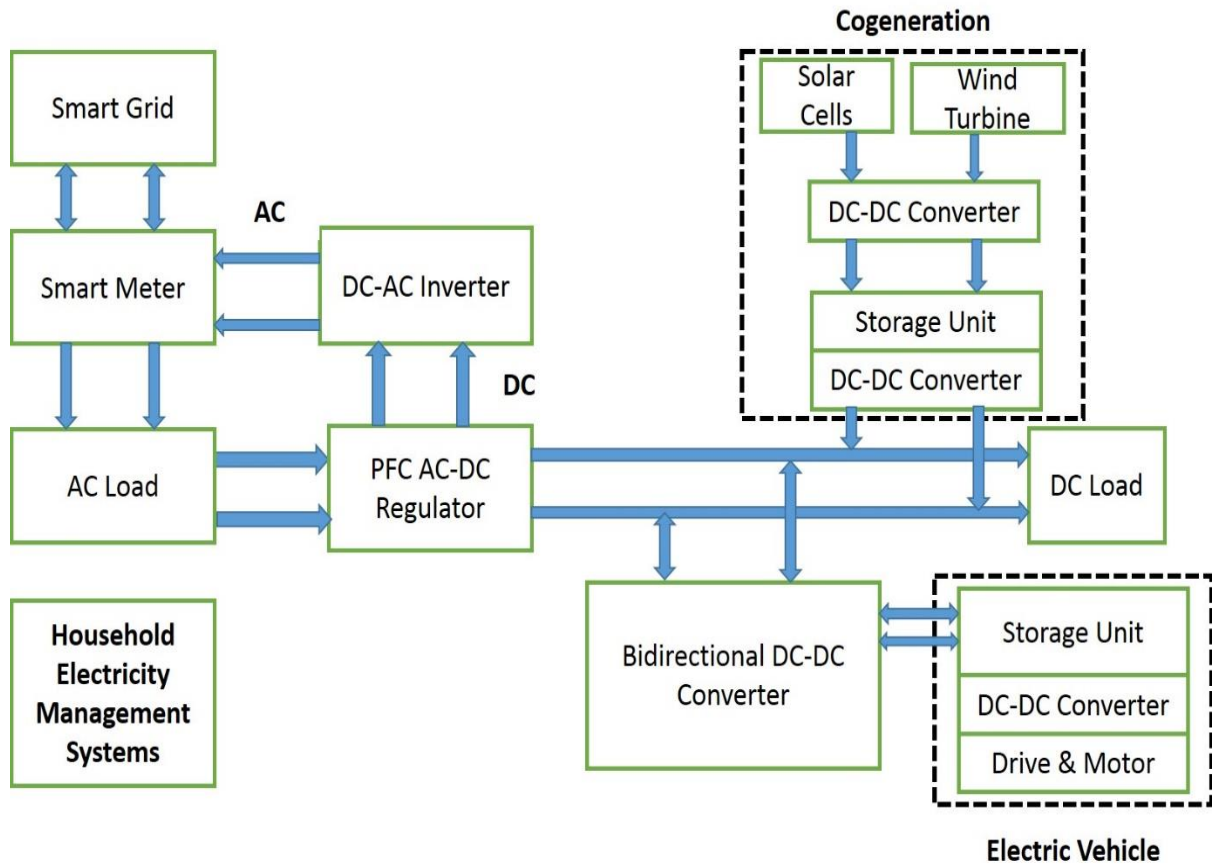


Figure 2.4 Power electronics applications in smart grid [13].

The global market for power electronics products is also expanding. The computer and office, consumer electronics, communications, industry and energy as well as automotive industry sectors account for 26%, 18%, 17%, 26% and 13% of the market respectively (see Figure 2.5). In 2009, the global market value of power electronics is estimated to be £70bn and the market is expanding at a rate of 11% per annum according to [14]. The UK electronics industry contributes about £50bn to the UK GDP and specifically, UK power electronics manufacturing covers 6.5% (estimated £5bn) of the global power electronics product.

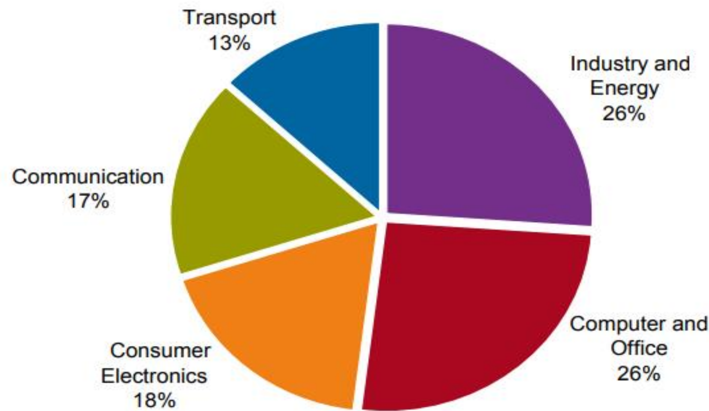


Figure 2.5 Power electronics applications [14].

In 2011, the market value of power electronics around the globe is projected to be £ 135 billion [15]. Due to its significant impact on the economy, it is considered by governments as a key driving technology in their strategy for fast development of sustainable economic growth [16-18].

Two of the most important trends in power electronics systems are (i) high power applications (30-300 MW) [19] and (ii) compact devices (such as SiC, 100 mm wafers with a micropipe density below 10/cm^2) [20] in energy conversion, automotive, railway, transport and aerospace applications [21-23]. Both these trends result in pushing the boundary of power density, operating temperature and introducing severe EMC (Electromagnetic compatibility) issues in power electronics systems.

Since the reliability of the most power electronics components due to electric and thermal loading are a critical feature, a power electronics system is to be designed efficiently in the context of the integrated electric-thermal domain. If reliability is analysed accurately, it can handle in-service mission profiles on a wide scale. It is therefore of high importance to predict the temperature of the components to prevent temperature-induced failures and thereby to enhance the operating performance of the components with long-term reliability.

2.4 Technical Challenges Facing Power Electronics System Design and Packaging

Power electronics systems usually operate under severe electric loading conditions and often function in harsh environments. Manufacturers aim to develop products that have a low

production cost, high reliability, high functionality, great power density and high efficiency etc. These are the performance metrics that generally evaluate the behaviour of power semiconductor devices, passive component integration, packaging and manufacturing [9]. Some of the major challenges encountered by the power electronics system designers in achieving high power density and compact power electronics system are as follows:

- Costs: The cost of manufacturing the power electronics device is one of the key considerations for manufacturers. Improved standardisation and modularity of devices can reduce the costs of device manufacturing and maintenance [9].
- Reliability: As power electronics systems are expected to operate in high-temperature, high-power, high current/voltage and harsh environmental applications, the reliability of components and systems are an extremely important issue in their design [9].
- Component Packaging and Thermal Management: For high-temperature, high-power, and high-speed applications of power electronics systems, component packaging plays an important role in improving the overall system level performance and in the reduction of temperature induced failures [9].
- Cooling Methods: In designing compact, high-power density power electronics systems, a cooling system needs to be integrated at the very beginning of the system level design. Otherwise, it will result in prolonged design processes, high maintenance costs and failure to achieve the required high-power density [9].
- Efficiency: Future power electronics system design aims at achieving high power density but not at the cost of efficiency. The trade-off in efficiency results in increased losses and thus increases the difficulty in thermal management. An important task of designing of power electronics systems is to minimise power losses and cooling requirements [9].
- Control: To realise the full potential of a power electronics system, integration of advanced control system with a gate drive unit and modern control schemes are required at the system level [9]. A larger gate drive unit consumes high power, occupies space and adds parasitic inductance. Therefore, the design of control systems with a low loss and small size gate drive unit is also an important issue to reduce the parasitic inductance which influences the switching behaviour of IGBT or MOSFET (metal oxide semiconductor field-effect transistor).

2.5 Overview of Power Electronics System Packaging

Power electronics packaging is an important issue in the manufacturing of power electronics products. It is essential in reducing the manufacturing costs, further enhancement of the reliability and in achieving high-power density. The thermal performance of power electronics system not only depends on the components but also on its packaging design and materials. Power electronics systems are influenced by various stressors such as temperature, overvoltage, overload and vibration etc. It should be well encapsulated for the protection from external environmental factors such as shock, vibration, humidity and dust etc. In most applications, power electronics systems also are subjected to temperature fluctuations over long periods in realistic applications, i.e. converter applications. Ultimately continuous operation of power electronics systems in harsh thermal environment conditions affects their performance and reliability.

The passive components such as inductors, transformers and capacitors are also considered as essential parts of power electronics packaging. Passive components are integrated in a way so that it can also share the cooling systems. Passive components are sometimes integrated at the bottom of the system so that surface mounted components get enough space on the substrate. Capacitors are also used as surface mounted or are packaged through dielectric layers. The EMI filter is embedded on the passive substrate and is mounted on the heat sink for thermal management. For the reduction of the volume of the power electronic systems, discrete passive components are replaced by integrated passive structures [24-26].

Power modules are the active components of power electronics system packaging. Improper packaging of a power module may lead to failure due to high current/voltage and thus result in disruption of energy conversion processes. Any failure in the wire bond and solder joint will increase current/voltage and ultimately the whole system will fail as quickly as possible [19]. That is why power modules should be packaged in a way so that they meet the criterions such as low cost, low weight, mechanical ruggedness and suitability for high-temperature applications etc. Furthermore, power modules should be packaged in a way so that they contain less parasitic inductance which also influences the power module operation and creates overshoot transient voltages which are also not desired for power electronics system operations [27].

Typically, a power module consists of a multi-layered structure with heterogeneous materials such as silicon chips, aluminium wires and ceramic direct copper bonding (DCB) substrates,

copper baseplates and solders (see Figure 2.6). Power modules are encapsulated with silicon soft gel to provide mechanical support and protect silicon chips, aluminium wires and substrates from external environmental factors such as shock, vibration, dust and humidity etc. [27-28].

The materials which are used in power electronic packaging are as follows:

- Power Semiconductor devices: Most of the devices are Si-based, although other semiconductors have also been used such as SiC, GaN, AlGaN and AsGa diodes etc. [19].
- Substrate: Ceramic substrates such as Al_2O_3, AlN, Si_3N_4, BeO etc. are commonly used with cu metallization both on top and backsides. For low and medium voltage applications, ceramic filled polymer layer is used [19].
- Baseplate: Common baseplates are copper matrix composites, or AlSiC, or carbon-reinforced composites etc. [19].
- Die-attach: Usual solder joint material is the PbSnAg alloy. Due to environmental hazards lead-free alloys or new materials such as sintered silver are used [19].
- Top-side interconnections: The widely used technique is aluminum wire bonding [19].
- Case and Cover: Silicon gel and epoxies are used.

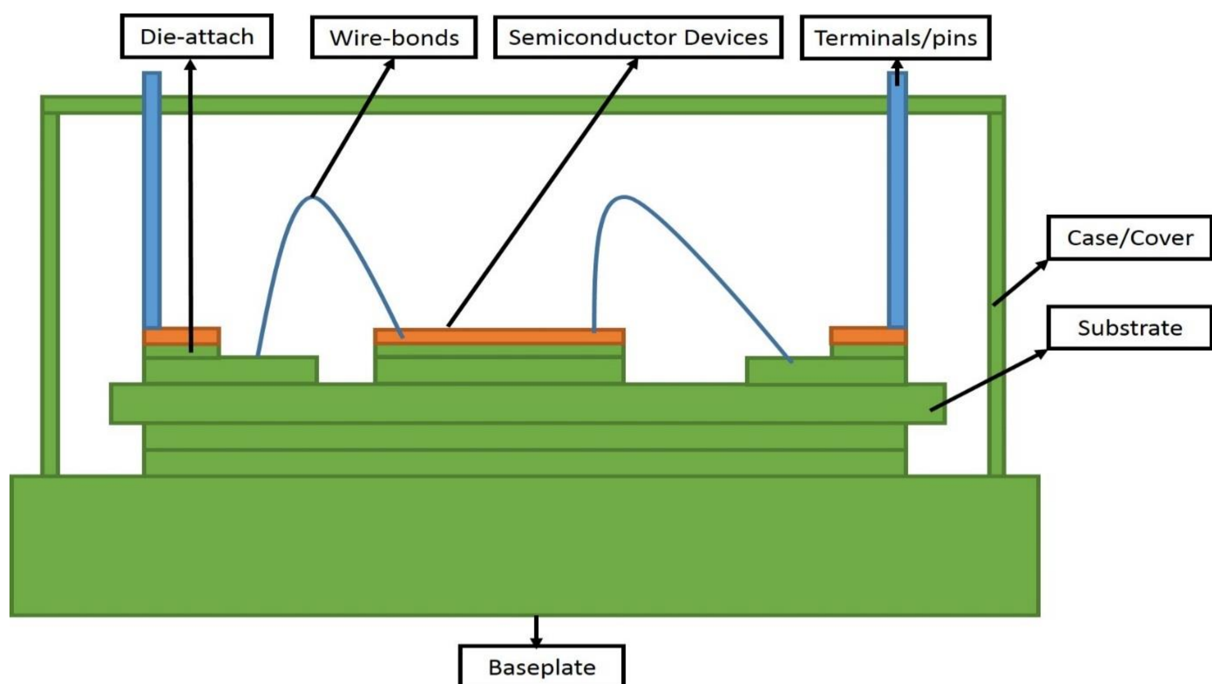


Figure 2.6 Structure of power module [11], [27].

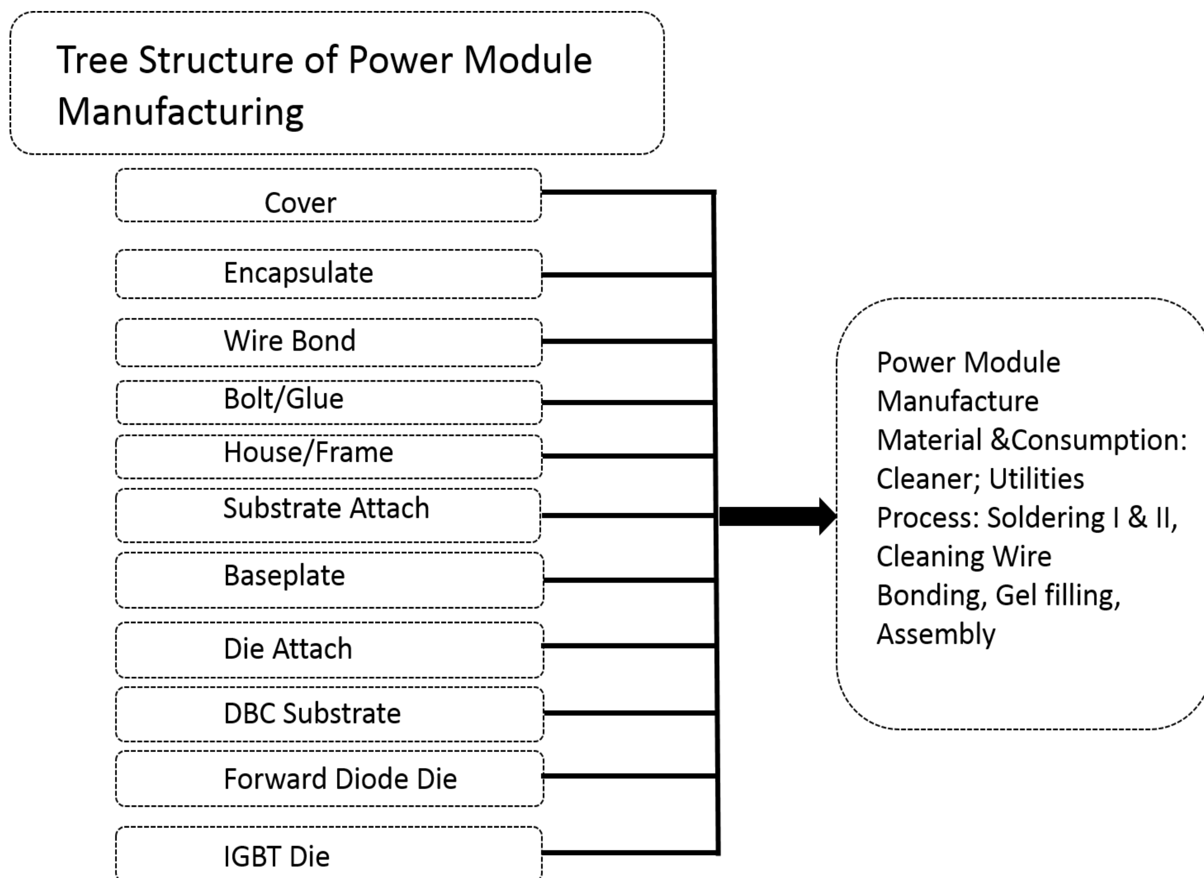


Figure 2.7 Manufacturing process of power module packaging [28].

Various types of technology are used in power module packaging (see Figure 2.7). These are as follows:

Wire bonding technology: Wire bonding is the dominant technology in manufacturing and packaging of multi-chip power modules due to its flexibility and cost-effectiveness. It is used to connect the terminals (or leads) to the semiconductor chips. 300μm aluminium wire bond is connected to the terminals with the ultrasonic welding [29]. Copper wire bonding is also used due to copper's superior properties over aluminium. Usually copper is more electrically conductive than aluminium and copper has a lower thermal expansion with a high thermal conductivity. This copper wire bonding can improve joint strength and reliability [29].

DCB Substrate and Metal base plate: Front and back side of alumina substrate is bonded with 0.25mm thin copper foil by the DCB method. As a metal baseplate 3mm thick copper alloy is used [29].

Soldering Technology: Tin-lead-silver alloy (lead: 93% mass or more) is conventional soldering technology for chip joints. Tin-silver based alloy (tin: 95% mass or more) is newly

developed solder to avoid the hazardous effect of lead [8]. The advantageous property of silver (high melting point of silver -961°C and CTE value of $19*10^{-6}K^{-1}$) can also replace high cost gold and palladium as a desirable candidate material in high temperature packaging applications [30]. Therefore, an Ag sinter layer can ease bonding between chips and substrates. In literature [30] low-temperature sinter technology is employed for die attachment (see Figure 2.8) in Semikron integrated intelligent power modules and thus, the reliability of the package has been improved three times more than standard soldered module. Die attachments materials used in high-performance packaging of a semiconductor device requires highly thermally-conductive material.

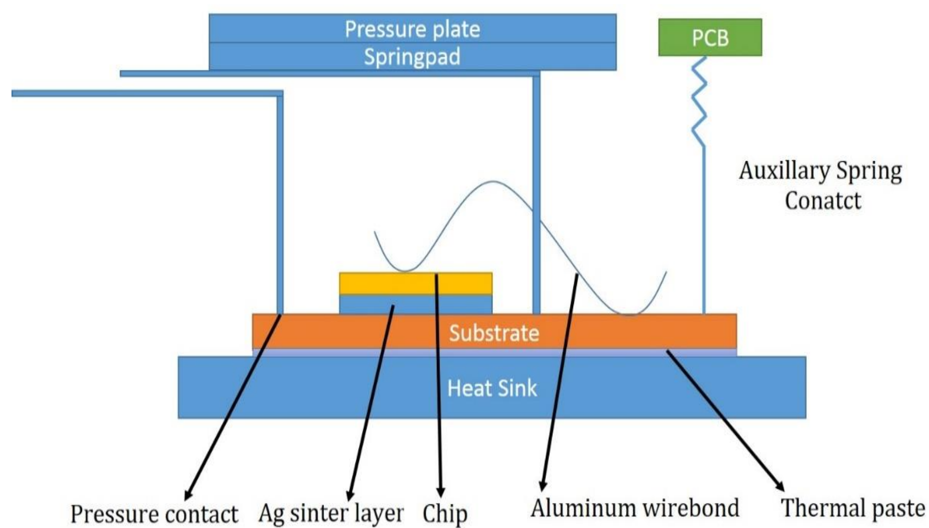


Figure 2.8 Cross-section of Semikron sintered high voltage power modules [30].

Transient liquid phase sintering (TLPS) paste [31] and nano-silver sintering technology [32] are also used in the die attachment of semiconductor packaging. Another material-HSST paste (mixture of silver fakes, thermoset resin and diluents) is also used as die attach materials by hybrid silver sintering technology which solves the problem of backside metallisation due to slow diffusion into bare silicon of the solder transient liquid phase sintering (TLPS) paste and nano-silver sintering materials [33].

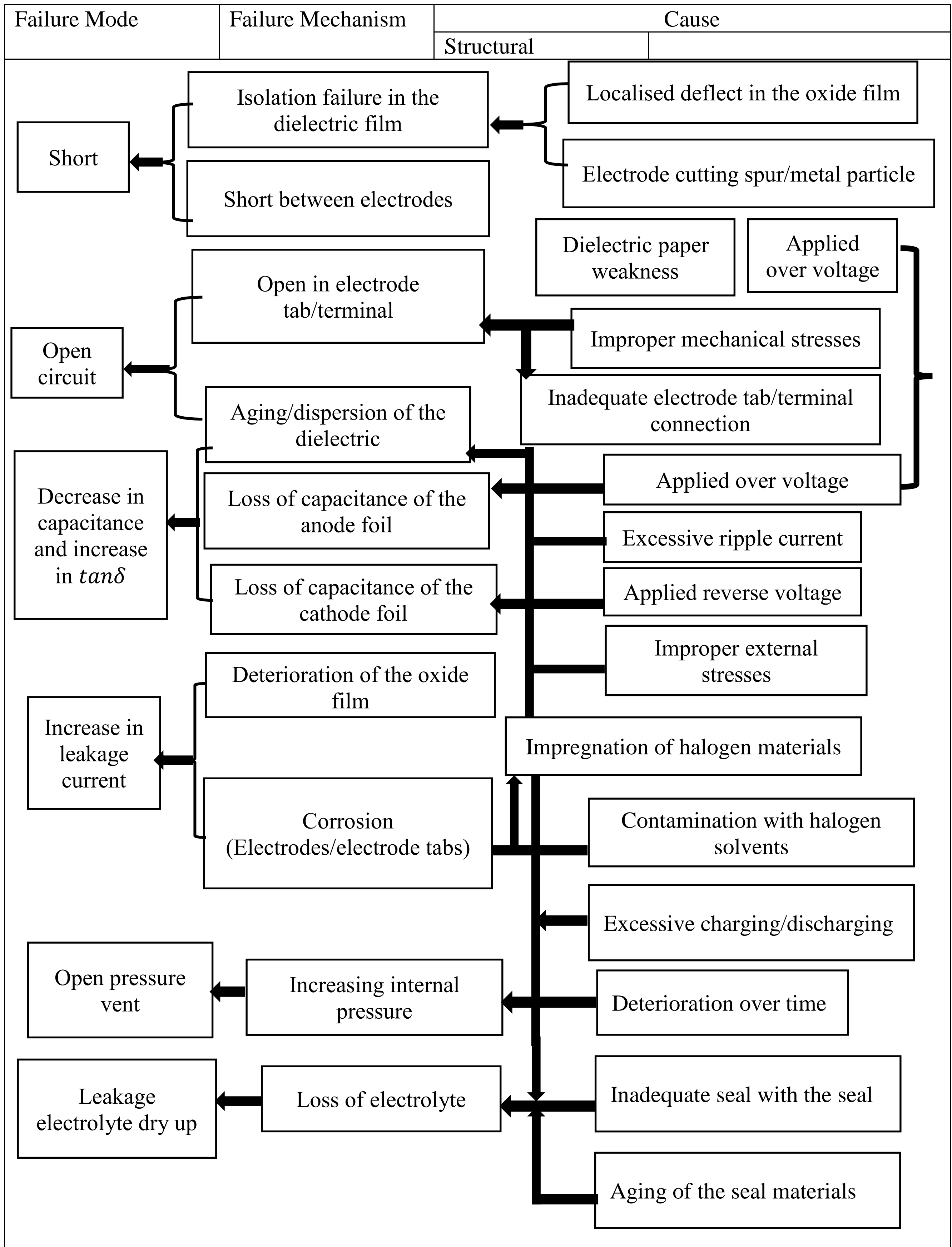
2.6 Failure Modes and Mechanisms of Power Electronics System

Components such as the capacitor, inductor and power semiconductor module which are used in building integrated power electronics systems undergo harsh environmental operating conditions such as dynamic changes of operating temperature (-40°C to +150°C), heavy

mechanical vibration and shocks etc. These components often experience different failure modes due to various failure mechanisms. Now the various failure modes and mechanisms of power electronics system will be discussed.

There are many reasons for the failure of capacitors in a power electronics system. Drying-out of the electrolyte is one of them. Under high temperature and high load conditions aluminium electrolytic capacitors may face deterioration of the Al-oxide layer. The paper spacer in aluminium electrolytic capacitor may move slightly due to vibration. Sealing material in the capacitor faces environmental stresses such as a corrosive atmosphere, high humidity, vibration and shocks etc. ELNA has reported that changes in capacitance ($\pm$ 20% to $\pm$ 30%), changes in the tangent of loss angle (1.5 to 3 times) and changes in leakage current etc. cause failures in aluminium dielectric capacitors [34]. Again, Kemet has reported that dielectric breakdown of the film capacitor may happen due to high-temperature applications [35]. Continuous operation of the capacitor results in increased end termination resistance. High ripple and peak current may result in higher losses which can lead to open capacitors. The dielectric material of a capacitor may undergo expansion or shrinkage due to temperature change. Insulation resistance decreases with the elevated temperature. When the temperature starts to rise, the pressure inside the capacitor also starts to increase and thus causes a breach in the capacitor which results in leakage of impregnation, filling of fluid and moisture susceptibility. The radiation effect also results in electric degradation in the form of dielectric embitterment. Table 1 describes in detail the failure mode and mechanism of the capacitor [34].

Table 1 Failure mode and mechanism of capacitor



Windings of the magnetic components (i.e. inductor and transformer) in a power converter often experience stress generated due to Joule heating in the copper coil. The magnetic permeability of core material is also temperature dependent. Overheating, destruction of wire insulation, cracks in brittle ferrite cores and internal delamination have been reported as failure mechanisms of SMD (surface mount design) inductors [36].

Detailed failure mechanisms in the power module have been reported in many literatures. Power modules are subjected to failures while power electronics systems are operated in high power ratings and undergo abrupt mission profile changes such as load variations and temperature variations. Local power dissipation in chips and the sudden change in external operating temperature lead to thermal fatigue [29]. To observe the package and material degradation, several accelerated tests are performed. Two types of tests such as thermal and power cycling are usually performed to study the wear-out failure mechanisms of power modules.

Solder joint failure is also highly dominant failure mechanism in a power module. The possibility of failure is high enough in the solder joint between DCB and baseplate due to a high CTE mismatch between DCB and baseplate [37-39]. This solder joint degradation causes the temperature rise of the power module due to the elevated thermal resistance of the module and thus accelerates the wire-bond lift off [40].

2.7 Reliability Issues of Integrated Power Electronics System

Power electronics systems which are employed in electric drive systems, hybrid electric vehicles and automotive industry etc. require stringent reliability standards. To ensure the reliable operation in harsh environments, power electronics systems are expected to contain less parasitic inductance and capacitance so that it can handle the overshoot effects during the transient phase of the converter. The interconnection between different components or interconnection within power module adds extra parasitic inductance and capacitance which affect the switching behaviour as well. The higher the interconnection, the package creates an extra thermal path accordingly and adds up thermal resistance which is undesired. Thermo-mechanical failure is prone to interconnection. In order to reduce the parasitic effect from the package, new interconnection technology has attracted a considerable amount of attention in power electronics packaging. Both packaging and manufacturing technology used in building power electronics components significantly determine the costs, functionality, operability and

reliability etc. Now, the reliability issues of capacitor, inductor and power module will be discussed.

Reliability issues of capacitor: The lifetime of a capacitor is highly affected by factors such as electrolyte type, sealing systems and operating temperatures. Temperature effect has been derived from the Arrhenius equation. An exponential-normal hybrid reliability model has also been developed by Sam G. Parler to calculate the lifetime of aluminium electrolytic capacitor [41]. In another report, an Illinois capacitor mentioned load life rating model of aluminium electrolytic capacitor instead of using MTBF (mean time between failures) model [42]. Kemet also has presented a lifetime model based on both the voltage and temperature [35].

Reliability Issues of magnetic components: For the operation in temperature variations (-40°C to +105°C) reduction of CTE between materials (of core and windings) that constitute an inductor result in a higher lifetime. For a wire wound inductor Murata has reported that the use of wound ferrite core in building automotive power inductor shows high reliability [43]. It can withstand up to 150°C which is important for automotive powertrain applications. Again, Ben Oni has mentioned that magnetic manufacturers use the MIL-std test approaches such as thermal shock, burn-in, seal, induced voltage, insulation resistance and electrical characteristics etc. to perform reliability analysis of both the inductor and transformer. They have also found that magnetic component fails more in the open mode [44].

Reliability issues of power module: As IGBT is a multi-layered structure of inhomogeneous materials, it experiences thermo-mechanical stresses during switching operations. Power cycling test is applied until the IGBT module gets destroyed. It is reported in [29] that cracks occur in the solder joint due to the shear strain generated by the CTE (co-efficient of thermal expansion) mismatch between the substrate and the silicon chip when ΔT_j is less than 80K. When ΔT_j is more than 100K, cracks occur in the interface between the silicon chip and the aluminium wire due to shear stress generated due to CTE mismatch between them.

Failure mechanisms have been studied under power cycling with lead-based solder alloys. To improve the fatigue life of the solder joint, new lead-free Sn-Ag based solder alloys are applied and tested. It has been found that the new Sn-Ag based solder depends on the solder joint at higher than around 110K, while the solder crack generation depends on the wire bonds at lower than around 60K [29].

A reliability analysis has been carried out concerning wire bond-lift off and substrate fracture. Solder joint strength has been improved using several dimples etched into the metallisation and a Monte Carlo simulation of 10,000 designs is performed taking into account the uncertainty standard deviation of 0.5% with each given variable [45]. ML-217 [46], reliability prediction methodology is adopted by a number of power module manufacturers to calculate mean time between failures (MTBF). But it results in poor prediction due to the calculation of the failure rate of each component based on statistics. Although, statistics is the easiest approach to study the effects of the design uncertainty and variability on reliability, it is not adequate to consider the time-dependent variability of operating conditions. However, the statistical approach may result in the wrong analysis of reliability if the data is not interpreted properly for the considered assumptions and non-statistical issues (e.g. design change and new generation of components etc.). Other historical failure rate data approaches such as Telcordia [47] and IEEE-1413 [48] also exist. In order to improve the reliability analysis, an approach which could be taken with the combination of numerical modelling techniques with experimentation and accelerated testing have been adopted by Bailey et al. [45]. A response surface optimisation approach with the Monte Carlo method is employed to determine the effects of uncertainty in the design. However, the method is still not robust and cannot be applied to overall power electronics system design [45].

Reliability prediction methods with real-time environmental conditions analysis prognosis and health management system have been developed subject to power modules [49]. The physics of failure based prognostic methods are widely used to determine the lifetime of solder joint due to fatigue. A physics of failure based prognostic method has been developed by Yin et al. [50]. The temperature profile obtained from the compact thermal model is analysed by the rain flow counting algorithm to calculate the number of cycles and the plastic strain in the solder materials at different operating conditions. Plastic strain has been used later to predict the reliability of solder interconnect within the lifetime prediction model. However, the model uses a linear damage rule and history data but it may result in less accurate prediction analysis.

For random failure rate calculation, a modified Arrhenius model is used in conjunction with a Chi Square statistical model [51]. For the analysis of wear out type failures the coffin Manson model is used. In the failure rate of lifetime calculation, empirically derived acceleration factors (AF) are used to de-rate the accelerated stress conditions to a failure rate indicative of actual use conditions [51].

Reliability analysis has also been studied through the physics of failure methods [10]. These approaches include the detailed design of the component, environmental loading conditions and material properties. To perform accurate reliability analysis, damage indicator model parameters are required. Key parameters of a damage indicator model include temperature, stress amplitude, plastic strain range and plastic energy density [52]. These damage indicators are then used later in relevant lifetime models. Power modules lifetime is very sensitive to railway traction profiles. Sn-Ag solder has been studied using the lifetime model of [53] where accumulated plastic strain per cycle and length of the solder joint are the key parameters.

2.8 State-of-the-art of Manufacturing of Integrated Power Electronics System Design

The power electronics industry is continuously focused and targeted to design the product that can meet the increasing demand of low-cost, high-power density as well as high thermal conditions. Power electronics systems are realised into a single integrated block treating electrical, thermal, mechanical and packaging etc. rather than converters based on discrete components [54-55]. Magnetic components mounted on PCB (printed circuit board) or silicon substrates are developed in achieving a higher level of integration of the power electronics system [54]. The design process is quite complex. It requires some design parameter considerations such as electrical topology designing, efficiency, total harmonic distortion and junction temperature etc. In order to improve packaging, there is no set of rules of design parameters of packaging materials identical to the design parameters of electrical modelling.

Power electronics systems are manufactured using discrete technology (see Figure 2.9a) where double sided PCB, wire wound inductor and individual heat sink concepts are employed [54]. Three novel concepts of manufacturing of power electronics system (power converter) have also been reported in this work. The heat conductor converter (see Figure 2.9b) is implemented on a ceramic substrate and bus-bar is attached to absorb heat from active and passive components. A lead frame converter (see Figure 2.9c) has been implemented with the aid of plastic composite nanocrystalline Vitroperm. PCB embedded converter employs passive integration on ferrite polymer composite material C303 and heat spreading and thermal vias [54].

Some published literatures are found related to the integration of Active IPEM (integrated power electronics module) and Passive IPEM (see Figure 2.10) [56-58].

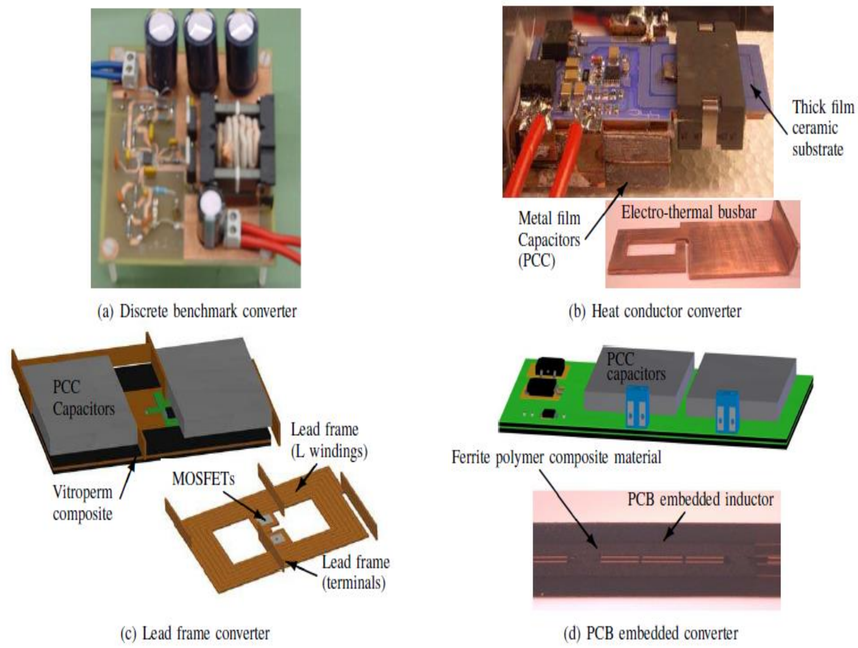


Figure 2.9 Building of Power converter based on different technology platforms [54].

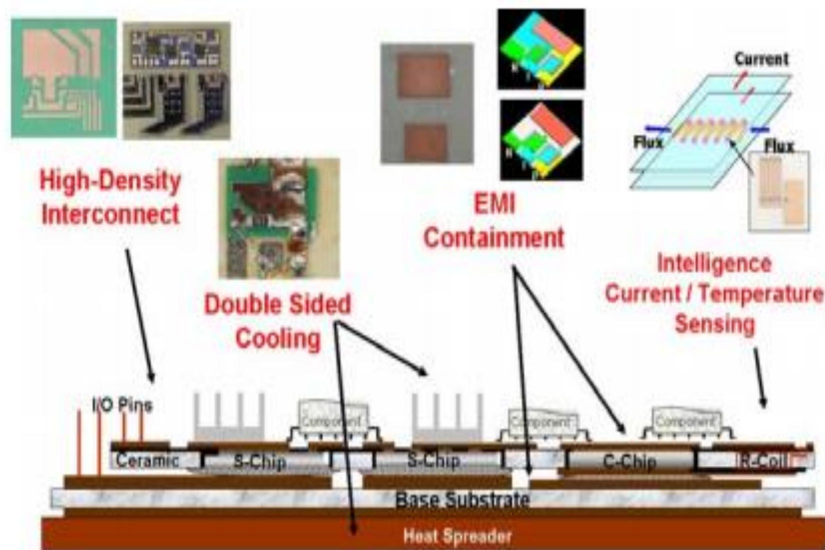


Figure 2.10 Active and passive component integration [56].

Integration of the passive component reduces the dimension of the overall power electronics system [56]. Passive filter size (see Figure 2.11) has been reduced to a 24% by researchers at the power electronics system laboratory at ETH Zurich [57].

At CPES researchers have presented a metal post interconnected parallel plate structure (MPIPPS) (see Figure 2.12) [57].

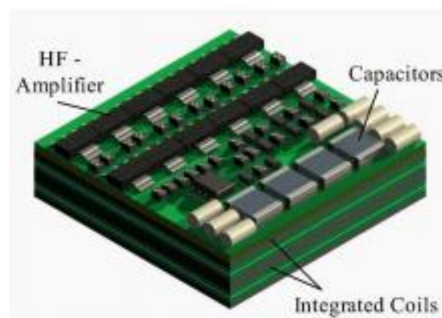


Figure 2.11 3D integrated passive and active EMI filters [57].

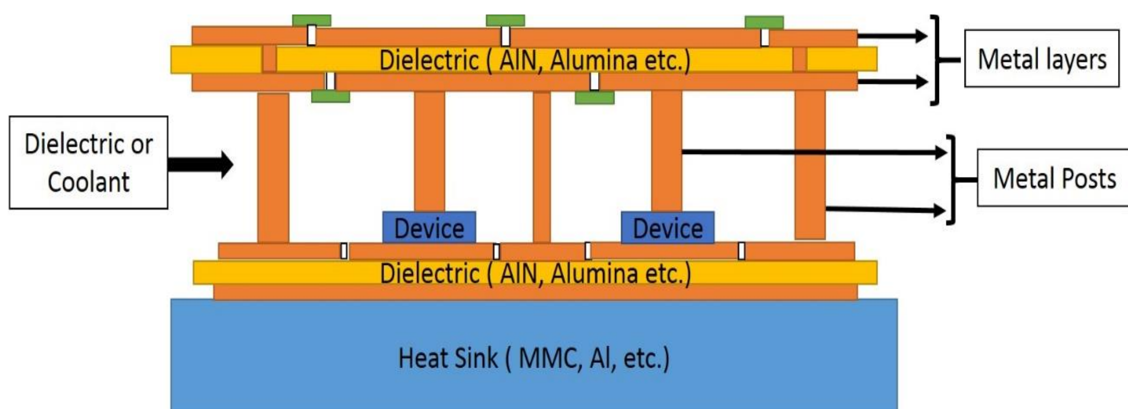


Figure 2.12 Multilayer hybrid metal post interconnected parallel plate structure [57].

Modular approach-based integration is also attempted to design power electronic systems. Both the active and passive IPEM are used to reduce the size of the converter and thus to increase power density (see Figure 2.13) [58]. IPEM based power electronics system is demonstrated for a 1 kW half-bridge DC-DC converter and 1-3 kW motor drive applications. However, for better thermal management integral aspects such as integration, packaging and thermal management etc. need to be emphasised at the system-level design.

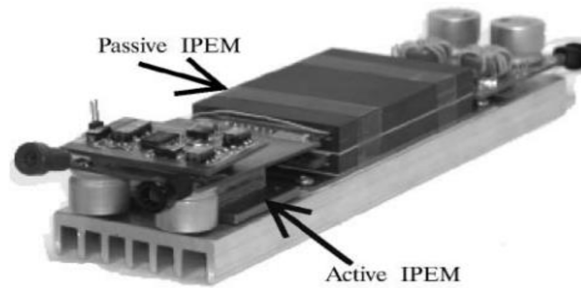


Figure 2.13 Integrated design approach of power electronics system [58].

2.9 Technical Barriers in High Power Density Power Electronics System

Passive components occupy space and add weight [24] in an integrated power electronics system which affects the power density. Power density has been improved by minimising the dimension of passive components. However, the power density is still limited to the factors such as switching frequency, passive component size, cooling system and thermal management etc. [24-26]. Passive integration with active components has also been implemented to reduce the overall size of the power electronics system (see Figure 2.14).

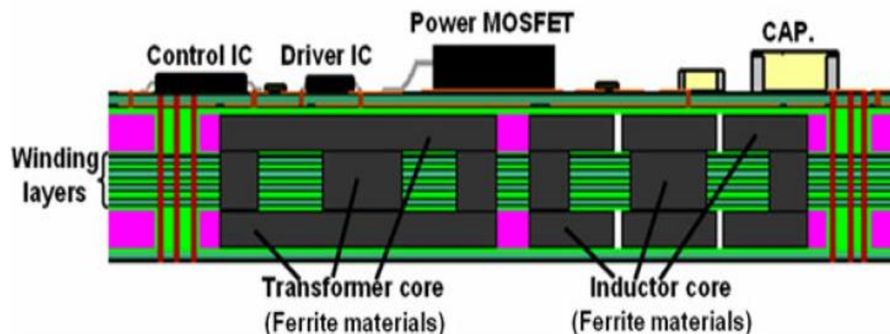


Figure 2.14 Structure schematic of converter based on embedded passive substrate [24].

Passive component integration has been realised through PCB integrated magnetic component designing while windings are designed as PCB tracks and core is placed via the planar magnetic components. The following approach (see Figure 2.15) provides a distinctive advantage of reduction in sizes of magnetic components. Due to this technology magnetic components can be embedded on low cost and thereby, more common ferrite can be made thinner. Thus, more semiconductors can be mounted as magnetic components occupy less space in the surface of the converter. This results in uniform heat transfer over the surface and less electromagnetic emissions due to copper shielding [24]. Therefore, power density gets improved and manufacturing costs get reduced. A synchronous full bridge converter

(48V input, 12V/26A output) is improved though passive integration. However, it is complex to install and capacitive components are not considered which cause difficulty in filter design [24]. In other research, for the reduction of volume of the passive structure PCB integrated air core magnetic component design is also realised in a frequency range of 27.12 MHz [59].

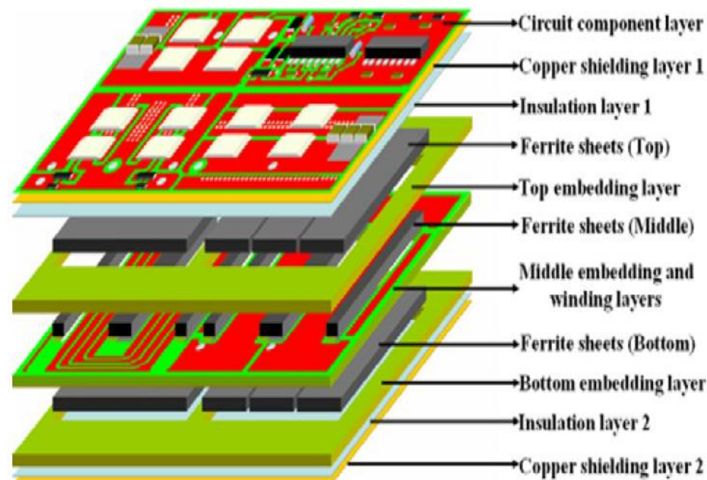


Figure 2.15 Detailed view of converter based on embedded substrate [24].

Achieving high power density is subjected to some of these factors such as increased thermal resistance and sizes of heat sink etc. Factors such as thermal coupling between semiconductors and heat sink and cooling mechanisms of passive components affect the power density significantly [60]. In other research, the power density of a series-parallel resonant converter has been increased by using copper-based heat sink instead of aluminium - based heat sink (see Figure 2.16). Power density has been improved from 9.65 kW/L (aluminium heat sink design for magnetic structure) to 10 kW/L (copper heat sink design for magnetic structure) [61].

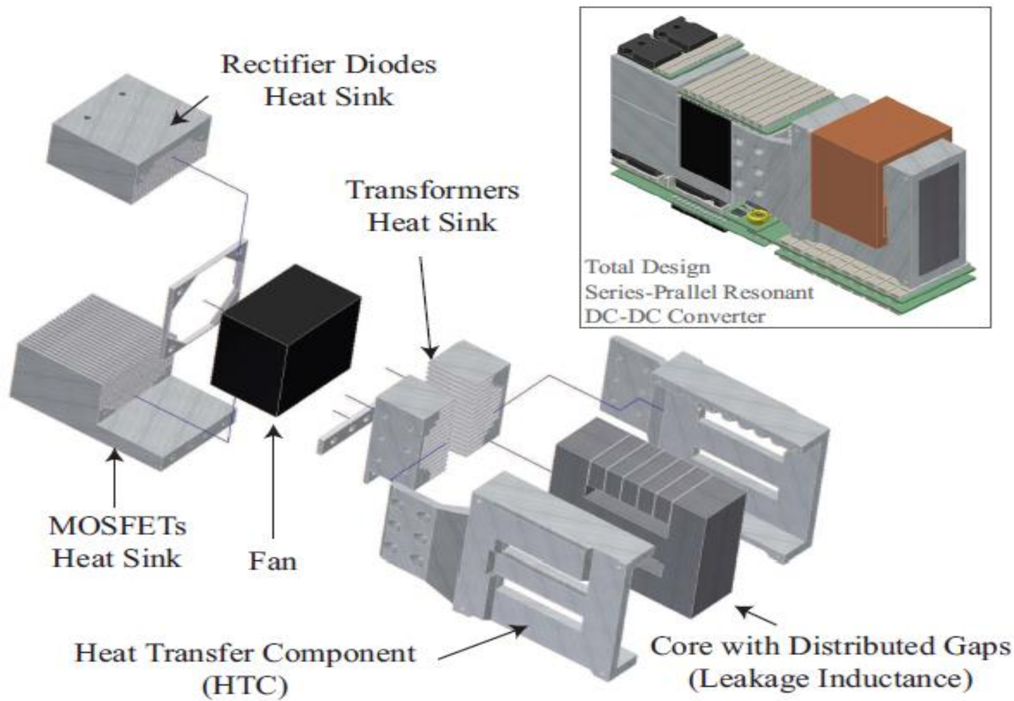


Figure 2.16 Heat sink components for the series-parallel resonant converter, designed for aluminium [61].

So far a power density limit of 28kW/dm^3 at 300 kHz and 44kW/dm^3 at 820 kHz has been obtained for an isolated DC-DC converter and for a three-phase unity power factor PWM rectifier respectively. Also, for a sparse matrix power density limit of 26kW/dm^3 at 21 kHz has been achieved. ECPE has demonstrated two water cooled power electronics systems. One is 75kW/dm^3, 8 kHz motor integrated inverter and other is 10kW/dm^3, 400 kHz, 3-phase PFC with EMI filter and output capacitors [25]. A cooling system performance index has been introduced to determine heat sink designs concerning power density [25]. A design subject to transformer with a double sided indirect air cooling via a heat transfer component (HTC) has been demonstrated. So far referring to the published literature, power density has been achieved by increasing the switching frequency. Switching frequency can reduce the volume of power passive structures but leads to a substantial rise in skin and proximity effect and core loss [25], [59], [62]. However, power loss density due to the raised switching frequency poses a barrier in designing high-power dense and compact power electronics systems.

2.10 Wideband Gap Semiconductor Devices as an Alternative for High Power Density Power Electronics

Si-based power electronics devices are the most advanced and mature technology in the field of power electronics manufacturing. However, Si technology has not been able to withstand high-temperature and high-density power electronic applications due to the reaping demerits of its intrinsic material properties such as the narrow band gap (1.1 eV) which limits the voltage blocking capacity, lower thermal conductivity and the operating thermal limit of 150°C etc. Manufacturing a high-temperature power electronics system device can prevent high temperatures which may be design friendly to decrease the dependency of costly and bulky cooling system design which also reduces the costs and size of the power electronics system.

To tackle the high-temperature issues wideband gap semiconductors have the potential to demonstrate the latent applications in a compact power electronics product design. It has superior electrical and thermal properties compared to Si. The advantages are listed below [63].

- SiC has higher breakdown voltage (say 5 to 30 times than those of Si).
- SiC devices have lower on-resistance and result in lower conduction losses and lead to overall higher efficiency.
- SiC has higher thermal conductivity and thus a lower junction to case thermal resistance.
- SiC has a high operating temperature up to 600°C [64].But most Si based power electronics are limited to only 150°C.
- Forward and reverse characteristics of SiC power devices change slightly with temperature and time and thus SiC devices are more reliable.
- Due to excellent reverse recovery characteristics switching losses are low in SiC-based power electronics [65].

Commercial Status of SiC devices:

In the high-power application, for the 1.2kV device range, SiC is constantly replacing the Si-based devices. Cree introduces a 1.7kV half-bridge module (see Figure 2.17) which exhibits

8-mΩ on-resistance and 10-times higher switching frequency than existing Si module technology and shows the potentiality of replacing Si IGBT modules rated at 400A or more [66]. This new device results in the reduction of size and costs of magnetic and cooling elements while achieving system performance and reliability.

Cree has already developed a 1.2kV three-phase power module (see Figure 2.18) which exhibits 25-mΩ on-resistance and turn-off loss of 0.6mJ [67].

Figure 2.17 1.7kV SiC power module Cree [66].

Figure 2.18 Cree 1.2 kV, 50A, SiC Six-Pack (three phase) power module [67].

GaN: Low cost silicon substrates have brought GaN devices to the market. Azzurro Semiconductors manufacturer offers 6-inch GaN-on-silicon wafer and 200mm wafers are technically feasible [68]. Commercially GaN devices are still not available in the market due to technological maturity and manufacturability. The fabrication of high performance GaN-on-Si high-voltage HFETS is going to be considered as a potential device in future power electronic applications [69]. 650V GaN with lower on-resistance is developed.

Having superior properties of wide band gap devices, Si-based power electronics can be replaced in a power electronics system to make it more efficient. It can be suitable in converter applications where compromises are required to be made in terms of power density, switching frequency, high blocking voltages, efficiency and reliability as well as reduced thermal requirements etc. Applications of SiC devices result in substantial improvements in meeting design targets of efficiency, reliability, size and weight and even, in case of operating in harsh environments. Therefore, wide band gap semiconductor materials are going to be potential to meet the challenges of high voltage, high-temperature and reduced EMI applications.

2.11 Conclusions

An overview of power electronics systems and its markets, technical challenges of power electronics system designing, power electronics system packaging, failure modes of power electronics systems, reliability issues, high power density barriers of power electronics systems and the potentiality of wide band gap semiconductor devices for power dense power electronics systems have all been discussed. The next chapter will discuss losses occurring in power electronics systems, magnetic component loss model, capacitor loss model, passive component thermal analysis and state-of-the-art electro-thermal analysis.

Chapter 3 Review on Electro-thermal Phenomenon and Research Methodology

3.1 Overview of the Chapter

This chapter discusses loss models in active and passive components. The methods that are usually used in the electro-thermal analysis of the integrated power electronics system have also been presented. These methods include the analytical method, finite element based numerical analysis, compact method and reduced order model method. All these methods both have relative advantages and disadvantages in terms of computation, accuracy and implementation etc. The challenges of the electro-thermal analysis and limitations of the existing models are also discussed in detail.

3.1.1 Electro-thermal Interactions

The loss model of the components is an essential part of the electro-thermal analysis. It couples both the electrical and thermal domains (see Figure 3.1). In the electrical domain, power losses are analysed for each component. In the thermal domain, these power losses are fed as inputs which analyse temperature distribution such as finding a hot spot, junction temperature and operating temperature limit etc.

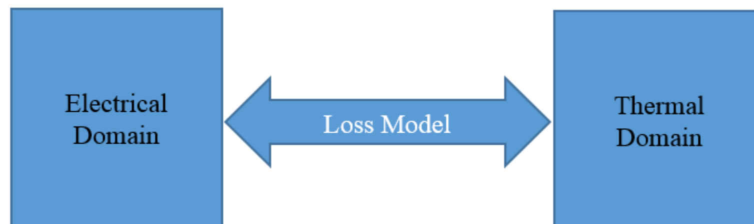


Figure 3.1 Electro-thermal modelling approach.

Electro-thermal interactions are inevitable in a high-power density power electronics system as power losses occur in the component due to various types of loss mechanism. Joule heating is one of them which causes a temperature rise both in active and passive components. At an elevated temperature the component's electrical characteristics such as IGBT/MOSFET on resistance and winding resistance in inductor increase which ultimately enhance the power losses in the components. To capture this electro-thermal interaction, component models should be represented in an electrical network considering the

component's temperature as an input variable parameter. The temperature-dependent component model can then be coupled to a thermal model.

3.1.2 Losses in Power Semiconductor Devices

The construction of an accurate electro-thermal model strictly requires an accurate power loss calculation and integration of the heat generation represented by self-heating and cross-coupling effects. Total power losses can be measured by combining both switching losses and conduction losses over one period of the switching transition. Losses due to turn-on energy (E_{on}) in the IGBT and reverse recovery losses (E_{rec}) in the diode occur simultaneously since the diode is blocked as soon as the IGBT is conducting. Losses due to turn-off energy (E_{off}) occur in the IGBT while losses due to turn-on energy occur in the diode. Losses in diode due to turn-on energy are very small compared to other losses and hence can be ignored in rapid switching processes.

The loss analysis can be carried out by using an analytical loss model of a power semiconductor device. The losses obtained from the analytical model can be compared with those from the circuit simulator and then the results can be used as heat source input to the FEA thermal models to predict the components operating temperatures, i.e. junction temperature.

Conduction losses are common in both IGBT and freewheeling diode. It occurs while both devices experience on state conducting current. As IGBT is not an ideal switch, there will be a voltage drop (V_{CE}) across the device while it conducts current (i_C). These conduction losses can be expressed as the product of the instantaneous current $i_{CE}(t)$ and the corresponding voltage $V_{CE}(t)$ [70]. It can be estimated by using Equation 3.1.

$$P_{conduction}(t) = V_{CE}(t) * i_{CE}(t) \quad \text{.......................... ....} \quad (3.1)$$

Where, $V_{CE}(t)$ is the instantaneous voltage drop and $i_{CE}(t)$ is the instantaneous collector current respectively.

Switching losses are the losses that occur while the IGBT and freewheeling diode experience the switching event, i.e. turn-on and turn- off state [71]. Both turn-on energy and turn-off energy can be calculated by using Equation 3.2 and Equation 3.3 respectively.

$$E_{on} = \int_{t_1}^{t_2} V_{CE}(t) * i_{CE}(t).dt \text{..} \quad (3.2)$$

Where, $V_{CE}(t)$ is the instantaneous voltage drop, $i_{CE}(t)$ is the instantaneous collector current and t_1- t_2 is the switching transition period (on state) respectively.

$$E_{off} = \int_{t_3}^{t_4} V_{CE}(t) * i_{CE}(t). dt \quad (3.3)$$

Where, $V_{CE}(t)$ is the instantaneous voltage drop, $i_{CE}(t)$ is the instantaneous collector current and t_3- t_4 is the switching transition period (off state) respectively.

Switching energy dissipation also affects chip temperature [71]. Equation 3.4 allows a rough calculation of the dependency of the switching energy dissipation for the IGBT and freewheeling diode (FWD). Figure 3.2 shows a graph of typical dependencies of the switching energy dissipations E_{on} , E_{off} and E_{rr} respectively on the value of collector current I_C.

$$E_{sw} = E_{swref} \left(\frac{I}{I_{ref}}\right)^{K_i} * \left(\frac{V_{CC}}{V_{CCref}}\right)^{K_v} * \left(1 + TC_{sw}\left(T_j - T_{jref}\right)\right) \quad (3.4)$$

Where, E_{sw} is the switching energy, E_{swref} is the reference switching energy, I is the operating current, I_{ref} is the reference current, V_{CC} is the supply voltage, V_{CCref} is the reference supply voltage, K_i is the exponent of current dependency (IGBT~1; FWD~0.5 ... 0.6), K_v is the exponent of voltage dependency (IGBT~1.2 ... 1.4; FWD~0.6), $TC_{sw}$is the temperature coefficient of switching losses (IGBT~0.003; FWD~0.005 ... 0.006), T_j is the chip temperature and T_{jref} is the reference chip temperature respectively

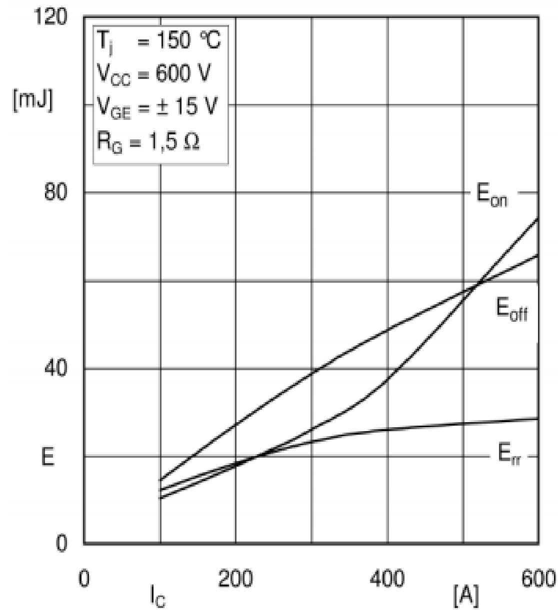


Figure 3.2 Typical dependencies of the switching energy dissipations of an IGBT module on the collector current [71].

Since both conduction losses and switching losses are dependent on junction temperature, these losses should be modelled in terms of junction temperature in electro-thermal analysis.

Conduction losses which are temperature dependent can be expressed as:

$$P_{conduction}(t) = f(I, T_j) \qquad (3.5)$$

Switching loss models which are also temperature-dependent need to be related to dc link voltage and junction temperature. The dependency of the switching loss on the DC link voltage (V_{DC}) and junction temperature (T_j) for a specific device needs to be taken into account in the loss models which can be obtained by curve fitting methods [72-74].

$$E_{Switching} = f(I, V_{DC}, T_j) \qquad (3.6)$$

For low voltage applications, MOSFET is usually used. On-resistance of the MOSFET also contributes to conduction losses. These losses can be calculated by using Equation 3.7. Switching losses due to both turn-on and turn-off switching events that occur in a MOSFET device can also be calculated by using Equation 3.8. Then the total losses are obtained adding up these two losses and it can be estimated by using Equation 3.9.

Analytical conduction loss models for MOSFET [75] are given below.

$$P_{cM} = {I_d}^2 r_{DS(on)} D + Q_{g[V_{GS}]} V_{GS} f_s \quad (3.7)$$

Where, P_{cM} is MOSFET conduction losses, I_d is the RMS (root mean square) drain current in the MOSFET, $r_{DS(on)}$ is the On-resistance of the device for a given drive voltage and junction temperature, D is duty ratio, Q_g is total gate charge, V_{GS} is the peak driver gate voltage for the MOSFET and f_s is the switching frequency of MOSFET (kHz) respectively.

Switching losses for MOSFET can be expressed as:

$$P_{swM} = (E_{onM} + E_{offM}) f_s \quad (3.8)$$

Where, P_{swM} is MOSFET switching losses, E_{onM} is MOSFET turn-on energy, E_{offM} is MOSFET turn-off energy and f_s is the switching frequency respectively.

Total losses for MOSFET can be expressed as:

$$P_{TM} = {I_d}^2 r_{DS(on)} D + Q_{g[V_{GS}]} V_{GS} f_s + (E_{onT} + E_{offT}) f_s \quad (3.9)$$

IGBT is usually used in high-voltage and high-power applications. On-resistance of IGBT leads to conduction losses. Conduction losses and switching losses can be calculated by using Equation 3.10 and Equation 3.11 respectively. Then the total losses can be obtained by summing up these two losses using Equation 3.12. Loss models for IGBT with freewheeling diode are given below.

Conduction losses for IGBT can be expressed as:

$$P_{cI} = V_{CE0} I_{cav} + r_C {I_{crms}}^2 \quad (3.10)$$

Where, P_{cI} is IGBT conduction losses, V_{CE0} is the On-state zero-current collector-emitter voltage, I_{cav} is the average IGBT current value, r_C is the collector-emitter on-state resistance and I_{crms} is the RMS IGBT current value respectively.

Switching losses for IGBT can be expressed as:

$$P_{swI} = (E_{onI} + E_{offI}) f_s \quad (3.11)$$

Where, P_{swI} is the IGBT switching losses, E_{onI} is the IGBT turn-on energy, E_{offI} is the IGBT turn-off energy and f_s is switching frequency respectively.

Total losses for IGBT can be expressed as:

$$P_{TI} = P_{cI} + P_{swI} = V_{CE0}I_{cav} + r_C {I_{crms}}^2 + (E_{onT} + E_{offT})f_s \qquad (3.12)$$

Losses also occur in a power diode due to its on-resistance. Conduction losses and switching losses can be calculated by using Equation 3.13 and Equation 3.14 respectively. Then these two losses can be summed up to obtain total losses of the diode (see Equation 3.15).

Conduction losses for diode can be expressed as:

$$P_{cD} = V_{D0}I_{Dav} + r_D {I_{Drms}}^2 \qquad (3.13)$$

Where, P_{cD} is the diode conduction losses, V_{D0} is the On-state diode voltage, I_{Dav} is the average diode current value, r_D is the diode on-state resistance and I_{Drms} is the RMS diode current value respectively.

Since turn-off energy is less compared to turn-on energy, it can be ignored. Switching losses for diode can be expressed as:

$$P_{swD} = \left(E_{onD} + E_{offD}\right)f_s \approx E_{onD}f_s \qquad (3.14)$$

where, P_{swD} is the diode switching losses, E_{onD} is the diode turn-on energy, E_{offD} is the diode turn-off energy and f_s is the switching frequency respectively.

Total losses for diode can be expressed as:

$$P_{TD} = P_{cD} + P_{swD} = V_{D0}I_{Dav} + r_D {I_{Drms}}^2 + E_{onD}f_s \qquad (3.15)$$

Since IGBT, MOSFET and diode all are essential components in both the buck converter and boost converter, all these loss models can be used in power loss calculation. The DC-DC boost converter design formula is described in Appendix A.

3.1.3 Losses in Magnetics

In power electronics systems, magnetic components such as inductors and transformers are the heaviest and bulkiest which add weight and take space which affect the power density limit and thus require the addition of an extra cooling arrangement. To achieve low-profile and compact structures of magnetic components, switching frequency is being increased. As the magnetic components are not ideal, they dissipate power due to the magnetisation change in the core, eddy current loss, skin effect, proximity effect and Joule losses in winding. All

these losses get increased during high switching frequency operation. This considerable amount of heat generation due to all these losses needs to be tackled and managed as part of thermal design concurrently with the electrical design. The lossy nature of magnetic components in higher operating frequency needs to be explored. Therefore, for the accurate design of magnetic components in terms of both the electrical and thermal domain, it is important to understand the loss model and to study it in the coupled electro-thermal analysis. In order to perform the electro-thermal analysis of magnetic components, losses due to eddy current, skin effect, proximity effect and magnetic flux change need to be determined. The following analytical formulas can be used in copper losses calculation of magnetic components.

Copper Loss, $P_{copper\ loss} = {I_w}^2 R_w$ .... (3.16)

where, I_w is the current through winding and R_w is the winding resistance respectively.

According to the Steinmetz formula, for sinusoidal current waveform of both inductor and transformer core loss can be calculated from the following formula [76].

$P_C = P_h + P_e = k_h f_s B^n + k_e {f_s}^2 B^2$ .... (3.17)

where, P_C is the core losses, P_h is the Hysteresis losses, P_e is the eddy current losses, k_h and k_e are material parameters, f_s is the switching frequency and B is the magnetic field respectively.

In power electronics, waveforms of inductor current and transformer are not sinusoidal. Loss mechanism is a nonlinear phenomenon due to non-linear flux distribution. The major concern is that Fourier series cannot be applied to solve the problems due to this non-linearity nature of flux distribution and thus results in increased core loss (3.8%) [77]. Steinmetz's equation has been modified due to non-sinusoidal flux distribution.

A modified Steinmetz equation is developed by Albach et al., assuming the domain wall motion losses on $\frac{dB}{dt}$ [78] [79] and the equivalent frequency is calculated from the following equation

$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt}\right)^2 dt$.......................... .... (3.18)

Using equivalent frequency and repetition rate f_r in the Steinmetz equation core loss can be calculated as:

$$P = k{f_{eq}}^{\alpha-1} B^{\beta} f_r \qquad (3.19)$$

A major drawback in this model is that arbitrary assumption of frequency affects accuracy in calculating core loss.

A generalized Steinmetz Equation (GSE) is proposed by Li et al., based on the idea of assuming instantaneous power loss depends only on instantaneous B, $\frac{dB}{dt}$ expressed as $p(t) = f(B(t), \frac{dB}{dt})$ [80].

Combining the instantaneous power dissipation with the Steinmetz equation yields

$$P(t) = K_1 \left|\frac{dB}{dt}\right|^{a} |B(t)|^{b} \qquad (3.20)$$

Results show that it is worse than MSE.

An improved generalized Steinmetz equation was developed by Venkatachalam et al., based on the idea of losses depending on whole cycle, not just $B(t)$, $\frac{dB}{dt}$ [81].

GSE was $\overline{P(t)} = \overline{K_i B(t)^x \left|\frac{dB}{dt}\right|^{y}}$ (3.21)

Above loss models can be employed in the estimation of both copper and core loss. Core loss calculation is much more straightforward in DC-DC converters. As the flux swing is constant in DC-DC converters, core losses can be easily calculated from the manufacturer-provided data sheet. But flux swing in PWM-based (pulse width modulation) inverters does not remain constant. Experimentally both electrical measurement and calorimetric measurement can calculate core loss. Electrical measurement which takes the voltage and current and thus the multiplication of both gives the power loss of a device under test. In the calorimetric measurement, $T = at + b$ is used to linearise the temperature rise of the calorimeter box and parameters are calculated through the least square fit function. Flux swing in each switching interval has been taken into account in the calculation of core losses [82]. One disadvantage of this method is the long-time which is required to reach the steady state temperature. This has been solved by adding higher order frequency term in the calculation of core losses for any periodic flux waveform [83].

Loss calculation can be performed by electromagnetic finite element analysis. FEA can estimate copper losses by using current distribution and core losses by using magnetic flux

distribution. The advantage of the FEA model is that it removes the difficulty of experimental set up to calculate losses. It can also take into account AC resistance effect in the calculation of core losses. AC copper loss has been minimised using multistranded Litz wire [84].

3.1.4 Losses in Capacitor

Capacitor is known as an electrical energy storage device. It offers the benefit of filtering the harmonics and ripple from the AC/DC voltage signal at the rectifier end of the inverter circuit or stabilising the DC output voltage from the batteries/fuel cell in electric/hybrid vehicles. It can also suppress the presence of electromagnetic interference in the form of electromagnetic noise in power electronics converter applications. These benefits have accelerated the potential applications of capacitors such as the aluminium electrolytic capacitor and film capacitor in various power electronics systems such as consumer electronics, electric/hybrid vehicles and industrial power electronics applications, i.e., three-phase inverters, electrical drives etc. Capacitors consist of two electrodes and these electrodes are separated by the dielectric. The dielectric materials usually are mica, oil, air, ceramic, plastic film and oiled paper etc. A ripple current flows through the dielectric in a capacitor and thus forms the power of heating generated due to the dielectric resistance of the capacitor. Thus, the Joule heating effect is observed in the capacitor and heat is dissipated in the form of thermal energy. In high frequency operation, there is loss tangent. When the AC signal goes through capacitors, then dielectric materials tend to absorb some of the energy. A dissipation factor is applicable for low frequency whereas loss tangent is applicable for high frequency [85-87]. The performance and life expectancy of the capacitor however, depends largely not only on the converter operating conditions such as voltage and current etc. but also on the capacitor's operating temperatures. To determine the hotspot temperature inside the core of the capacitor, the temperature-dependent electrical model is required to represent the electro-thermal interactions occurring in the capacitor due to the Joule heating effect in the dielectric. The typical lumped element model includes a lossless ideal capacitor in series with a resistor named as the equivalent series resistance (ESR). This model can be used in a circuit simulator to estimate the loss calculation due to high ripple and peak current through the capacitor. Figure 3.3 describes the loss behavioural circuit component model of the capacitor in series with an ESR.

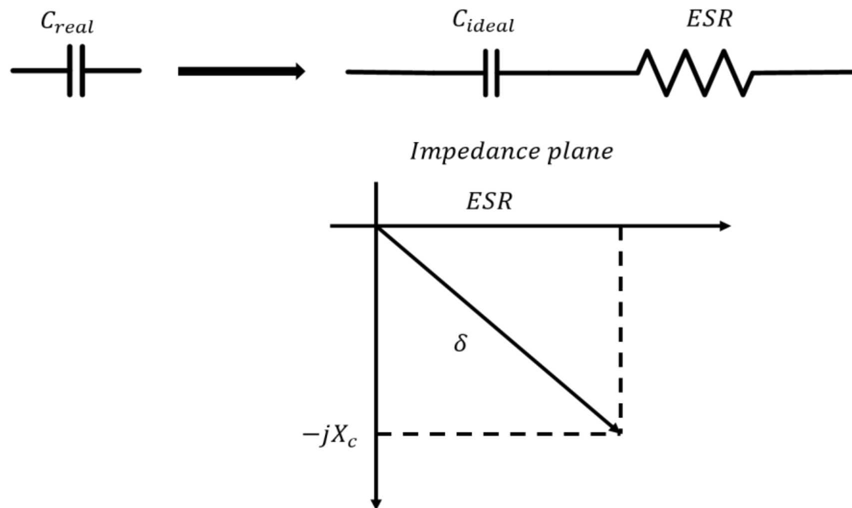


Figure 3.3 A real capacitor has a lumped element model of a lossless ideal capacitor in series with an ESR [88].

ESR can be calculated by using Equation 3.22 [85].

$$ESR = \frac{\sigma}{\varepsilon\omega^2 C} \quad (3.22)$$

where, σ is dielectric's bulk conductivity, ε is the lossless permittivity of the dielectric, ω is the angular frequency of the AC current and C is the capacitance respectively.

Dissipation factor can also be calculated using Equation 3.23 [85].

$$\tan\delta = DF = \frac{1}{Q} = \frac{ESR}{X_C} = \omega C.ESR = \frac{\sigma}{\varepsilon\omega} \quad (3.23)$$

where, δ is the loss angle, DF is the dissipation factor, Q is the quality factor, ESR is the equivalent series resistance and X_C is the reactance of the capacitor respectively.

Power losses in a capacitor can be calculated by using Equation 3.24.

$$P_{losses-C} = {I_{Crms}}^2 * ESR \quad (3.24)$$

where, I_{Crms} is the capacitor RMS current, ESR is the equivalent series resistance and $P_{losses-C}$ is the power losses in the capacitor respectively.

All these loss models can be used in the calculation of losses of the components of power electronics systems. These estimated losses can further be used in thermal analysis to predict temperature rise of the components.

3.2 Electro-thermal Modelling Approaches

Electro-thermal modelling is a systematic approach where the thermal energy dissipated in the components is studied and analysed with the help of integrating electrical and thermal model. There are several methods that have been used by many researchers in the electro-thermal analysis of active components in power electronics systems. These methods can be classified into four groups. These methods include the analytical method, finite element based numerical method, compact method and model order reduction method. At first, the electro-thermal analysis methods are presented in detail and later their merits and demerits are discussed.

3.2.1 Analytical Approach

Electric current/potential and temperature distributions are governed by partial differential equations (PDE). In some cases, with certain assumptions the problem can be simplified so that analytical solutions can be found for the most important variables such as the gross electric current and junction temperature etc.

To perform the electro-thermal analysis of a power electronics system, an accurate estimation of power losses in the switching devices is important. A simplified behavioural loss model of the semiconductor device that ignores detailed physics, i.e. thermal effects in its on-resistance may incur the wrong estimation of conduction losses. The model is required to perform the wide range of switching cycles under the various loading conditions such as currents and temperatures. Therefore, the model needs to be accurate and fast in terms of computational speed.

The modelling of temperature dependent switching characteristics at the device level has been widely studied and discussed in the literature through several switching loss models used to predict the loss [89-91]. Some are relatively simple but require experimental data [89-90], while the other is based on a more complex mathematical representation of ambipolar diffusion equation [91] which requires longer simulation times and poses difficulty in integrating into circuit simulators such as SPICE and PLECS etc. Blaabjerg et al., in [89] , have outlined an analytical switching loss model for non-punch–through and punch-through IGBT considering power loss as a function of the load current, DC-link voltage and the temperature. Byrant et al., in [90], have presented an accurate physics-based IGBT and p-i-n diode models for circuit simulator and have used Fourier series to solve an ambipolar diffusion equation in semiconductor material. They also have extracted the parameters for

both the IGBT and diode models such as active die area, high-level lifetime, drift region width, drift-region doping and emitter recombination parameters from both the simulation and clamped inductive load test. Igic et al., in [91] , have formulated an analytic study of physics-based dynamic electro-thermal models of power bipolar devices such as (PiN diode and IGBT) and have applied a 1D ambipolar diffusion equation to derive the compact electric models for the PiN diode and both the punch-through and non-punch through (PT and NPT) IGBT devices which can take into account the effect of temperature. Maw by et al., in [92] , have outlined a junction temperature dependent device physics based compact model for IGBT and PIN diode which have been used in calculation of inverter power losses using a look-up table of device losses and attempt to observe the effect of the temperature changes of devices due to the changes in the loading profile of the hybrid electric vehicle converter. Palmer et al., in [93], have developed a quasi 2-D model which captures certain features of the collector voltage at turn-off, such as the slow rise of the collector voltage during the gate voltage before the current falls [93]. It has been noticed that the self -junction temperature dependent loss model developed in [89] and the model in [91] have not been coupled with the circuit simulator except the model in [91] through a thermal node to the electrical model. However, the models outlined in [89-91] do not take into account the effect of other adjacent components temperature influence if the device is placed close to each other at the system level, for example, components are mounted in the heat sink. In addition to this, these models are cumbersome to be able to be fit into the circuit simulator at the system level due to the estimation of power losses by either extraction of parameters from experimental measurements [89] or the solution of analytical ambipolar diffusion equation [91]. Particularly computational time and performance matters in the applications like hybrid electric vehicle inverter whereas load profile changes due to operating conditions. To speed up the simulation, a look-up table based device loss model is applied which takes into account the temperature generated due to changes in load profile [92]. However, the model uses interpolated data for the particular switching time which may not accurately predict the device junction temperature. In addition to this, thermal interactions from adjacent components should be included to improve the model.

Several previous works related to analytical modelling of the active components package at the system-level have been found and discussed in [94-96]. Du et al., in [94], have applied Fourier series to solve one dimensional and two-dimensional transient heat conduction problems in packages (system level). Lu et al., in [95], also have dealt with heat dissipation

problems in IGBT modules using a Fourier series method [95]. While Swan et al. in [96], have implemented Fourier series to solve a 3-D heat equation for an integrated power module that consists of a diode and an IGBT chip [96]. The model presented in [94] considers a 1-D heat transfer while in [95] a 2D heat transfer model has been studied. In [96] the model solves a 3-D heat transfer. A 1-D model is easier to implement than a 2-D or a 3-D model due to simplistic boundary conditions. The model presented in [96] is more robust than the model of [94-95]. However, the model only considers one IGBT chip and one diode. It does not take into account other adjacent IGBT chips and diodes and also ignores the temperature dependency of the material properties [96]. Moreover, Fourier based solutions take time to reach accurate solutions since these must compute a large number of Fourier terms. Therefore, this method is not realistically feasible to apply in modelling the thermal interaction between chips in the multichip power module. In consideration of our research aim, the above-described models seriously lack in other components interaction, only deal with certain boundary conditions and even avoid chip to chip effect and interaction of the other passive components. Moreover, the challenge is how to incorporate this model in concurrent electro-thermal analysis at the system level.

3.2.2 Finite Element based Numerical Method

When the analytical approach cannot be used to analyse electro-thermal problems for structures with complex geometry and boundary conditions, numerical approaches are applied to solve the governing partial differential equations (PDE). The numerical approach such as Finite Element Analysis (FEA), Finite Difference Method (FDM), Finite Volume Method (FVM) and Computational Fluid Dynamics (CFD) can all be used to solve electro-thermal problems.

While FEA and other numerical methods can be used for heat transfer analysis directly, they can also be used to extract parameters that are used in other analysis methods. For example, by using FEA, Chan-Su Yun et al. in [97], have extracted RC parameters to predict the thermal characteristics of an IGBT module mounted on a water-cooled heat-sink and have predicted the Elmore delay which characterises the propagation delay of the heat flux through each layer of the package [97]. Several previous works related to parameter extraction have been demonstrated in the literature with system level applications. For instance, Luo et al. in [102], have studied a three-phase inverter power module. They have extracted thermal network parameters from both experimental and FEA-obtained transient thermal impedance from junction to case and have compared the two methods. Two other important research

works related to parameter extraction have been found. Zhou et al. also have investigated three-phase IGBT inverter module and have generated a compact model through the use of Flotherm software [98]. In order to calculate thermal time constants more accurately, Ciappa et al. have developed a modified Elmore extraction method in [99]. In the Elmore technique, the thermal impedance at each layer obtained from the step response of the FEA model of IGBT has been described as a first order approximation by two weighted exponentials [100]. Again, Habra et al. have proposed a new methodology for the extraction of dynamic compact thermal models through FEA [101]. The model can be easily employed in analysing multiple heat sources and further application in generating a simplified compact model. The parameter extraction methodologies demonstrated in [97-101] still need to be improved to study non-linearity effects. The above-mentioned parameter extraction process [98], [101-102] can ease the thermal simulations and provide the more accurate results. One big disadvantage of this FEA based thermal equivalent network parameter extraction method is the long computation time. It also assumes simplified convective boundary conditions and applies at the bottom of base plate for modelling heat convection from the base plate connected to the heat sink with thermal grease. A simplified boundary condition does not represent the dynamic thermal performance of the cooling condition and thus incur errors in a thermal simulation. Dynamic thermal effects are also very difficult to analyse as the electrical models are also temperature dependent, e.g. on resistance of the switch. In addition to this, power loss incorporation from each step of the circuit simulator poses a serious difficulty to ensure coupling to FEA thermal analysis. However, due to the increased cost of computation time and difficulty in integrating into a circuit simulator, the FEA approach is still not practised extensively by power electronics engineers at system-level design.

A mixed method combining FEA and CFD has been found in [103]. Bennion and Kenneth Kelly have analysed system-level performance of a power module package configuration and characterised a package's thermal behaviour by using both the FEA method and CFD. This work has been found quite helpful for the design trade-off analysis associated with alternative packaging configurations and thermal management technologies for power electronics [103]. A limitation of the method is that the thermal resistance is simplified considering convection only on the surface area of the package whereas the mass flow rate affects the performance of heat-sink. However, the idea of using both the FEA method and CFD can be helpful in our system-level integrated power electronics system design but the problem lies in coupling,

computational time, model interchange and model parameters updating as well as in non-linear interaction of the components.

3.2.3 Compact Method

FEA-based models are detailed modelling, therefore, require extensive amounts of computational resources and design time. A compact thermal model is a simplified representation of a lumped thermal RC network for determining specific locations such as the prediction of the junction temperature in a power module. The compact model is also called a lumped thermal network model. Compact models are solved by conventional circuit simulators such as PSPICE (Personal Computer Simulation Program with Integrated Circuit Emphasis).

At the system-level design, electrical circuit simulation is a simple and effective technique to describe the electrical state of power electronics systems. Circuit simulators such as PSPICE cannot be used to predict current density and electric potential distribution.

Circuit simulators use an RC-type network to predict the junction temperature of a semiconductor device with the help of device behavioural models that link electrical parameters to junction temperature. An RC network can be built from manufacturer-provided data sheet parameters or empirical parameters or even from FEA-extracted parameters. The compact thermal model also uses an RC type lumped parameter network rather than going into detailed modelling and hence avoids actual package geometry. Compact thermal model is quick to be solved, but it ignores details of physical behaviour.

Thermal network-based modelling of an integrated multichip power electronics module using has been studied by Rodriguez et al., in [104]. Also, some works are undertaken in detail to estimate the temperatures with the aid of building a thermal model by using the extracted thermal parameters. Such works are described in [105-107]. Blasko et al. have outlined a third order thermal network model by extracting parameters from the manufacturer-provided thermal datasheet [105]. Both Martin Marz and Paul Nance have proposed a thermal equivalent RC network using the parameters extracted from transient thermal impedance [106]. Again, Igic et al. have applied a deconvolution method for the extraction of RC thermal network parameters. The method is based on either measuring or modelling thermal transient response function of the device for a step function excitation [91]. In order to run the simulation fast Huang et al. have adopted a look-up table based approach in the power

loss calculation rather than slow physics-based compact device models. They mainly have focused on deriving a thermal network extracted from heating curves of the IGBT junction and case temperature which are measured on a power cycling rig [107]. The methodologies described in [91], [107] do not take into account the effect of cross coupling effects in the critical layers. The power electronics module consists of multiple chips mounted on the same substrate in the same package which undergoes heat generation due to power losses in each chip during its operation and this heat flows inside the package crossing multiple layers of different material before reaching to a heatsink. Thus, the module experiences complex thermal behaviour and the cross-coupling occurs when all dies share the same substrate and heatsink. However, the thermal network obtained in [91], [107] is not applicable to address this lateral heat spreading and cross-coupling effect of the multichip power module.

Cross-coupling thermal influence in a compact power module has been studied by few researchers and these works have also been documented well in [108-109]. Musallam et al. have developed a compact thermal model of IGBT power module considering the cross-coupling effect for PWM based current controlled full-bridge inverter [108]. While Zhou et al. have developed a compact thermal model for a three-phase inverter [109]. The difference lies in the model set up. In [105] , the model considers the transient response from experimentally passing the current through the dies experimentally while the model in [106] needs a detailed physical description of the package both in terms of geometrical dimensions and the material properties of the constituent material of the package. However, still, the methodology needs to be updated considering mutual component interaction and more research interest on FEA-based parameter extraction for other passive components as well has to be drawn.

Electro-thermal problems can also be solved by using a combination of circuit simulator and finite element analysis. To avoid the process of experimentally obtaining the thermal impedance curve for the power modules at different layers, FEA-based simulations are used. Step input power is applied to obtain the thermal impedance curve. Nejadpak et al. have used the FEA method to extract the RC network from transient thermal impedance to model the electro-thermal behaviour of SiC IGBT devices [110]. A similar type of approach has been adopted by Kojima et al., in [111]. The model in [111] is quite suitable for MOSFET thermal modelling which considers device physics in the model. The coupling between the system-level circuit simulator and FEA thermal model may incur convergence issue because of simulation solver settings. The model in [106] and [108] can be used in our proposed research

but still needs to include more detailed non-linear parameters for example temperature dependent parameters either thermal conductivity or electrical on-resistance and further research how well the model can be integrated into a circuit simulator.

Few researchers also apply the Foster network and Cauer network in the electro-thermal analysis. The Foster and Cauer networks are the simplest ways of representing a 1-D heat transfer problem in power electronics module. The foster network model parameters are commonly derived from the manufacturer-provided datasheet. The Cauer model is based on the physical materials properties of the components. In the Foster model parameters do not represent physical structure of the device. It can solve easily a 1-D problem in a single chip but it cannot describe multichip thermal interaction problem sufficiently. Therefore, the use of present form of thermal model is limited in application and cannot be further extended [100].

From the thermal impedance curve, which is usually found in data sheets, a curve fitting technique is applied to derive four RC circuit networks. Thus, the Foster network describes the thermal impedance of the whole device and the individual points in the module cannot be considered [112].

Cauer network is derived from the physical structure of the IGBT or experimental tests. Each layer consists of thermal resistance and thermal capacitance which can be clearly obtained from its resultant dimensions and thermal properties. To improve computing speed, reduction of an RC thermal model from the seven layers to three layers is demonstrated by Mussalam et al. [113].

The key difference between Foster and Cauer model is that the Foster network node to node heat capacitance does not correctly represent heat flow [112] while the Cauer network represents real heat flow through the inclusion of node-to ground capacitances in the thermal model [112], [114]. Cauer network can predict the thermal response of each layer with respect to a corresponding layer. However, to guarantee accuracy in the thermal simulation, a network of two or more RC pairs is required. Foster and Cauer networks are interchangeable and with the knowledge of one of the networks, the other networks can be derived [100].

Drofenik et al. have offered a numerical solution regarding circuit simulator for loss calculation of power semiconductors. It calculates losses by multiplying the actual current through the IGBT with the curve fitted conduction loss equation which is of second order

polynomial. This aids in loss modelling but there is no implementation of thermal coupling that affects estimation of junction temperature [115].

3.2.4 Model Order Reduction Method

Detailed FEA simulation is computationally costly. Compact models aim to simplify the thermal model into electrical network equivalents. Reduced order thermal model is pursued to decrease the number of degrees of freedom needed to represent the overall behaviour of a large system and generates a dynamic compact thermal model and thereby improves computational efficiency.

In order to reduce the maximum terms or functions of a large system, the reduction of sparse matrix model has received a lot of attention in literature i.e. keeping the accurate information of the models with minimum computation effort. Recent proposed methods are based on Arnoldi iteration method and the Krylov subspace method. The method adopts the pole/residue representation and the assumption of conjugate pairs to offset the stability requirement. A state space representation is then realised and reductions are performed accordingly. The reduced state space representation is converted again in partial fraction form. An application of model order reduction technique is i.e. generating compact models. In [116] Evans et al. have proposed a fast method for dynamic thermal impedance extraction for multi-chip power modules using finite difference mesh and GMRES (Generalised Minimal Residual Method) algorithm which is based on the Arnoldi iteration. Again, Hauck et al. have implemented the Arnoldi algorithm to study power devices on PCB and have extracted spice equivalent thermal network [117]. In other research, Augustin et al. have demonstrated the application of the model order reduction method for power device with multiple heat sources [118]. Again, Habra et al. have outlined a methodology to extract a simple and user friendly compact model including layer by layer thermal resistor network structure for each components or systems with single and multiple heat sources [119]. The reduced order model shows very good correlation with the measured results. The model can be quite useful in our proposed research where multiple heat sources are considered in thermal simulations and the reduction of computation time can be achieved by using this technique. Both the work in [116-119] represents the application of model order reduction and does not deal with the actual power electronics behaviour. In addition, these models lack demonstration of the extraction of any equivalent thermal network that can be used to evaluate junction temperatures of semiconductors. However, the modelling approach can be adopted in power electronics converter simulation. But, the work [116] is exceptional in the

sense that it has shown for the first time an automatic extraction of PSPICE equivalent thermal network including thermal coupling. The obtained thermal network can be easily exported in a circuit simulator. The method seems quicker than the traditional curve-fitted models generated from the FEA results. Furthermore, the reduced order model can be quite useful in operating the coupled electro-thermal simulation.

Table 2 represents the comparison of various thermal models adopted by researchers so far in terms of accuracy, complexity and device level/package level interfaces. Most of the models use curve fitting and RC parameters extracted from the FEA in literature and hence are relatively complicated [100].

Table 2 Comparisons of different thermal models from the literature

Thermal Modelling Approach	Complexity in Computations	Individual layer dimension required	Accuracy	Experimental input	Multi-chip interface	Comments
Foster [120] [112]	Simplest	No	Universal less accurate at high frequencies	No	No	Usually used by manufacturers
Cauer [113], [114]	Less complex	Yes	Universal Accurate	No	No, Difficult 1D	Usually used
FEM [98],[101-102]	Less complex but time consuming			No	modelled	Large computation time and memory
Modified Elmore (Ciappa) [99]	Complex less time consuming	Yes	Universal More accurate	Experimental validation at certain points	modelled	Combine FEM and two terms RC parallel Circuits
FEM+ Multi exponential [114]	Complex Less Time consuming	Yes	Most accurate	Experimental validation at certain points only	modelled	Combines FEM and RC parallel (Usually four terms) circuits
Fourier [96]	Complex	Yes	Universal	No	Modelled	Thermal diffusion based, computation time high
Hefner's model [121]	Complex	Yes	Accurate	No	Modelled	Finite difference method
Model order Reduction [116]	Complex but less Time consuming	Yes	Most accurate	No	Modelled	Model order reduction

3.3 Challenges and Limitations of Existing Electro-thermal Analysis

In a compact high-power density power electronics system, components generate a considerable amount of heat and the proximity of the components hinders heat dissipation. This makes it difficult to control the temperature in such systems. Currently, electrical and thermal simulations are designed separately which produce design errors and increase costs. Furthermore, the interactions among components are ignored in power electronics system design. In addition, the loss models of semiconductor devices are inadequate and simplistic because nonlinearity effects are not taken into account. Regardless of these issues, the simulation speed can also be a key factor in the analysis of the long-term in-service mission profile. All these issues need to be considered carefully to achieve an accurate electro-thermal analysis framework. In the following section, these issues in electro-thermal design framework of power electronics systems will be discussed.

3.3.1 Limitations of Existing Models

The research works that have been carried out so far in electro-thermal modelling of power electronics components and systems do not cover all the design aspects. For example, few of them have used power loss calculation that is based on realistic device models [122-124] and most thermal analysis are focused on components avoiding detailed analysis of thermal coupling effect and non-linearity [104-105], [111], [125-129]. Some researchers have studied device power loss models [130-134] or power loss estimation and thermal models [135-137] but they have not used these models for system level design. Only very few researchers have tried to cover all the design aspects such as electric-thermal interaction, cooling, weight, volume and cost etc. but then the models are either lacking in detail [138] or some portion of the model is too simple [139]. For SiC-based power electronic systems, only in a few publications detailed electro-thermal modelling has been found [140-144].

Generally speaking, the power loss model can be divided into two categories. The first is based on empirical models. These models are used in simulations as either curve fitting equations [145] or look-up tables [89] which are derived by using power loss data from circuit simulation results. Examples of the demerits of empirical models include (1) the test bed has to be constructed (2) test results may be inaccurate, (3) it is costly and time-consuming and (4) it can be applied only for specific conditions.

The other category of loss models is mathematical models for which load currents are regarded as current sources which remain similar for the switching period. Then power losses are calculated by averaging the instantaneous current, voltage and device characteristics in a period [146]. In comparison to experiment based empirical models, it is more efficient. It is quite tough to simulate real current and voltage in complex power electronics systems such as PWM-controlled inverters. To precisely model, the average value of the current is calculated using PWM modulation index instead of taking the value of instantaneous current and voltage [136]. This method improves the efficiency in computation and it can quickly solve a complex power electronics system with the control strategy which is being taken into account in the model equations.

For the thermal analysis of power electronics systems, many researchers have implemented very similar methods. The device loss models that are used in the analysis coupled to the simplified thermal network. Most of them are limited only to predict the junction temperature rise in IGBT power modules [140-144]. The differences are noticed in the ways of extraction of thermal parameters and the solution algorithms. The curve fitting method is widely used in extracting thermal parameters [139]. Few provide the thermal response to the step power input of the power semiconductor device in the time domain [147] and frequency domain [141].

For power semiconductor devices, experiment-based models are often used in the electro-thermal analysis because the models are simple to implement and temperature effects can be included easily [89], [136-137], [146]. There are also simulator-based models which ignore temperature dependency [131-132], [139]. Analytical methods are simple to use, but they do not consider the effect of temperature changes [133-134]. Therefore, it is not the best choice in modelling the power electronics system.

The following sections cover more on existing power electronics semiconductor device model research.

Recently a lot of papers have been published on device models. The models can be quite complicated. Some widely used methods are classified into a few groups and the relative advantages and disadvantages are discussed below.

1. Analytical models

Analytical models are mathematical formulae that are used to describe device behaviours. They are used to model fundamental physics equations under precise conditions [148-150]. Analytical models are useful to analyse the simple geometric package structure when it is applied under simple boundary conditions. But these models are sensitive to changes of system characteristics. With accurate design, only a small set of parameters are needed and reasonable accuracy can be guaranteed at the cost of low computational effort.

2. FEA based models

Physics based models solve partial differential equations that govern physical phenomena in semiconductor devices. The variables such as the potential distribution, carrier concentration and current density etc. can be solved [151]. These models are widely used to understand the performance of the devices. In general, non-linear partial differential equations do not have analytical solutions. Various techniques such as finite element analysis [98], [101-102], Laplace transformation and lumped-charged method [152-153] are applied to solve the equations. Physics based modelling provides detailed results that have physical significance. But it is complicated to use and computationally costly. On top of that, the accuracy relies on the model parameters used. The model requires a large number of parameters such as structural parameters (related to device design), physical parameters (related to material, physical phenomena) and electrical parameters as well as thermal parameters etc. which are sometimes difficult to extract. Only a few research papers have provided the required parameters and few works are found related to parameter extraction methods [98], [101-102]. From an engineering perspective, this method is difficult to apply. Finite Element Analysis (FEA) and other software packages are also widely used to solve heat transfer problems [121], [154-155]. FEA is more complicated than FDM but FDM requires rectilinear cells. In general, FEA more accurately solves heat transfer problems compared to FDM [156].

3. Circuit/Compact models

Thermal behaviour can be analysed by circuit type network models. Circuit simulators such as PSPICE, SABER etc. can model the device junction temperature using thermal equivalent networks [157]. RC-type lumped parameters can be derived from the manufacturer-provided datasheets, experimental results or FEA results. This method is accurate and fast and easy to implement in circuit simulators but does not provide detailed information about the temperature distribution across the component or between components.

Basically, an RC thermal equivalent network can be classified into two types. These include a Foster network and Cauer network. A Foster network uses data sheet parameters and does not have a physical significance. A Cauer network is derived from physical structure of the components or FEA results which takes the physics into account.

In realistic applications, the thermal network can be extracted from the transient thermal impedance curve provided by semiconductor device manufacturers and the thermal network can be used as the tool to estimate the peak junction temperature of the device [158]. This transient thermal impedance curve is obtained based on the convolution method. However, it only regards the typical operating conditions and does not take into account the dissipated power for pulse width in the order of the few microseconds. In [159] the equivalent RC thermal network including thermal resistance and thermal capacitance, offers a solution to integrate the thermal model with the electric circuit model.

Converter design can also be carried out using circuit and thermal simulators such as PSPICE [160-161], SABER [104] and PLECS [107]. In these software packages, power losses can be input as a function of the junction temperature which can be obtained from the simulator and thus a feedback loop is formed. Electro-thermal simulation uses compact or physics-based device behaviour models in combination with heat sink models [162-163]. An IGBT electro-thermal model has elements for gate, collector, emitter and this could be connected to heat sink equivalent. In PLECS [164] (Piecewise Linear Electrical Circuit Simulation), heat sink is linked to a thermal chain which consists of an RC type network. In any of these commercial simulators, electro-thermal modelling of the power devices is an essential part of a simulation. But this needs precise although but not too complicated electro-thermal models of the power semiconductor device.

4. Reduced order thermal model

The high-fidelity FEA model can provide accurate temperature prediction since the geometrical and thermal properties can be modelled in detail. However, it requires a special time domain simulation solver and takes much time to solve. Reduced order thermal models are another way of representing large system. Relatively, it is much faster, because it decreases the number of degrees of freedom and thus enhances computation speed. It is less accurate than detailed FEA analysis but requires a model order reduction algorithm [116-118].

3.4 Conclusions

This review of studies on the component loss modelling and electro-thermal analysis reveals that until now, the component-wise electro-thermal analysis has been carried out. Much effort has been applied to studying the individual components in the design, especially switching devices such as the discrete MOSFET, IGBT and diodes etc. Very few studies cover the multichip power module and chip to chip mutual electro-thermal interactions. Some studies have also been found related to the passive component loss model and electro-thermal analysis of the capacitor and inductor for high power converter applications. Approaches have also been outlined to consider the effect of heatsink and thermal interface materials. Moreover, the parameter extraction process in some works is not clearly described and the interaction of electro-thermal model has not been well explained. Component wise electro-thermal analysis has been performed but, the integration of the components in the converter system-level applications and its overall electro-thermal behaviour has been neglected. In addition, no demonstration of the methodology of the concurrent analysis has been presented until now. Thus, the electro-thermal analysis avoiding thermal coupling and non-linearity leads to inaccurate and imperfect results. Neglecting the thermal interaction leads to one to think that experience-based design can improve but this might worsen the design and add higher cooling arrangement and increase the design cost. Thus, the main concern becomes reliability performance for the design engineer. Among the existing models, the compact models and reduced order models show more promise in power dense power electronics system design. FEA is more time-consuming than other methods. However, FEA can also ease the parameter extraction process for the consideration of cross-coupling effect between components. In this work, in order to overcome the limitations of the existing research in the literature (of electro-thermal modelling of power electronic components), a novel modelling methodology have been outlined and demonstrated in applications like the DC-DC boost converter, three-phase voltage source inverter and IPT-based dual interleaved bidirectional boost converter. The methodology incorporates the electrical and thermal model and couples the tight linking between these models. The power loss models have been incorporated with the thermal model. The next chapter will discuss the development of concurrent electro-thermal analysis and implementation of the modelling framework.

Chapter 4 Development of Concurrent Electro-thermal analysis and Implementation

4.1 Introduction

Thermal issues come into the design aspects due to heat generation of the non-ideal components and induce component thermal interaction. In order to tackle this electro-thermal interaction, it is important to understand the electro-thermal behaviour in compact power electronics systems at the early stage of the design cycle. The literature review has revealed that the effect of the component interaction on electro-thermal behaviour has not been investigated in depth for power electronics applications. This chapter will discuss the modelling framework of electro-thermal analysis, including the component loss model, thermal model generation and implementation of the framework in the analysis of the component interaction of the known converter topology applications.

4.2 Components Interaction

In compact power electronics system components are packed closely. Due to their proximity strong electromagnetic interference as well as thermal coupling between components can affect the device performance. To demonstrate the component interaction, an IGBT module [189] containing four devices has been chosen. The purpose of this simulation is to understand the impact of thermal influence of adjacent devices on temperature distribution. To perform this, initially one device is powered up by 50W and the other devices are kept inactive. A similar approach is applied to other devices. Finally, all devices are powered simultaneously to observe mutual thermal coupling. Figure 4.1 shows the temperature distribution in an IGBT module in which only one active device is switched on and it dissipates 50 W of heat. The temperature at the bottom is fixed at the ambient temperature of 20°C. The junction temperature raises to be 117.66° (see Figure 4.1). The junction temperature changes if the location of the active device changes. In fact, the maximum junction temperature is 114.65°, 109.78° and 107.66° respectively when one of the other devices is switched on. When all the devices are switched on, the maximum temperature is raised up to 199.12° (see Figure 4.2).

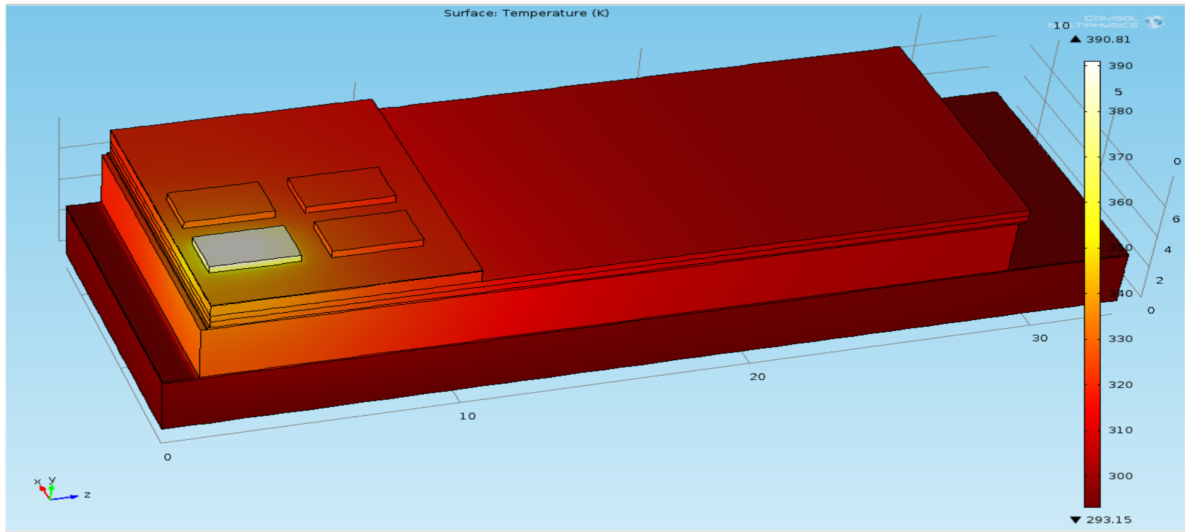


Figure 4.1 First Si-IGBT thermal analysis at 50W power dissipation.

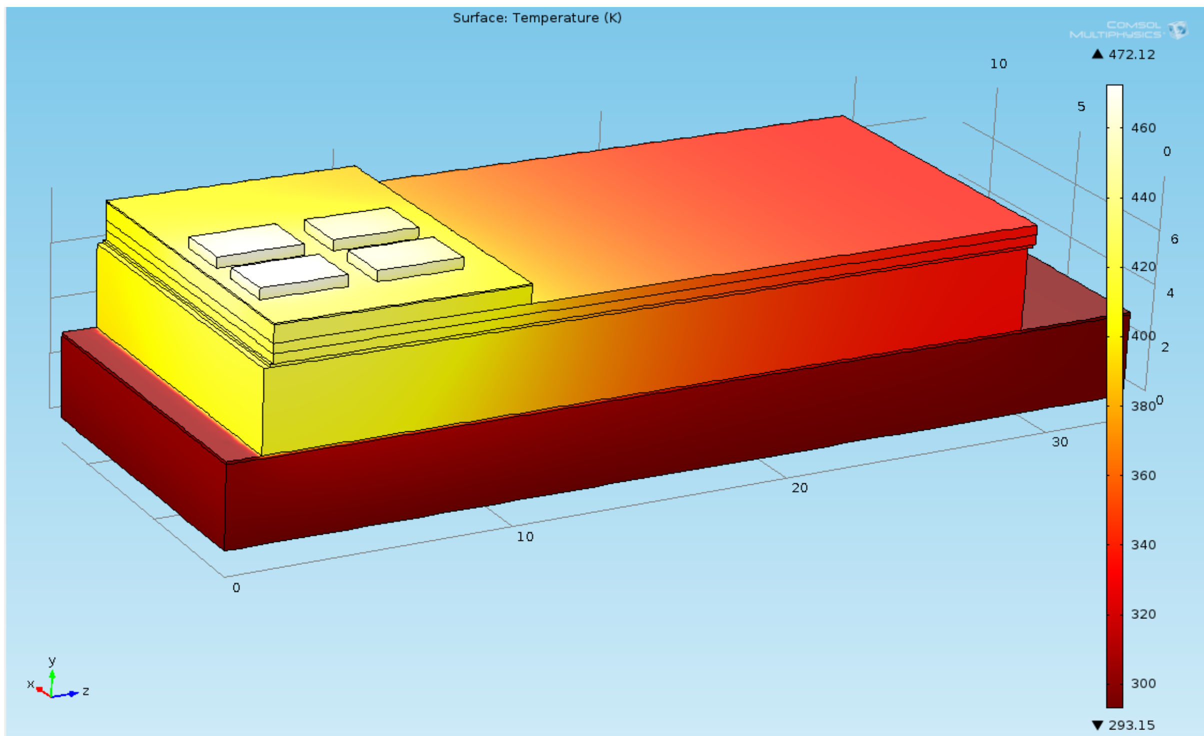


Figure 4.2 All Si-IGBT thermal analysis at 50W power dissipation simultaneously.

These results suggest that for the same power dissipation, the junction temperature is dependent on its location and the components interact with each other thermally.

4.3 Modelling Methodology for Loss Based Concurrent Electro-thermal Analysis

The method that is going to be used in this work is to create a parameterised converter electro-thermal analysis. Initially, a converter topology and its components characteristics

will be defined. A circuit simulator is then used to model the behaviours of the converter topology and from the simulation results, the power losses of all the components will be calculated using loss models that are based on either those obtained from literature or derived in this work. The power losses are then used in compact electro-thermal models to predict the temperatures. As it has been mentioned earlier, it is important to consider component interaction for compact systems and information about the interaction is important for the designer in minimising loss and component selection in the early design stage. By using virtual design methods, the costly trial and error approach can be supplemented. The resulting analysis methodology would permit designers to consider the effects of packaging and therefore, it will be very useful tool for reliable design and development of high power and compact power electronics systems. Figure 4.3 sums up the proposed methodology.

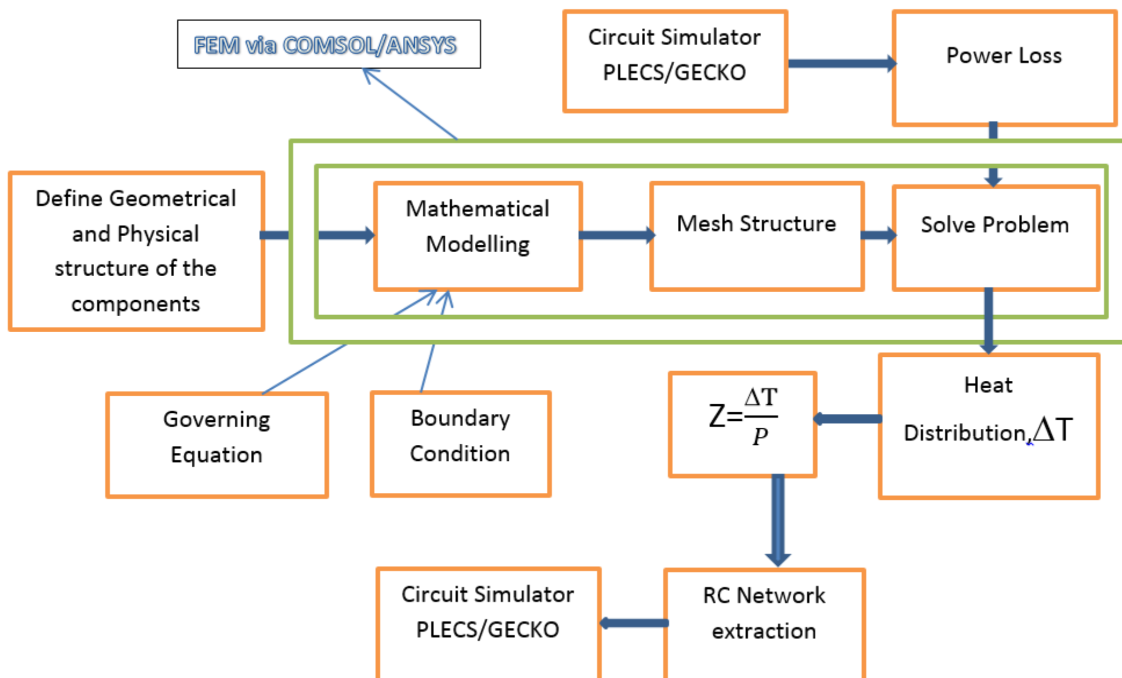


Figure 4.3 Proposed methodology.

The methodology can be divided into two parts. The first part is used for parameter extraction in which the power electronics components and system are characterised. The second part is the circuit simulation which is used for power loss modelling and coupled with the FEA extracted parameterized RC thermal network. As part of the parameter extraction, FEA

analysis can be carried out using COMSOL [165] or ANSYS [156] and circuit simulation can be performed using PLECS [164] or GeckoCircuits [166].

Before proceeding to the detailed study of implementing concurrent electro-thermal analysis the relevant theory of modelling a heat conduction problem needs to be discussed. This chapter will provide the theoretical basis behind the building numerical thermal analysis of power electronic components that are used in a power conversion system in the form of converter applications. It will present the detailed description of heat transfer mechanisms in general and the formulation of heat transfer PDE and the boundary conditions that are applied in solving thermal problems. Also, the electrical-thermal equivalent network has been derived from the transmission line representation of heat transfer theory, the extraction of the RC thermal network in the form of either Foster or Cauer equivalent is discussed and the differences are identified. The theory of extracting thermal network parameters are also discussed in detail including the methodology for heat transfer equations and the different boundary conditions relevant to the thesis.

4.3.1 Basics of Modelling Method

To perform the electro-thermal analysis of a power electronic converter in a circuit simulator, the thermal model parameters are required. In order to extract thermal model parameters, the modelling method is made up of a finite element method. In electro-thermal analysis, the thermal model parameters extraction process, it constructs the fundamental analysis tool prior to make a coupling between the electrical and thermal model. Also, FEA provides the temperature field distributions in the whole converter. Because of the wide application of finite element technique in the simulation results, the following is a detailed discussion of the finite element formulation.

In numerical modelling, the way of solving the heat transfer problem is always three-steps. The first step is the mathematical model formulation of heat transfer. Then, the next procedure is to discretise the governing equations and solve them by an appropriate numerical method. Finally, the achieved solutions are post-processed in order to reach the desired output. Figure 4.4 illustrates the computer based numerical modelling steps.

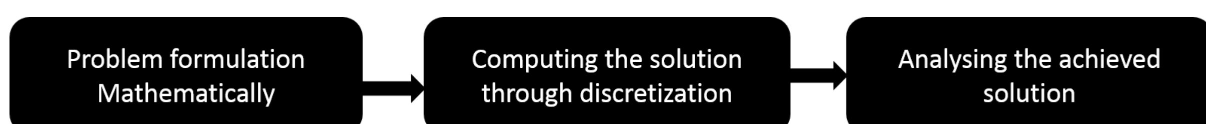


Figure 4.4 Computer modelling- a three stage process.

Thermal energy, in general, refers to the energy exchange between bodies. In this research, components are treated as an almost solid body. Typically, three different modes of heat propagation such as conduction, convection and radiation take place in a system. In solid materials, such as power electronic components, conduction is considered as a dominant mode of heat transfer and other ways such as convection and radiation are assumed as negligible. The conduction heat transfer can be expressed by Fourier's law of heat conduction that the conduction heat transfer rate per unit area is proportional to the normal temperature gradient:

$$Q = -kA\frac{dT}{dx} \quad (4.1)$$

Where, Q is the heat transfer rate, k is the thermal conductivity ($Wm^{-1}K^{-1}$), A is the cross - section area of the heat transfer direction and T is temperature, ($°C$).

The Fourier's law of heat conduction (4.1) can be used to derive basic equations that govern the heat transfer in a solid. For a 1D heat transfer shown in Figure 4.5, the partial differential equation (PDE) shown in equation 4.2 can be derived based on the energy balance that the sum of energy conducted in the left face and the heat generated within the element equals to the sum of the energy conducted out of the right face and the change of internal energy due to temperature change [167].

$$k\frac{\partial^2 T}{\partial x^2} + Q = \rho c_p \frac{\partial T}{\partial t} \quad (4.2)$$

Where, for each material, c_p is the specific heat capacity, ρ is the density, k is the thermal conductivity (it is assumed to be not temperature dependent in our problem), T is the field temperature and Q is the heat generation.

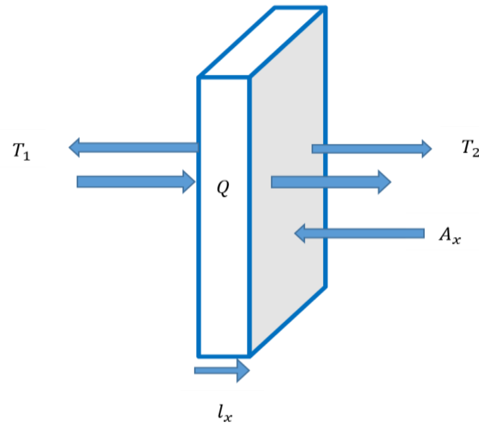


Figure 4.5 One dimensional heat transfer.

The PDE for 3D heat conduction heat transfer is shown in Equation 4.3.

$$k(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}) + Q = \rho c_p \frac{\partial T}{\partial t} \quad (4.3)$$

In essence all numerical thermal analysis methods try to solve Equation 4.3 or give an approximation of this equation with specific boundary conditions.

Convective heat transfer can be modelled as:

$$Q = hA(T_f - T_\infty) \quad (4.4)$$

The Table 3 illustrates typical values of average heat transfer coefficients encountered in engineering design:

Table 3 Heat transfer coefficient of various flow types [168]

Flow Type	$h, (Wm^{-2}K^{-1})$
Forced convection; low speed flow of air over a surface	10
Forced convection; moderate speed flow of air over a surface	100
Forced convection; moderate flow of water in a pipe	3000
Forced convection; boiling water in a pipe	50,000
Forced convection; vertical plane in air with 30°C temperature difference	5

The most widely used thermal modelling method is an RC type (resistor-capacitor) compact thermal network model. It is more accurate and computationally fast to solve and easy to integrate into circuit simulators. In addition, it can help estimate the instantaneous junction temperature in long-term load profile dynamic simulations [102], [105]. Electro-thermal analogies are shown in Table 4. The detailed derivation of heat transfer PDE and classification of RC network is described in Appendix C.

Table 4 Electrical-thermal Analogies

	Thermal	Electrical
Through Variable	Heat Transfer rate, Q, watts	Current, I ,amps
Across Variable	Temperature, $T, K\ or\ °C$	Voltage, V, volts
Dissipation Element	Thermal resistance, R_{th}, $°C/W$	Electrical Resistance, R, ohms
Storage Element	Thermal capacitance, C_{th} , $J/°C$	Electrical Capacitance, C, farads

4.3.2 Analytical Loss Characterisations of Boost Converter Topology

To carry out the electro-thermal analysis for a given topology, power losses occurring in the constituent components need to be estimated. In the power converter design, power losses of the components are important design parameters because they determine efficiency of the power converter circuits and cooling systems of the power devices. Therefore, a method is needed to estimate the power losses of the components accurately for the efficient design of the power converter circuit. In order to design a power electronics system, (e.g. designing a power converter) the electrical and thermal parameter related to the design specifications of the given topology need to be extracted. The power converter specifications can be its voltage, power ratings, efficiency, switching frequency, power density, thermal limit and modulation scheme for generating gate pulse to activate the device. Then for determining the efficiency of converter loss modelling is required. Thus, loss modelling for active and passive components is required to represent the various loss mechanisms that occur in the components while the converter could be in operation. From the loss calculation, thermal management can be achieved. From the prediction of the losses, the required heatsink and appropriate cooling system can be designed. For the improvement of overall power density,

the effect of increasing switching frequency can be analysed through overall loss prediction from the converter. Then the power density and weight of the converter can be evaluated. Figure 4.6 describes the generalised integrated electro-thermal analysis approach of power electronics system design.

A 5 kW 250-500V boost DC/DC converter is considered as a power converter topology and it constructs an electrical network for stepping voltage from one level to another. The key components are Infineon IGBT IGW50N60H3 (package TO-246) and the ultra-fast power diode BYV29B-500 in the converter. Both IGBT and diode share the same heatsink. The heat spreading inside the two components leads to mutual cross-coupling between thermal paths. Modelling this thermal interaction between IGBT and diode is of interest to study. The converter configuration and package information are depicted in Figure 4.7. The electrical parameters of the converter are listed in Table 5. An accurate power loss model can enable the converter designers to perform first calculations and to compare between different semiconductors. In addition, it can help to select the required heatsink accurately for thermal management.

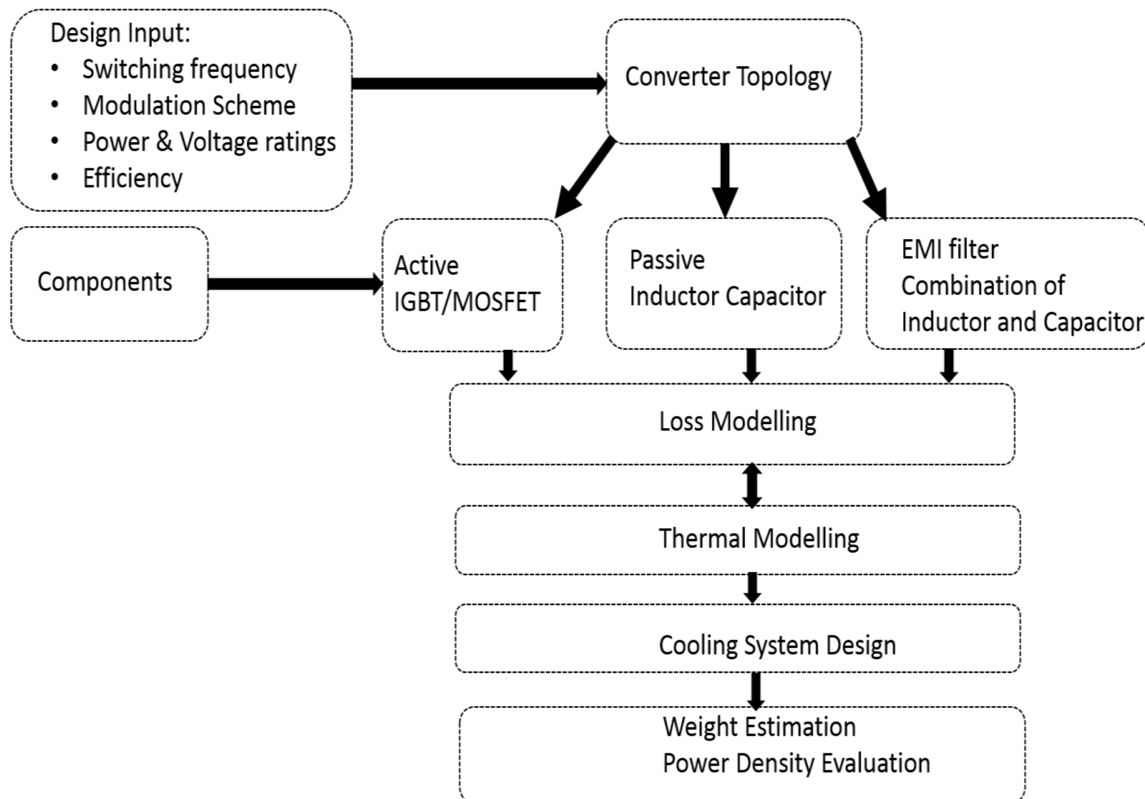


Figure 4.6 Integrated Electro-thermal Analysis of Power Electronics System Design.

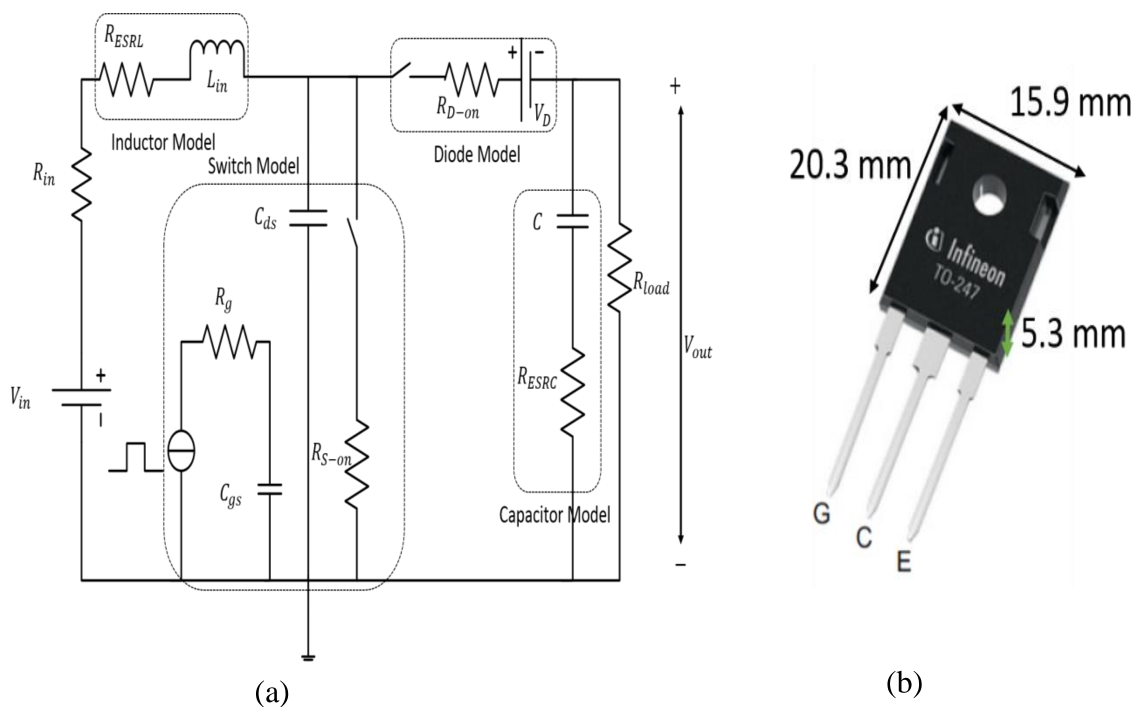


Figure 4.7 (a) Equivalent circuit of boost converter topology with parasitic elements (b) IGBT package [169].

Table 5 Converter electrical parameters

Duty ratio, D	0.5
Load current, I_{load}	10A
Ripple voltage, V_{ripple}	1% of output voltage
Ripple current, I_{ripple}	30% of load current
Input Current, I_{in}	19.6A

4.3.3 Loss Modelling

Energy losses in the power semiconductor devices of a converter topology can be divided into conduction losses and switching losses. Conduction losses are directly dependent on loads. An example of conduction losses in MOSFET/IGBT can be described as the multiplication of on-state MOSFET/IGBT resistance by on-state current. Conduction losses for the IGBT can be calculated, with the widely used approximation between on-state current and on-state voltage given in Figure 4.8.

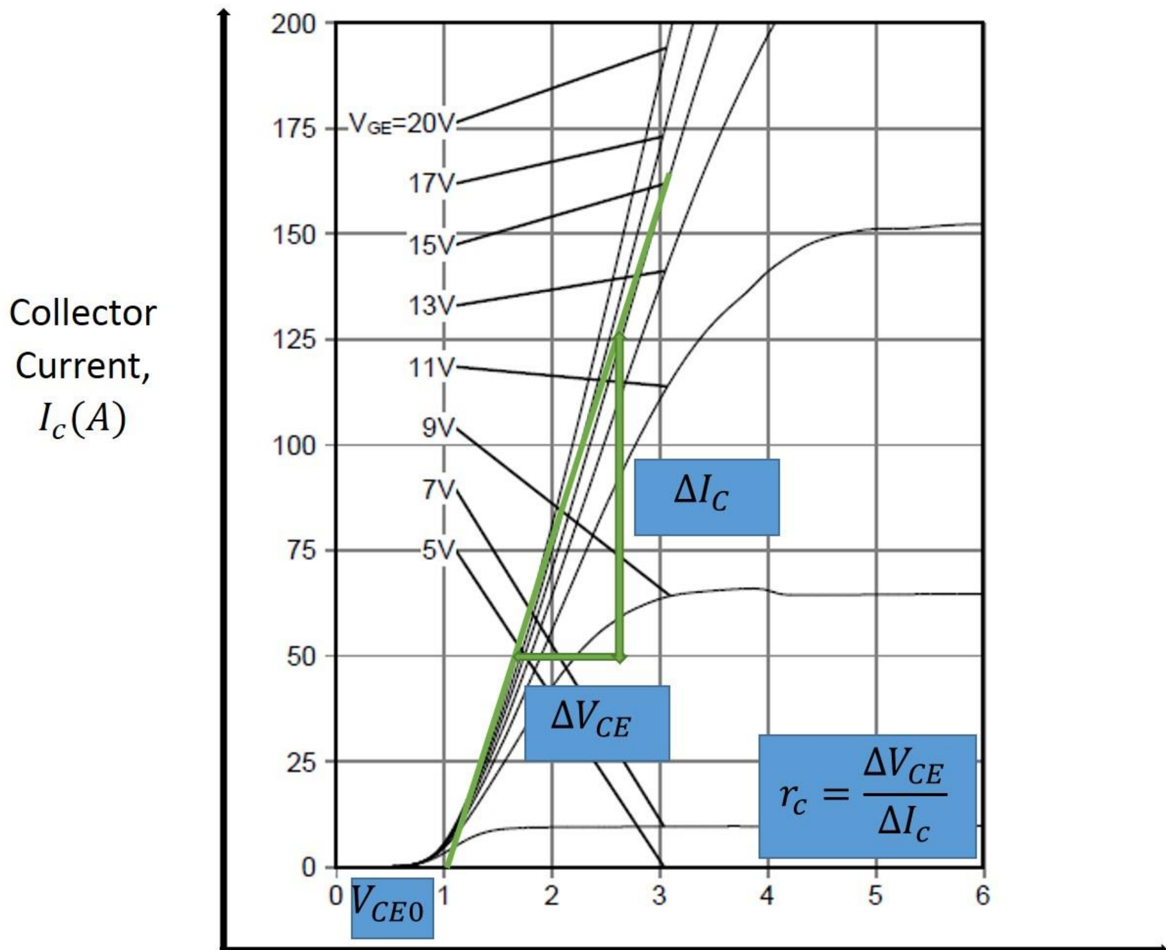


Figure 4.8 IGW50N60H3 IGBT- V_{CE} vs. I_C curves at 25°C [169].

Threshold voltage and on-resistance of IGBT/MOSFET are temperature dependent. On resistance can be calculated from the slope of the tangent line drawn on $V_{GE} = 15V$. After determining the on-resistance, conduction losses can be estimated using the formula as described in section 3.1.2.

The total switching losses in one switching cycle can be considered as the sum of the energy during turn-on and during turn-off processes. Manufacturers usually provide data of IGBT switching frequency energy as a function of forward current and gate resistor under various operating temperatures. The switching losses can also be calculated using the formula as described in section 3.1.2.

Losses also occur in the power diode due to its on-resistance. It can also be estimated by using the formula described in section 3.1.2. On resistance can be calculated from the slope of the tangent line drawn on $V_{GE} = 15V$ as shown in Figure 4.9.

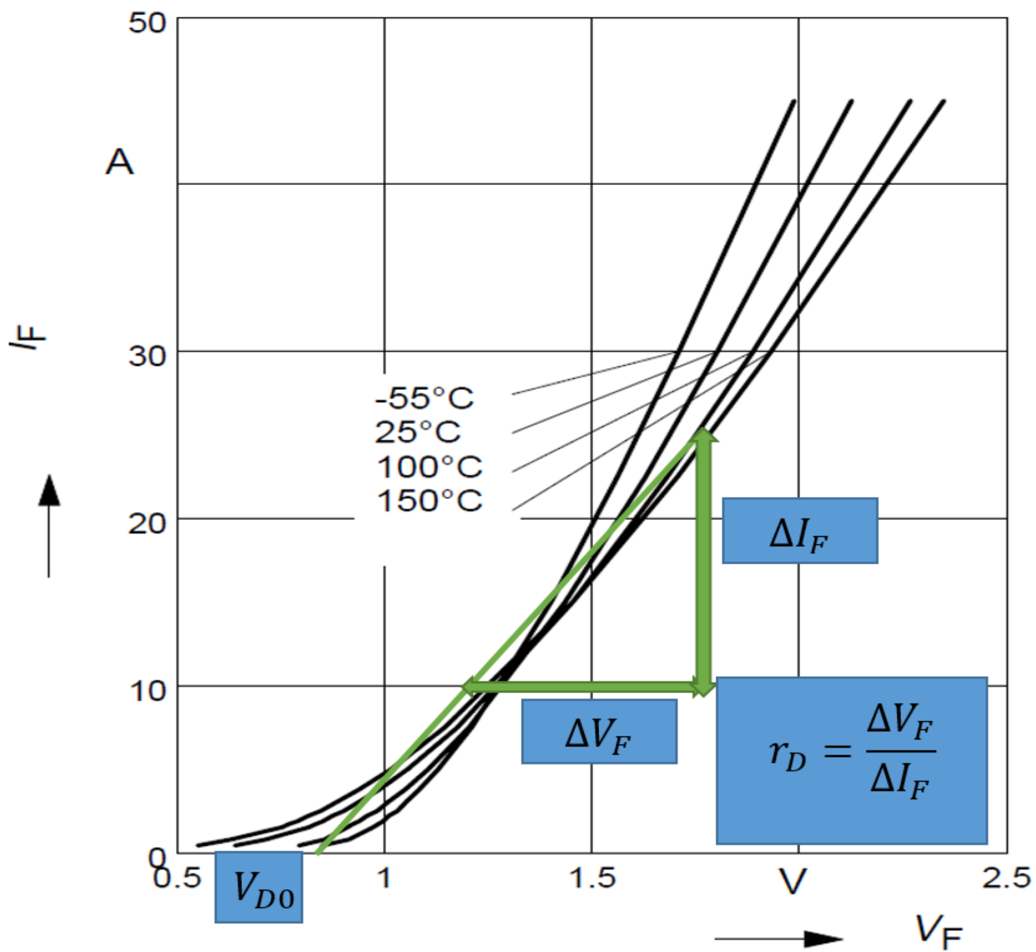


Figure 4.9 Forward current as a function of forward voltage [170].

When the power losses of the IGBT and diode are known, then the heatsink can be designed. The heatsink design process is articulated in Appendix D.

4.3.3 Electrical Circuit Simulation of Loss Analysis

The DC-DC boost converter studied in this work contains one IGBT, one diode, one inductor and one output capacitor. Losses occur in both active and passive components due to various loss mechanisms. To model the losses in those components, component models must be built using the electrical properties obtained from the manufacturer datasheet. For example, to perform the analysis of losses of both IGBT and diode, the components should take into account device parameters related to power losses.

To account for the temperature effect on on-resistance, on-resistance of the IGW50N60H3 IGBT is calculated from the manufacturer provided IGBT characteristics curve at 25°C and 175°C respectively. Figure 4.8 and 4.10 respectively illustrate the characteristics at two different temperatures given in the datasheet. For a proper linearisation, the maximum operating current should be considered. The on-resistance formula is expressed in Equation 4.5. In this example, using Equation 4.5 the values extracted from the IGBT characteristics curve are given in Table 6 and 7 respectively. Table 8 shows the temperature dependent on-resistance. Figure 4.11 shows the temperature dependency of on-resistance and the relationship between on-resistance and junction temperature is expressed in Equation 4.6.

$$r_c = \frac{\Delta V_{CE}}{\Delta I_c} \qquad (4.5)$$

The same procedure is applied to the diode conduction loss modelling.

Table 6 IGBT characteristics value at 25°C

V_{CE}	I_c
1.6	50
2.7	125

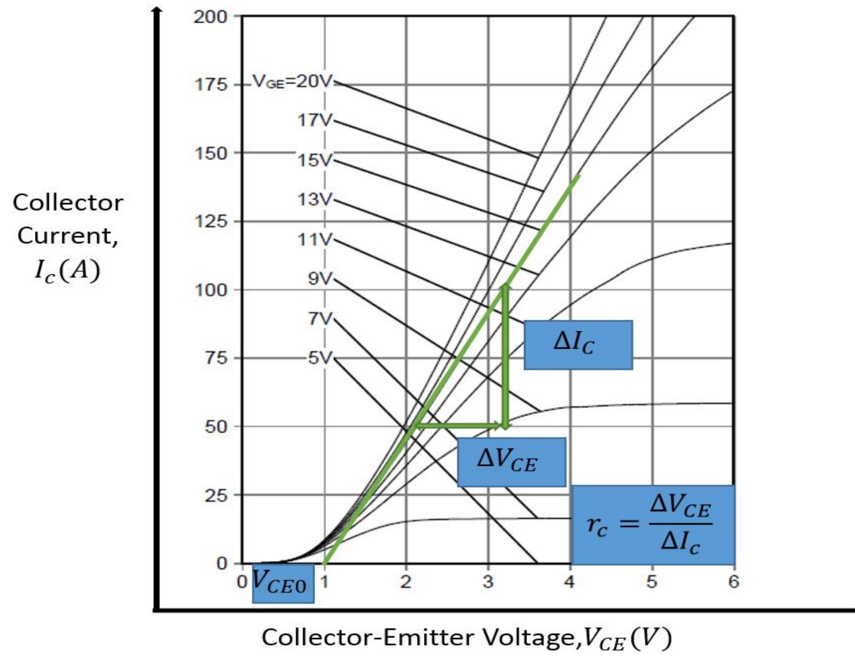


Figure 4.10 IGW50N60H3 IGBT- V_{CE} vs. I_C curves at 175°C [169].

Table 7 IGBT characteristics value at 175°C

V_{CE}	I_c
2.1	50
3.2	100

Table 8 Temperature dependency of on-resistance of IGBT

Temperature	R_{dson}
25	14.7 $m\boldsymbol{\Omega}$
175	22 $m\boldsymbol{\Omega}$

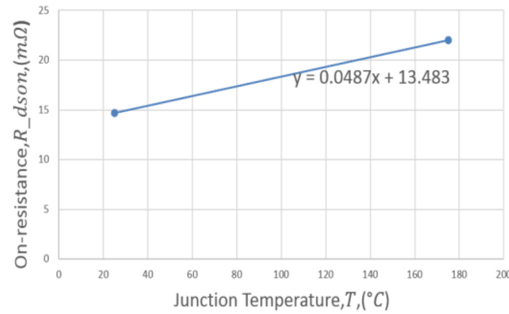


Figure 4.11 On-resistance as a function of junction temperature.

Curve-fitted expression can be written as

$y = 0.0487x + 13.483$ .... (4.6)

y can be represented as $R_{dson}(T_j)$ and x can be represented as junction temperature T_j

Equation 4.6 can be rewritten as

$R_{dson}(T_j) = 0.0487 * T_j + 13.483$ .... (4.7)

In this thesis, circuit analysis software PLECS is used to model the losses in IGBT and diode. The model parameters for the circuit analysis are listed in Table 9. In PLECS, a thermal description of the components can be represented by the loss characteristics such as conduction losses, switching losses and thermal impedance. The way by which the thermal representation is carried out is shown in Figure 4.12. This thermal representation allows the detailed modelling analysis. If the assigned thermal description does not satisfy the thermal design constraints for example exceeding the junction temperature of Si devices greater than 125°C, a new component can be characterised by editing the thermal description library.

Table 9 Model parameters for circuit analysis

Linearised conduction losses	Value
IGBT threshold voltage,V_{cesat}	V
IGBT conduction slope,R_{dson}	$m\boldsymbol{\Omega}$
Diode threshold voltage,V_{cesat}	V
Diode conduction slope,R_{dson}	$m\boldsymbol{\Omega}$

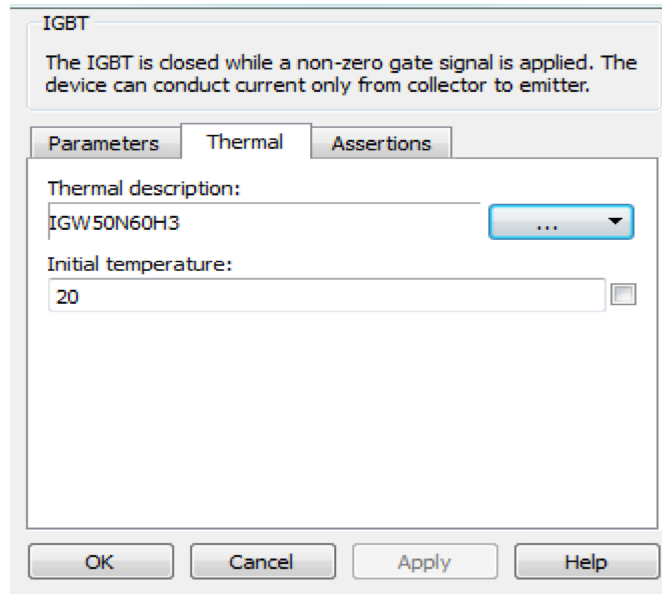


Figure 4.12 Thermal description editor for IGBT.

To represent the temperature dependent conduction loss characteristics, manufacturer-provided curves (I_C vs V_{CE}) at both 25°C and 175°C (as shown in Figure 4.8 & Figure 4.10) are used to construct the thermal loss map with the help of a 2-D look-up table. PLECS can be used to estimate the exact collector-emitter voltage by performing the linear interpolation from these values in a look-up table. For example, the temperature dependent I-V characteristics for the IGW50N60H3 can be represented by the curves that are shown in Figure 4.13.

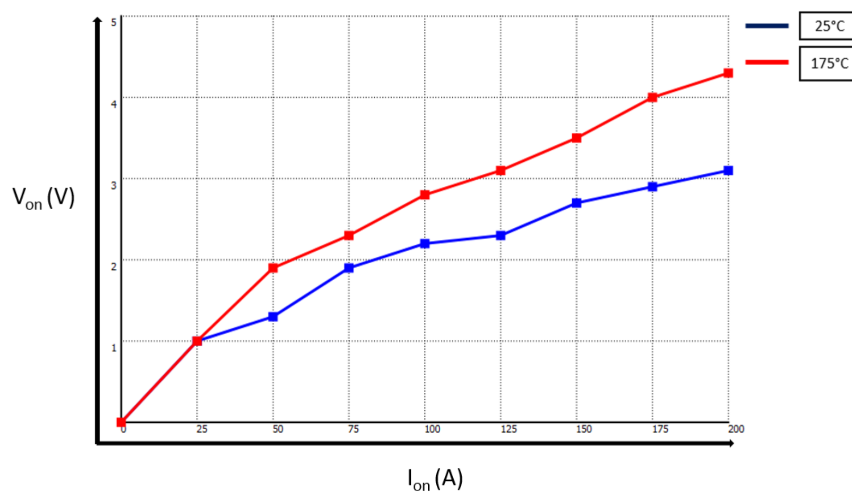


Figure 4.13 Temperature dependent I-V characteristics of IGW50N60H3 IGBT.

From the knowledge of thermal dynamics, the thermal time constant is quite large. It is in the range of seconds compared to the electrical transients. To capture the switching phenomena which are in the range of few hundred microseconds, a circuit simulator will have to maintain a time step much smaller than the switching time. Then, simulation speed would result in slowness generated due to the huge computational load and increased memory for operations of several tens of seconds. In order to eliminate the problems of long time simulation for the calculation of power losses, time-dependent power losses have been averaged [171]. Figure 4.14 describes the average loss calculation approach of IGBT in PLECS. A periodic average block is suited to perform the average conduction loss while periodic impulse average block is suited to perform average switching loss. Similarly, the average diode loss calculation is shown in Figure 4.15. The analysis approach including periodic average and periodic impulse average techniques have been described in Figure 4.16. Total switching time is considered as the averaging time for both the cases.

For example, the average smoothing power losses for IGBT conduction, is calculated by using Equation 4.8.

$$P_{conduction\ losses-IGBT}(t_s) = \frac{1}{t_s}\int_t^{t+t_s} P_{conduction\ losses-IGBT}(t)dt \quad (4.8)$$

where, t_s is the switching period. The generic blocks in the PLECS can enable the model to calculate the average conduction loss and switching loss.

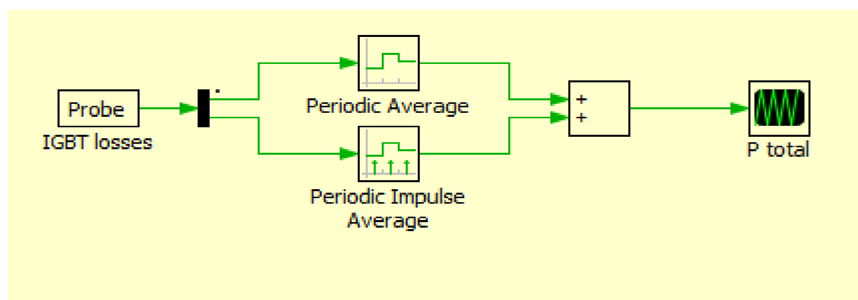


Figure 4.14 Average loss calculation scheme of IGBT in PLECS.

Similarly, the average smoothing power for switching losses can be calculated by using Equation 4.9.

$$P_{Switching\ losses-IGBT}(t_s) = \frac{1}{t_s}\int_t^{t+t_s} P_{Switching\ losses-IGBT}(t)dt \quad (4.9)$$

The average smoothing power for the diode can also be calculated by using Equation 4.10.

$$P_{conduction\ losses-Diode}(t_s) = \frac{1}{t_s}\int_t^{t+t_s} P_{conduction\ losses-Diode}(t)dt \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4.10)$$

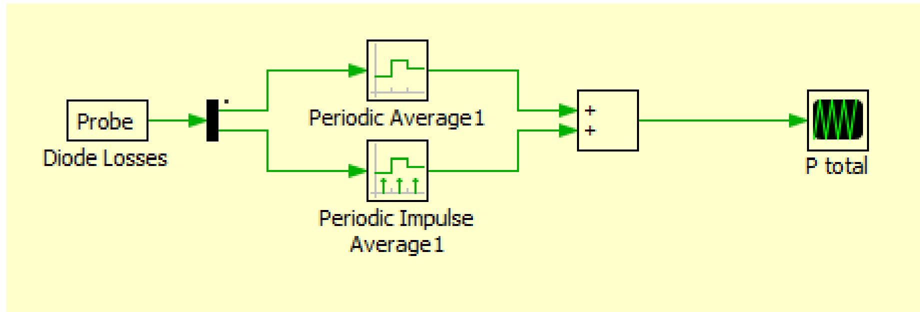
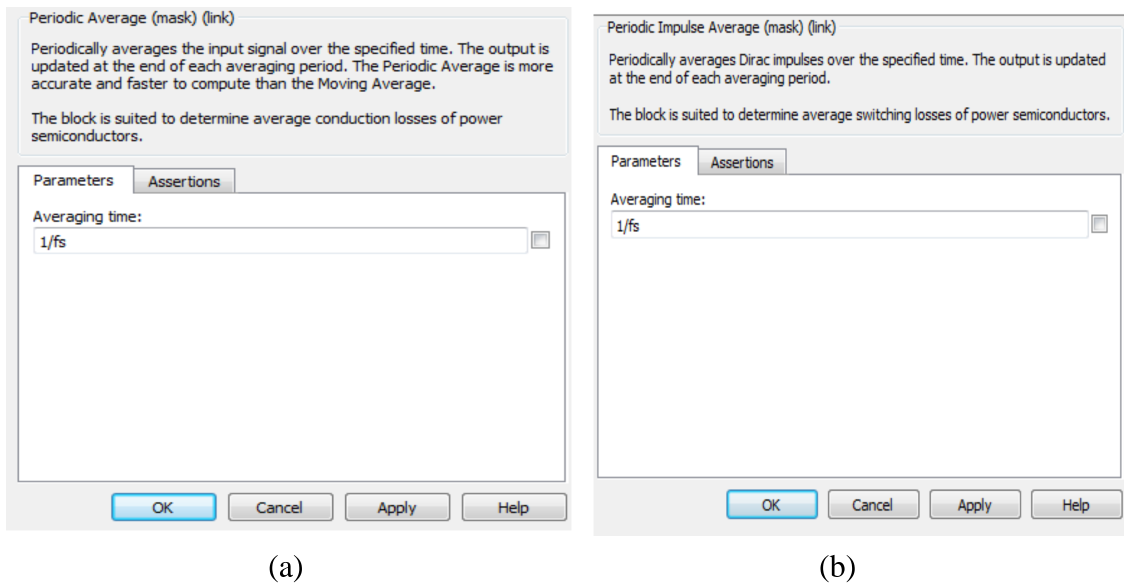


Figure 4.15 Average loss calculation scheme of diode in PLECS.

To determine the average conduction losses, the periodic average block is used. The averaging period is set as the period of one switching cycle. Similiarly, a periodic impulse average block can also be used for calculating the average switching losses.

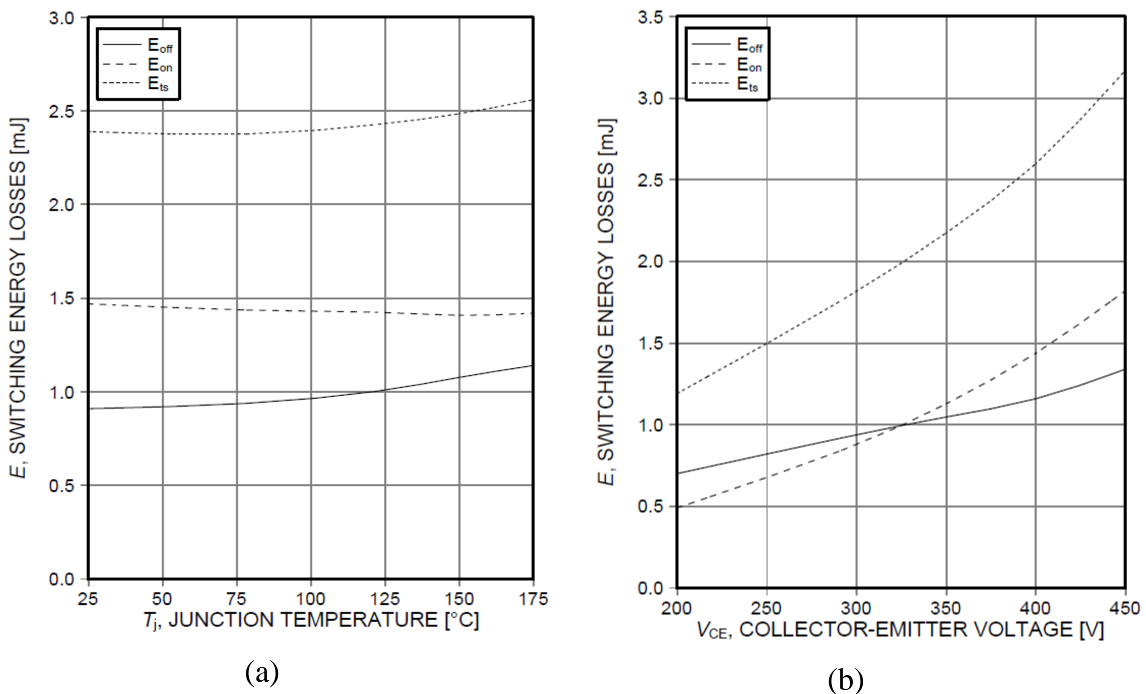


(a) (b)

Figure 4.16 Periodic Impulse Average loss calculation scheme (a) conduction losses (b) switching losses.

Switching losses can be modelled in PLECS by creating a 3D look-up table that combines blocking voltage, current and temperature. The 3-D look-up table enables the calculation of losses due to instantaneous turn-on and turn-off energy. As it has been assumed that the IGBT is in service within the voltage parameter of 175°C, the manufacturer provided turn-on

and turn-off energy data sheet at 175°C has been used to construct a 3D thermal map. In the datasheet the turn-on and turn-off energy is derived under the experimental conditions of the base-collector emitter voltage of 400V. To model more accurately, the data up to 600V is added and the energy loss is considered to be linearly increasing with the escalated voltage. Switching turn-on and turn-off energy loss as a function of junction temperature and collector-emitter voltage has been shown in Figure 4.17. According to the datasheet, the turn-on energy at 25°C and 175°C is 1.45 mJ and 1.42 mJ respectively. Turn -off energy at 25°C and 175°C is 0.91 mJ and 1.13 mJ respectively. To model the switching energy losses at higher collector-emitter voltage, the mathematical relationship between switching energy and collector current is expressed as Equation 4.11 and Equation 4.12 respectively.



(a) (b)

Figure 4.17 Switching energy losses as a function of (a) junction temperature (b) collector-emitter voltage.

$$E_{on} = \frac{E_{on-ref} * I_{op}}{I_{ref}} * \frac{V_{op}}{V_{ref}} \quad (4.11)$$

$$E_{off} = \frac{E_{off-ref} * I_{op}}{I_{ref}} * \frac{V_{op}}{V_{ref}} \quad (4.12)$$

where, I_{op} is the operating current, V_{op} is the operating voltage, I_{ref} is the reference current, V_{ref} is the reference voltage, E_{on-ref} is the reference turn-on energy and $E_{off-ref}$ is the reference turn-off energy.

Using Equation 4.11 and Equation 4.12 respectively, IGBT turn-on and turn-off energy is calculated for the two temperatures 25°C and 175°C. The data related to both turn-on energy and turn-off energy is stored in Table 10-13. To create the temperature dependent loss map, a 3D look –up table is built including temperature dependent loss data. The data listed in Table 10 and Table 11 respectively is used to create a loss map due to turn-on energy. Similarly, data listed in Table 12 and Table 13 is used to create a loss map due to turn-off energy. To implement temperature dependent loss due to turn-on and turn-off energy, the look-up table is set as shown in Figure 4.18(a) and Figure 4.18(b) respectively.

Table 10 Turn-on Energy calculation of IGBT at 25°C

$Temperature, T = 25°C$						
$Voltage, V (Volts)$	$Current, I (A)$					
	0	5	8	10	15	20
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	0 mJ	0.1812 mJ	0.29 mJ	0.3625 mJ	0.5437 mJ	0.725 mJ
600 V	0 mJ	0.2175 mJ	0.348 mJ	0.435 mJ	0.6525 mJ	0.87 mJ

Table 11 Turn-on Energy calculation of IGBT at 175°C

$Temperature, T = 175°C$						
$Voltage, V (Volts)$	$Current, I (A)$					
	0	5	8	10	15	20
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	0 mJ	0.1775 mJ	0.284 mJ	0.355 mJ	0.5325 mJ	0.71 mJ
600 V	0 mJ	0.213 mJ	0.3408 mJ	0.426 mJ	0.639 mJ	0.852 mJ

Table 12 Turn-off Energy calculation of IGBT at 25°C

$Temperature, T = 25°C$						
$Voltage, V(Volts)$	$Current, I(A)$					
	0	5	8	10	15	20
$0\ V$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$
$500\ V$	$0\ mJ$	$0.1138\ mJ$	$0.182\ mJ$	$0.2275\ mJ$	$0.3413\ mJ$	$0.455\ mJ$
$600\ V$	$0\ mJ$	$0.1365\ mJ$	$0.2184\ mJ$	$0.273\ mJ$	$0.4095\ mJ$	$0.546\ mJ$

Table 13 Turn-off Energy calculation of IGBT at 175°C

$Temperature, T = 25°C$						
$Voltage, V(Volts)$	$Current, I(A)$					
	0	5	8	10	15	20
$0\ V$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$	$0\ mJ$
$500\ V$	$0\ mJ$	$0.1412\ mJ$	$0.226\ mJ$	$0.2825\ mJ$	$0.4238\ mJ$	$0.565\ mJ$
$600\ V$	$0\ mJ$	$0.1695\ mJ$	$0.2712\ mJ$	$0.339\ mJ$	$0.5085\ mJ$	$0.678\ mJ$

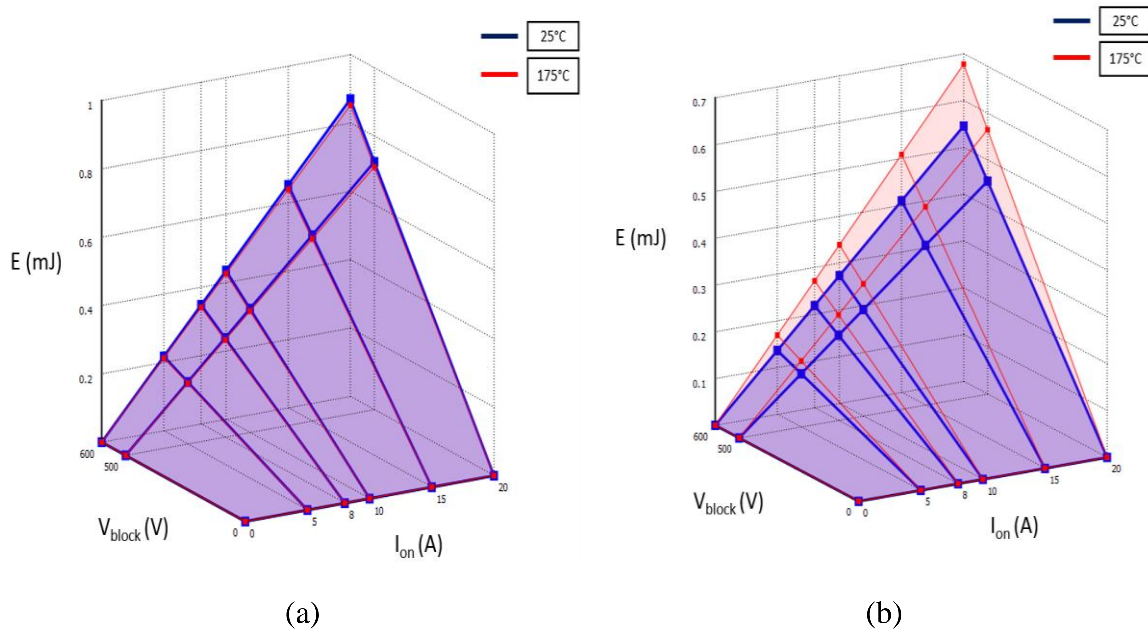


Figure 4.18 (a) Turn-on Energy and (b) Turn-off Energy of IGW50N60H3 IGBT.

Similarly, the diode conduction loss can be modelled by diode I-V characteristics curve as shown in Figure 4.19. Diode turn-on and turn-off energy is not considered in the analysis as the diode turn-on losses and turn-off losses are negligible.

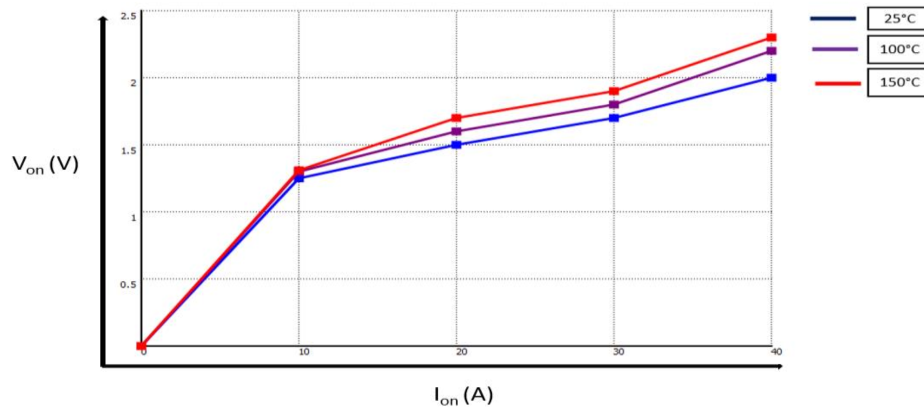


Figure 4.19 Temperature dependent I-V characteristics of IDB15E60 DIODE.

4.3.4 Inductive Component Loss Model

Since the converter contains magnetic components, it is required to estimate the losses in the inductor as part of system losses. To model the losses in PLECS, the inductive component is represented with two resistors. An AC resistance is included in the electrical inductance model to represent Joule heating losses due to a ripple current and DC resistance is also used to represent DC winding losses. These losses are summed up and treated as winding losses. To estimate the temperatures, these winding losses are applied to the thermal network of the inductor. To make the model simple, core loss has been considered fixed although the core characteristics changes with the operating temperatures. In the model, the calculation process of core losses is simplified due to the difficulty in finding the experimental data of the core at different temperatures. To consider the effect of temperature in the core, the temperature dependent core model must to be included. To generate a temperature dependent core model, practical experimental set up is required. Furthermore, it is not our focus to derive the temperature dependent core characteristics experimentally as our work is mostly confined to computer modelling. Therefore, the temperature dependent core loss modelling has been ignored. However, some works could describe the core loss modelling. The losses due to DC current in the form of DC winding losses have been modelled with the DC resistor. As the winding temperature changes the winding material say for copper resistance, the winding losses gets increased. To couple the inductor electrical and thermal model the winding

temperature is feed back into the corresponding winding loss model of the inductive components at system level.

Winding losses in inductors can be modelled with the temperature dependent properties. Temperature dependent resistance variation is realised with variable resistance inductance model in this work. The resistance varies accordingly with the operating temperature [172]. The winding resistance can be expressed as:

$$R_{winding} = R_{T_{ref}} * (1 + \alpha(T_w - T_{ref})) \quad \text{.....} (4.13)$$

Where, $R_{winding}$ is the electrical resistance of winding, $R_{T_{ref}}$ is the electrical resistance of winding at reference temperature, T_w is the winding temperature and T_{ref} is the reference temperature respectively.

The temperature dependent inductor loss model is linked to both the electrical model and thermal model. The electrical current in the winding of inductance generates the winding losses and these losses are applied to the inductor-lumped thermal model. The thermal model can be built based on the obtained parameters either those from analytically or FEA-based analysis.

4.3.5 Capacitive Component Loss Model

Capacitors are treated as the essential energy storage components in power dense converters. In power converters, capacitors are also used for filtering. During the long-load cyclic operation of the converters capacitors experience failures due to electro-chemical ageing, vaporisation and loss through the seal. In compact converters, the elevated temperature rise outperforms the widespread use of capacitors due to low costs and high capacitance per volume. Capacitor lifetime is heavily influenced by the operating temperature. Increasing ripple current generates the higher ESR loss and thus generates higher core temperature and thereby triggers the failure. The physics-based loss model can better explain the ESR loss mechanism. The use of physics-based capacitor model is limited in modelling because of the difficulty to integrate it into a circuit simulator. The published literature points that physics - based models to date have not been applied in power electronics applications. Although these models are accurate but require high computational costs. However, in practical applications, the physics-based models have not been studied in the power electronics area.

Capacitor temperature rise is crucial for the reliability performance of power electronics operation. With the increasing ripple current excessive pressure on the reliability of the

capacitor has become a matter of serious investigation. The capacitor has been modelled with ESR of the capacitor. The dielectric losses can be predicted from the capacitor electrical model. The electrical model is then coupled to the thermal model. The temperature-dependent ESR model is coupled to the capacitor core temperature. Thus, the generated temperature changes the electrical properties of the capacitor. These get changed into increasing losses and these losses are further taken into capacitor thermal model.

ESR is also frequency dependent. Dielectric losses are the prime source of heating up the capacitor that raises the core temperature. This heat conducts between the capacitor winding layers. From the winding layers heat conducts to the can and from the can it radiates outside the environment. Dielectric losses can be modelled with the temperature dependent equivalent series resistance of the capacitor [173] . The temperature-dependent ESR can be expressed as:

$$ESR_{(T)} = ESR_{T_{ref}} * 2^{[-\frac{(T_{op}-T_{ref})}{A}]^{B}} \quad (4.14)$$

where, $ESR_{(T)}$ is the equivalent series resistance in the capacitor at operating temperature, $ESR_{T_{ref}}$ is the equivalent series resistance in the capacitor at reference temperature, T_{op} is the operating temperature, T_{ref} is the reference temperature, A and B are constants.

The temperature dependent capacitor electrical model has been simulated with the thermal model. Figure 4.20 illustrates the capacitor model representation and the ESR losses are considered as the heat source and the circuit-based thermal network can be derived from the lumped approach.

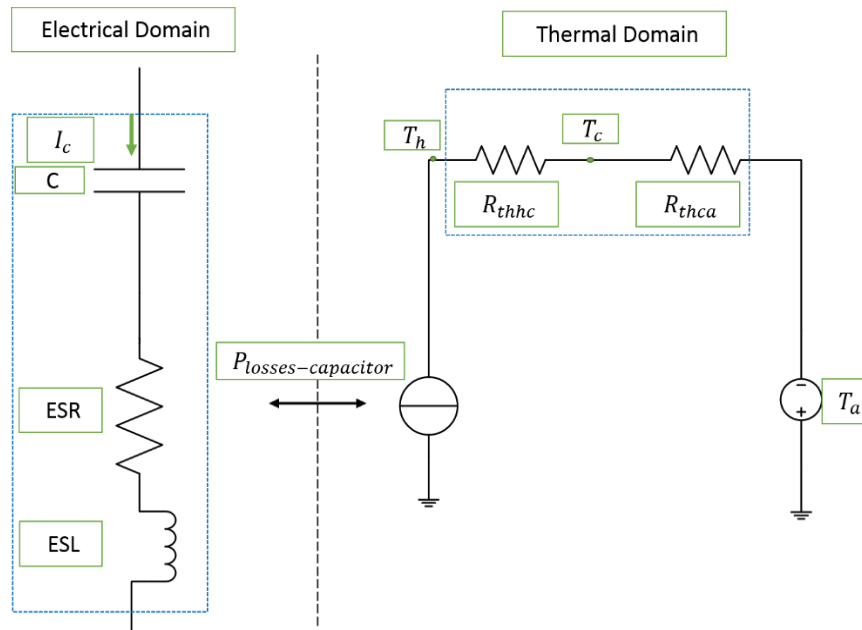


Figure 4.20 Capacitor electrical-thermal equivalent circuit model.

4.4 Magnetic Component Thermal Design

Magnetic components are getting increasingly important in making more compact power electronics products. The dimensions of an inductor depend on many design parameters such as flux swing, magnetic material saturation, DC-bias, switching frequency and cooling method etc. Therefore, to design a magnetic component, the peak-to-peak inductor ripple currents and the peak fluxes must be considered. Accordingly, magnetic components are designed to satisfy the requirement for peak-to-peak inductor ripple currents during a stable operation without causing any magnetic saturation.

An algorithm has been developed to design the inductor in terms of electrical and thermal parameters. The algorithm calculates the electrical properties of the inductor and predicts the temperature rise in both core and windings which can be used later in deriving an analytical lumped thermal model.

In this work, the inductors that are used in DC-DC boost converters are analysed. These inductors are assumed to be made from round/foil/Litz wire windings.

To accomplish the design target, the following parameters are calculated by using the proposed algorithm:

- Peak flux density
- Turn number in the windings

- DC resistance of the winding
- AC resistance of the winding including skin and proximity effect
- Resistance factor
- Power losses due to DC current flow through the winding
- Power losses due to AC ripple current flow through the winding
- Gap loss in the core
- Core losses
- Winding power losses
- Core losses due to hysteresis and eddy effect
- Winding temperature rise with respect to ambient
- Core temperature rise with respect to ambient

At the beginning of the algorithm typical converter parameters are declared: input voltage V_{in}, output voltage V_o, maximum converter output power capability P_0, converter efficiency η, ripple current ratio r and operating/switching frequency f_s. By using Equations (4.15-4.21), the electrical parameters are generated such as dc input current I_{in}, peak to peak inductor current ΔI_{ripple}, duty ratio D, inductor inductance L, and inductor peak current I_{Lmax} etc.

Input Current can be expressed as:

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{P_0}{\eta V_{in}} \qquad (4.15)$$

Duty cycle in the continuous conduction mode can be expressed as:

$$D = 1 - \frac{V_{in}}{V_o} \qquad (4.16)$$

Input Current ripple can be expressed as:

$$\Delta I_{ripple} = I_{in}.r \qquad (4.17)$$

Inductance can be expressed as:

$$L = \frac{D.V_{in}}{f_s.\Delta I_{ripple}} \qquad (4.18)$$

The rms (root-mean-square) current for CCM operation can be written as

$$I_{crms} = \sqrt{\frac{D(I_{Lmax}{}^2+I_{Lmax}*I_{Lmin}+I_{Lmin}{}^2}{3}} \qquad (4.19)$$

$$I_{Lmax} = I_{in} + \frac{\Delta Iripple}{2} \qquad (4.20)$$

$$I_{Lmin} = I_{in} - \frac{\Delta Iripple}{2} \qquad (4.21)$$

The magnetic flux density for the core (B), the current density (J) and the copper fill factor (K) etc. are defined in order to calculate the turn numbers. Also inside the program, the relative magnetic permittivity μ_r values are defined.

The number of winding turns can be calculated by using Equation 4.22, which is based on the constraint that the peak flux density in a core should not exceed a predefined maximum value B_{max}.

$$N = \frac{L*I_{in}}{B.A_e} \qquad (4.22)$$

The dimensions of an inductor core are described by these parameters: the core limb width (a), the window width (b), the window length (c), the core thickness (d), the core width (e) and the core height (f). From these parameters, the window space can be calculated for a given winding turn number.

The one turn winding cross-section area can be calculated as follows:

$$A_{w1} = \frac{I_{in}}{J} \qquad (4.23)$$

The total winding area $A_{winding}$ can be obtained by multiplying the number of turns that are required to generate the desired inductance.

$$A_{winding} = N.A_{w1} \qquad (4.24)$$

Equation 4.25 is the condition that has to be met if the winding can fit into the available core window area

$$A_{winding} < A_e \qquad (4.25)$$

The maximum permissible temperature has been set as the operating temperature in the winding. The DC resistance of the winding has been calculated using Equation 4.26.

$$R = \rho \frac{l_w}{A_{winding}} \qquad (4.26)$$

where, ρ is the resistivity of the conductor material, l_w is the length of the wire and $A_{winding}$ is the wire bare area.

The length of the wire comprising an n-turn winding can be expressed as

$$l_w = n(MLT) \qquad (4.27)$$

where, MLT is the mean-length-per-turn of the winding. The mean-length-per-turn can be expressed as a function of the core geometry.

$$R = \rho \frac{n(MLT)}{A_{winding}} \qquad (4.28)$$

Winding losses are common in magnetic components due to Joule heating. These losses are temperature dependent and conductor spacing in winding configuration also cause proximity effect and thereby adds losses to it. Particularly in high frequency, AC loss effect is also dominant. AC loss effect can be expressed as the ratio of AC to DC resistance.

The widely used formula for calculating the DC winding resistance is presented in Equation 4.29 [174].

$$R_{dc} = \frac{\rho l_w}{A_{winding}} (1 + \alpha(T_{op} - T_0)) \qquad (4.29)$$

where, l , A , α , T_{op}, T_0 are the electrical conductivity, mean path length, cross-sectional area, temperature coefficient resistance, operating temperature and reference temperature respectively

For the temperature dependent power loss calculation in the windings, the input parameter is the temperature-dependent material conductivity. The conductivity value at a reference temperature of 20°C is used in this analysis. Once the winding resistance and the current are known the copper loss can be calculated.

In general, the current in the inductor contains an AC component. High order harmonics are present in the power converter and these induce losses. But for simplicity, the total power loss in the winding is estimated by considering the fundamental frequency only.

The gap loss can be calculated using Equation 4.30 [175] .

$$P_g = 0.0775 * l_g * E * f_s * {B_{acpeak}}^2 \quad (4.30)$$

where l_g is the air gap, E is the tongue width of the gap in cm, f_s is switching frequency in Hz, B_{acpeak} peak flux density in Tesla, and P_g is the gap loss in Watts.

Two losses are predominant in the inductor loss mechanism. These losses can be categorised into core losses and copper losses. The core losses are electric load independent while the copper losses are dictated by the operating load. Core losses are also affected by the eddy current effect in the magnetic core material and the alteration of the non-linear B-H curve. The effects of the eddy current and hysteresis loss can be combined and generally, the core manufacturer provides the empirical equation of core loss density and to some extent provides the loss density curves. By fitting the curves of the loss density core loss can be modelled.

The modelled equation can be expressed as follows:

$$P_{cr} = k * {f_s}^{\alpha} * {B_{acpeak}}^{\beta} \quad (4.31)$$

where, k is the material coefficients, f_s is the switching frequency in kHz, B_{acpeak} is the Flux density in mT and P_{cr} is the core losses in $\mathrm{mW/cm^3}$ respectively

Core losses can be modelled according to Metglass AMCC-6.3 core [172].

$$P_{cr} = 6.5 * {f_{sw}}^{1.51} * {B_{acpeak}}^{1.74} \quad (4.32)$$

Where f_s is the switching frequency in kHz, B_{acpeak} is the peak flux density in tesla (T) and P_{cr} is the core losses in W/kg.

Winding losses can be estimated by using RMS current in the winding. In this work a current density of around $5A/mm^2$ in the winding conductor is assumed. The required winding cross-sectional area can be approximated for the current which flows through the inductor.

To calculate the copper loss, average length of the turn has been calculated from the dimension of the winding bobbin. The mean resistance per turn can be estimated by using the parameters like area of copper foil and resistivity of copper at 60°C. Finally, total resistance and power losses have been calculated using the obtained total turn number.

The temperature rise of the inductor due to copper losses, core losses and gap losses has been calculated using the method described in [172]. To estimate the effective surface area, a hypothetical box is considered around the inductor which includes the winding and the core. Then the total effective convective surface area (SA) has been calculated from the manufacturers provided geometric parameters of the selected core. The surface area can be calculated as follows:

$$SA = 2 * f * (b + d) + 2 * (b + d) * (b + e) + 2 * f * (b + e) \quad (4.33)$$

Temperature rise can be predicted using the following equation adapted from [172]:

$$\Delta T = \left(\frac{P_{losses\ in\ inductor}}{SA}\right)^{0.833} \quad (4.34)$$

4.4.1 Inductor Design Example for Boost converter

To illustrate the preceding design toolbox, a design procedure for an inductor in the boost converter is given in Appendix E.

4.4.2 Performance Evaluation of Inductor

The performance of the designed inductor for the boost converter depends on the parameters like inductor current, winding resistance and winding power losses etc. To minimise temperatures, losses need to be reduced. Therefore, to evaluate the performance of inductor, losses in the designed inductor need to be estimated. Since both the skin effect and proximity effect affect inductor loss mechanism, these need to be considered in the loss evaluation as well [176].

The winding losses in the inductor winding consist of a DC component and an AC component. The DC component is dependent on the DC resistance of the winding as well as the DC component of the inductor current. The AC component is dependent on the AC resistance of the windings as well as harmonics in the inductor current [176].

To estimate DC winding losses, DC resistance of the winding is an important parameter in the analysis which needs to be calculated.

The DC resistance of the winding can be estimated as:

$$R_{dcwinding} = \frac{\rho N l_{winidng}}{A_{winding}} = \frac{2.1124*10^{-8}*43*.1720}{13*10^{-6}} = .0120\Omega \quad (4.35)$$

The winding losses generated by DC winding current can be estimated as:

$P_{dcloss-winding} = {I_{max}}^2 * R_{dcwinding} = 23.46^2 * .0120 = 3.3118W$..................(4.36)

Similarly, AC winding losses due to an AC winding current can be estimated as:

$P_{acloss-winding} = {I_{acmax}}^2 * R_{acwinding} = 4.3292^2 * .3223 = 6.040W$................. (4.37)

Finally, total winding losses can be estimated as:

$P_{total-winding} = P_{dcloss-winding} + P_{acloss-winding} = 3.3118 + 6.040 = 9.3518W$... (4.38)

4.4.3 Capacitor Thermal Analysis

Usually to serve the purpose of storing and filtering, usage of capacitors is increasing in the converter's applications. Aluminium electrolytic capacitors are finding extensive applications due to having their low cost per microfarad and per ripple ampere as well as high volumetric efficiency.

It has been observed that the lifetime of the capacitor is interlinked to the operating temperature. The temperature dependency of the capacitor can be included in the thermal model and it is described in Appendix G. To predict the temperature of the capacitor, thermal model parameters are required to be extracted.

4.4.4 Thermal Modelling of the Metallized Film Capacitor

As it is known that the individual metallisation and dielectric layers are very thin, thus in the thermal modelling of the film capacitor bulk thermal conductivities in the axial and radial directions will be used. This approach has been taken in [177]. A small element of the capacitor winding as shown in Figure 4.21 will be considered.

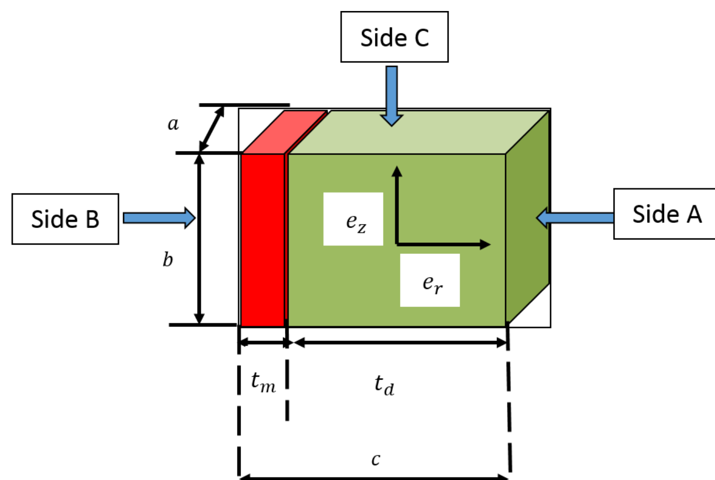


Figure 4.21 Very small element of the film capacitor.

The small element of the film capacitor can be represented by the geometric parameters like dielectric layer thickness (t_d), mettalisation layer thickness (t_m), length (c), width (a) and height (b) respectively.

To determine the thermal conductivity in both radial and axial direction, thermal conductivity of both the dielectric layer (k_d) and metallisation layer (k_m) are considered in the calculation.

Now, from the above figure, the thermal resistance between side A and B can be expressed as:

$$R_{AB} = \frac{1}{k_d} * \frac{t_d}{a*b} + \frac{1}{k_m} * \frac{t_m}{a*b} = \frac{1}{a.b} \left(\frac{t_d}{k_d} + \frac{t_m}{k_m}\right) \quad (4.39)$$

Hence, the thermal conductivity along the radial axis (k_r) is:

$$k_r = \frac{1}{R_{AB}} * \frac{c}{a*b} = \frac{t_d+t_m}{\frac{t_d}{k_d}+\frac{t_m}{k_m}} \quad (4.40)$$

Again, the thermal resistance of the same element between side C and D can be expressed as:

$$R_{CD} = [k_d * \frac{t_d*b}{a} + k_m * \frac{t_m*b}{a}]^{-1} \quad (4.41)$$

So, the thermal conductivity along the vertical axis (k_z) is:

$$k_z = \frac{1}{R_{CD}} * \frac{a}{b*c} = \frac{t_d*k_d+t_m*k_m}{t_d+t_m} \quad (4.42)$$

As $t_m \ll t_d$, so the above equation can be simplified as:

$$k_z \approx \frac{t_d*k_d+t_m*k_m}{t_d} = k_d + \frac{t_m}{t_d} * k_m \quad (4.43)$$

4.4.5 Thermal Resistances in Different Directions

The hot-spot temperature can be determined by using the lumped thermal resistance concept. Now, in general, heat will flow in radial and axial directions within the capacitor winding. Applying the lumped parameter concept, radial thermal resistance and axial thermal resistance can be determined. To extract the parameter, it is worth considering the capacitor structure as shown in Figure 4.22.

The structure of capacitor can be represented by the geometric parameters like input radius of the roll (r_{in}) , output radius of the capacitor (r_{out}) , height of the capacitor (h_c) and diameter of can (d_c) respectively.

To determine the thermal resistance, thermal conductivity along the radial axis (k_r) and thermal conductivity along the vertical axis (k_z) are considered in the calculation.

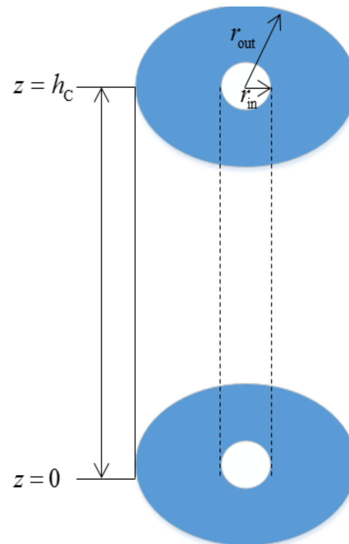


Figure 4.22 Capacitor winding with top and side insulated.

The top, side and bottom of the capacitor are kept at a constant temperature. According to [178], if the power generation is uniform throughout the winding, the axial thermal resistance (R_{axial}) can be determined as:

$$R_{axial} = \frac{h_c}{2*k_z*\pi*(r_{out}^2-r_{in}^2)} \quad (4.44)$$

Again, if the capacitor winding shown in Figure 4.22 is on the top and bottom, the radial resistance (R_{radial}) can be determined as [178]:

$$R_{radial} = \frac{r_{out}^2-r_{in}^2+2*r_c^2*\ln(\frac{r_{in}}{r_{out}})}{4*\pi*k_r*(r_{out}^2-r_{in}^2)} \quad (4.45)$$

It can be seen from Figure 4.22 that the capacitor winding is surrounded by an aluminium case. If the capacitor is firmly placed on a very good heatsink, then heat will flow axially through the can side and bottom.

The thermal resistance of the can-side ($R_{can-side}$) can be expressed as:

$$R_{can-side} = \frac{\left(\frac{1}{2}\right)*h_c}{\pi*k_{Al}*((r_{out}+t_c)^2-r_{out}^2)} = \frac{h_c}{2*\pi*k_{Al}*d_c*(2*r_{out}+t_c)} \quad (4.46)$$

Here, the average path length of the heat flux through the can is $\left(\frac{1}{2}\right)*h_c$. As $d_c \ll r_{out}$, so the above expression can be simplified as [179]:

$$R_{can-side} = \frac{h_c}{4*\pi*k_{Al}*r_{out}*t_c} \quad (4.47)$$

Again, the thermal resistance of the bottom can be expressed as:

$$R_{can-bottom} = \frac{d_c}{\pi*k_{Al}*r_{out}^2} \quad (4.48)$$

Now, the equivalent electrical analogy of the thermal network is illustrated in Figure 4.23.

The core-can thermal resistance (R_{cc}) can be derived as:

$$R_{cc} = \frac{(R_{radial}+R_{can-side})*(R_{axial}+R_{can-bottom})}{(R_{radial}+R_{can-side})+(R_{axial}+R_{can-bottom})} \quad (4.49)$$

So, the total thermal resistance (R_{thc}) will be:

$$R_{thc} = R_{cc} + R_{heatsink} \quad (4.50)$$

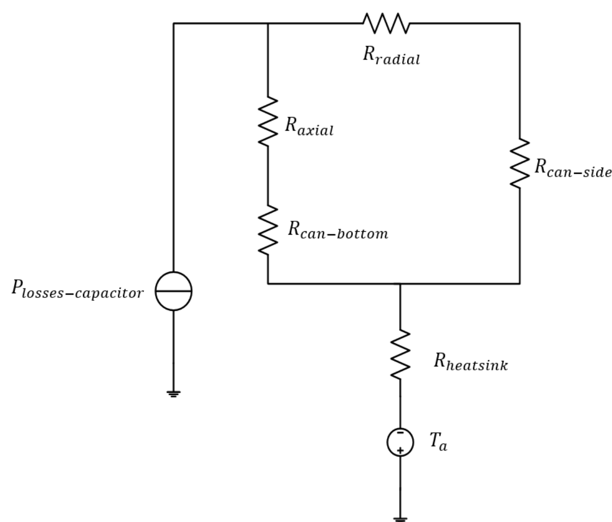


Figure 4.23 Equivalent electrical analogy of the thermal network.

4.5 System Level Integration and Electric-thermal Domain Analysis

Components all are designed by parts are embedded and integrated into the cooling system to build a whole structure of the converter. To achieve high-power density, components sizes are dimensioned initially. Particularly there is an increasing demand in making the size of the converter as small as possible while at the same time enhancing the operating output power capability. The ratio of the processing output power by the converter and the volume occupied by the overall components including a converter structure is called the power density of the system which indicates the compactness of the converter design. It is usually measured and expressed as $[\frac{kW}{liter}]$.

As power electronic converters generate considerable amount of heat and this heat must be removed from the components. The generated heat can be either managed or minimised by using both air-cooled and water-cooled heatsink. Both remove heat by the convection process. Thus, the converter's electro-thermal problem becomes a conduction-convection problem. Conduction happens from the package to heatsink baseplate and after convection occurs at the fins of the heatsink. The convection must be estimated to solve the conduction-convection problem accurately. This can be solved by employing 3-D FEA computational fluid dynamics software. The employment of CFD in the electro-thermal analysis couple the single heat-conduction PDE with four scalar equations (Navier –Stokes) describing fluid flow. Thus, the electro-thermal analysis becomes complex due to becoming a large model which is to be solved by computer. As a result, issues like computational costs and convergence are raised. The concern is that not only the heat-conduction equation has to be solved by each element of the model but also the Navier-Stokes equation has to be solved and the solution can only be achieved when each of the elements could meet the linearisation. Following this, the model might take a very large mesh when the complex power module structure is modelled as it contains many detailed geometric layers. The matrix equation then might become large and take a long time to solve and reach the stability of the solution. This large meshing often causes convergences problems and numerical instabilities for such kinds of complex conduction and convection processes. More often, the flow channel in the cooling plate employs very fine three-dimensional structures with critical layers which are difficult to represent geometrically. Therefore, the flow through these pipes cannot be simulated maintaining an acceptable and desired level of accuracy.

To avoid this problem in terms of simulation speed arising from convective cooling, the air or water cooled heatsink can be modelled for all 3-D FEA simulations if the heat transfer coefficient at the fins can be known. The bottom fins of this cooling system are defined as the boundary of the 3-D FEA model by setting a homogenous heat transfer coefficient which describes convective heat transfer with good accuracy. Now the heat transfer problems have been purely thermal and then no extra arrangement of CFD is necessary. Therefore, the resulting matrix of this kind of large model is significantly reduced which makes the model simple and easy to solve. This simplified approach of convection cooling results in small simulation times, avoidance of numerical instabilities and higher accuracy of simulation results. Thus, the effect of the convection can still be modelled maintaining high levels of accuracy without offsetting the simulation speed and accuracy.

It is important to model the heatsink with the fins because the baseplate acts as a heat spreader in the power electronic converter and heat is transferred from the baseplate to the ambient through fins by the process of conduction and convection. Due to having largest mass, it has a significant effect on the thermal time constants. Therefore, it is essential to represent the cooling system correctly in the model [180-185].

To estimate the heat transfer coefficient for the forced air cooling convection, a program has been developed based on the following assumption.

The heat sink has been represented by its geometric dimension and material property. These include heat sink width (b), heatsink length (L), thickness of heat sink baseplate (t_{base}), fin height (c), fin thickness (t), flow channel (n), flow rate (F) and thermal conductivity of heatsink material (k). Figure 4.24 describes an air-cooled fin-type heatsink geometric configuration.

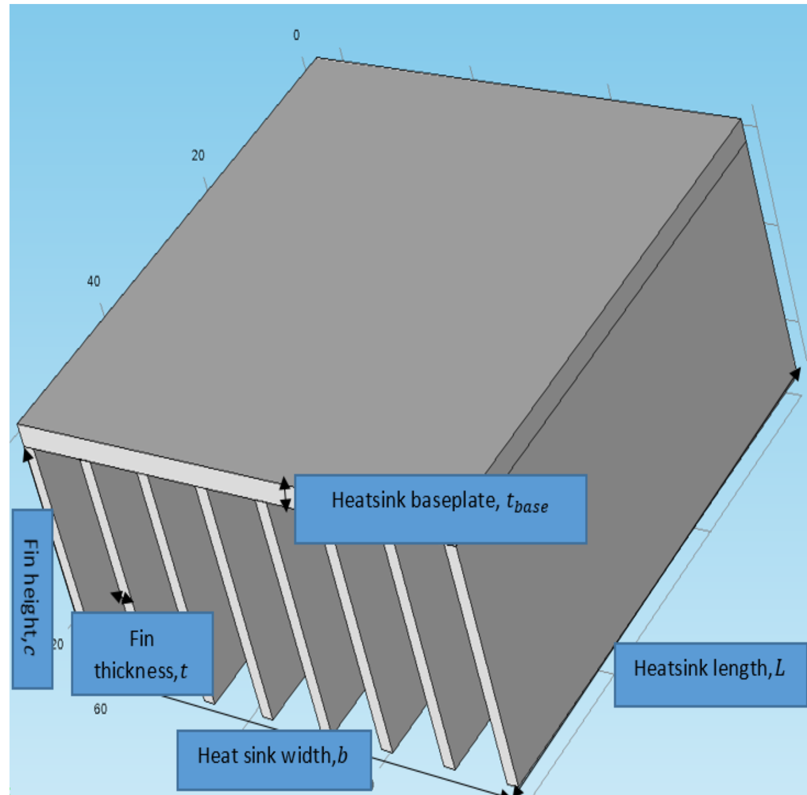


Figure 4.24 Geometrical model of the air cooled extruded fin-heatsink.

A program has been written using the equations listed in Appendix G. The program takes into account the heat sink geometry information as an input. The program automatically calculates the average heat transfer coefficient. The Nusselt number, thermal resistance of the heat sink can be estimated by using this program. The thermal resistance of baseplate ($R_{th,baseplate}$), fin thermal resistance ($R_{th,fin}$) , thermal resistance of baseplate to air ($R_{th,a}$) and thermal resistance of fin to air ($R_{th,A}$) can be estimated. As the thermal resistances, i.e. $R_{th,fin}$, $R_{th,A}$ and $R_{th,a}$ depend on the volume flow, the geometry and the position along the longitudinal axis of the channel, the effect of all these factors must be considered in the calculation. All these thermal resistances can be accurately modelled according to [182] and [183] and can be combined and expressed as a single thermal convective resistance. The thermal resistance formula for air cooled extruded fin-heatsink is described in Appendix G.

4.6 Integrated Electric-thermal Software Coupling

The electro-thermal analysis of power electronic systems involves many disciplines such as control theory, circuit theory, semiconductor physics, material sciences and heat transfer etc. The design framework that has been adopted for modelling electro-thermal behaviour in converter applications is illustrated in Figure 4.25. It solves the electro-thermal problem combining the design input of the converter, geometric structure of the components, material properties and loading profile etc.

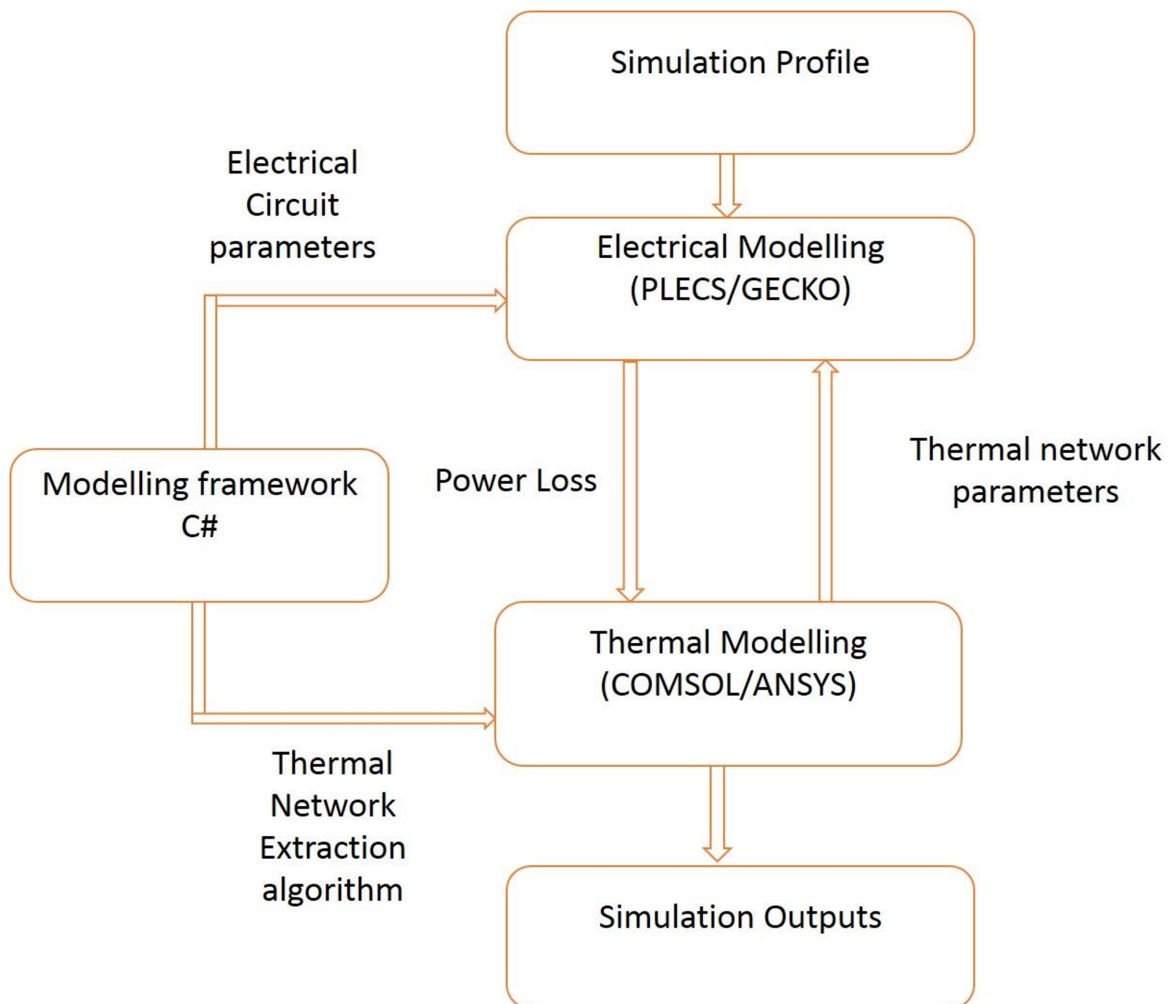


Figure 4.25 Structure of the integrated electro-thermal modelling framework.

4.6.1 Description of the Integrated Framework

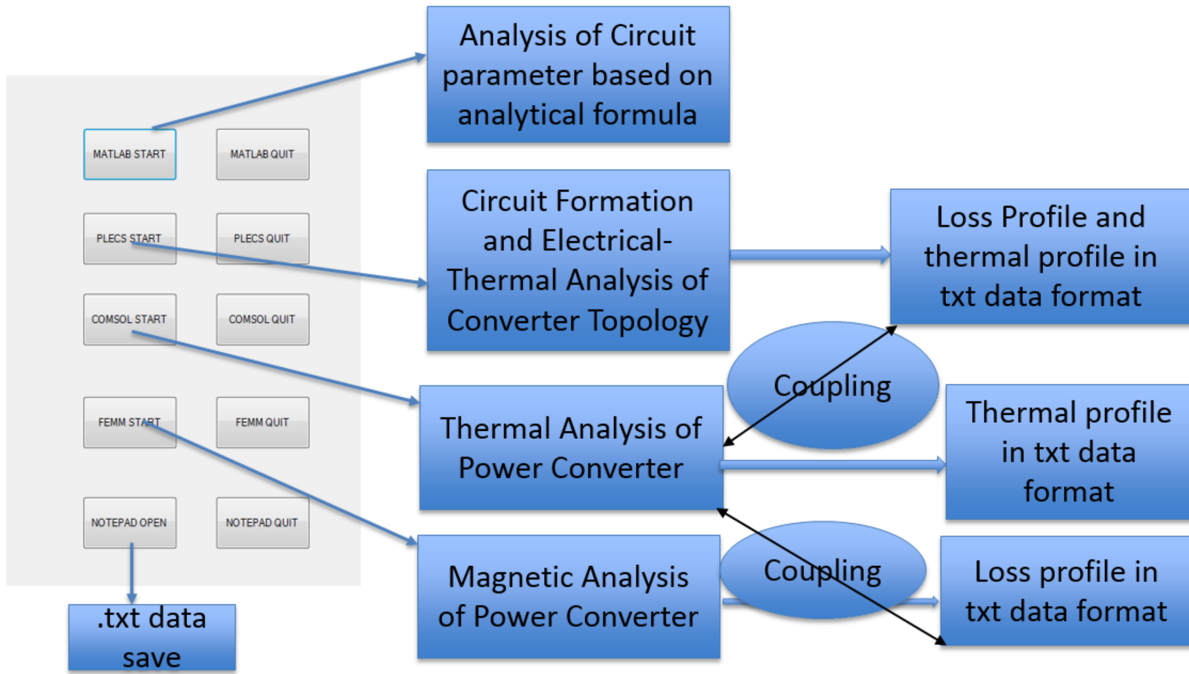
The software packages which are used in power electronics system design lacks in the ability of interaction and data transfer. The circuit method, i.e. the power loss model is not coupled to FEA software. Integration framework is required to interface with the CAD based FEA

software and permit data sharing between them. It is then useful to deal with the multidisciplinary design analysis.

In doing so, a framework in the form of GUI software has been developed where the converter design process can be performed step wise and relevant losses can be obtained. The corresponding thermal network parameters can be extracted by applying these losses in the FEA model which is constructed in COMSOL Multiphysics. To begin the process, the framework first takes the converter design as the input. Then the corresponding electrical model parameters are extracted to build a circuit model in PLECS. Inside the PLECS, the components are represented as temperature-dependent models. The circuit simulator, PLECS provides the power losses and these losses can be exported to the FEA model in COMSOL. These loss data can be exported to Excel through the data interface and later stored Excel data can be imported in COMSOL. After conducting the FEA heat transfer simulations the required thermal impedance curve is extracted including the heatsink model and later this data is post-processed within the framework. For simplicity, the program is written to extract the thermal parameters and these can be displayed in the framework. Later these parameters are used to construct the thermal model. This improves the accuracy of the lumped thermal model and solves the problem of the inaccurate prediction of temperature from the manufacturer-provided thermal parameter.

The framework is established with the combination of GUI software which manages the design variables and performs the analysis process step-by-step. Three tools are integrated to perform simulations. These include FEA-based COMSOL Multiphysics, MATLAB and the circuit simulator PLECS. GUI consists of many design programs which have inputs and outputs both in the form of plain text files, for control program GUI to provide the parameter values for the analysis of results. An in-house GUI integration tool is developed to simplify the configuration by providing a generic interface to FEA model manipulations and thermal parametric studies. This GUI is written in C#.

The design framework is shown in Figure 4.26.



(a)

(b)

Converter Topology Specifications

Input Voltage,Vin: V
Output Voltage,Vout V
Output Power,Pout kW
Efficiecny,n: %
Ripple current ratio,r: %
Switching frequency,fsw: kHz

Inductor Design Specifications

Magnetic flux desnity,B: T
Current density,J: [A/mm^2]
Copper fill factor,K:
Core limb width,a: mm
Window width,b: mm
Window length,c: mm
Core thickness,d: mm
Core width,e: mm
Core height,f: mm
Mean magnetic length,lm: mm
Core effective cross section area,Ae: mm^2
Foil width,W: mm
Operating temperature,T: [°C]
Core weight,wt: kg

Design Output

AC peak flux density,Bac: T
Turn numbers,N:
DC winding resistance,Rdc: [Ω,ohm]
AC winding resistance,Rac: [Ω,ohm]
Skin depth: [m]
Resistance factor,Fr:
DC Power losses,Pdc: W
AC power losses,Pac: W
Gap loss,Pgap: W
Pgap1: W
Core losses,Pcore: W
Total Power losses,Ptot1: W
Total Power Losses,Ptot2: W
Temperature rise,DT1: [°C]
Temperature rise,DT2: [°C]

Inductance,L: [H]
Peak-to-Peak ripple current [A]
Air gap length,lg: [m]
Foil thickness,H: [m]
Convective surface area,SA: [m^2]

Inductor Thermal model parameter

Inductor Design + Loss modelling

(c)

Inductor Specifications

Core loss,Pc: W
Winding loss,Pw: W
Winding temperature,Tw: [°C]
Core temperature,Tc: [°C]
Ambient temperature,Ta: [°C]

Inductor Thermal model

Thermal network paramters

Rth1: [°C/W]
Rth2: [°C/W]
Rth3: [°C/W]

Heat sink model

(d)

Capacitor Geometry Details

Inner radius,rc: mm

Outer radius,rout: mm

Height,hc: mm

Can thickness,tc: mm

Dielectric thickness,td: μm

Metallization thickness,tm: nm

Dielectric thermal conductivity,kd: [W/(m.K)]

Metallization thermal conductivity,km: [W/(m.K)]

Can thermal conductivity,kAl: [W/(m.K)]

Design Output

Radial thermal conductivity,kr: [W/(m.K)]

Axial thermal conductivity,kz: [W/(m.K)]

Axial thermal Resisatnce,Raxial: [°C/W]

Radial thermal Resisatnce,Rradial: [°C/W]

Canside thermal Resisatnce,Rcanside: [°C/W]

Bottom thermal Resisatnce,Rbottom: [°C/W]

Calculate

(e)

Heatsink Specifications

Width,b: mm

Heatsink length,L: mm

Base thickness,tbase: mm

Fin height,c: mm

Fin thickness,t: mm

Flow channel,n:

Flow rate,F: m^3/s

Thermal Conductivity,Heatsink,λ_hs: [W/(m.K)]

Design Output

Nusselt Number,Nu:

h: [W/(m^2.K)]

RthA: [°C/W]

Rthbaseplate: [°C/W]

Rthconv: [°C/W]

Rthd: [°C/W]

RthFin: [°C/W]

Rthsa: [°C/W]

RthSA: [°C/W]

Calculate

Component interaction

(f)

Foster network parameters

R1: [°C/W] C1: [°C/W]

R2: [°C/W] C2: [°C/W]

R3: [°C/W] C3: [°C/W]

Close Run

Cauer network Parameter Extraction

(g)

Cauer network parameters

R1: [°C/W] C1: [°C/W]

R2: [°C/W] C2: [°C/W]

R3: [°C/W] C3: [°C/W]

Run Close

(h)

Figure 4.26 (a) Generic design framework (b-h) electro-thermal modelling tools.

4.6.2 Interface to PLECS Circuit Simulation

The interface to PLECS circuit simulation is provided through a program written in GUI. It combines PLECS schematics and PLECS scope. This is because the circuit simulation includes two steps such as circuit simulation that is carried out in schematics and performance analysis that is carried out in scope. These script files contain commands for setting up the analysis for calculating and recording the power dissipation into a text file running behind a MATLAB program. All the inputs to the PLECS circuit simulator are electrical design parameters that are outputted from the GUI.

4.6.3 Interface to COMSOL FEA Thermal Simulation

The interface to thermal simulation is created through an in-house integration GUI tool that has been developed using C#. This tool supports the fundamental calculations that are required for parameter changes and thermal simulation and provide a platform to perform these operations through a simple format text file. The operations that are currently supported through this interface include modifying power converter design parameters, replacement of thermal boundary conditions and obtaining temperature profiles for given devices. For GUI, the input file contains the converter components loss model parameters. Then the proposed framework calculates the losses processing the input file. The obtained loss profiles data are stored in Excel by data format button in the GUI and then the stored loss profiles data are read by the COMSOL for thermal simulation. The software interfacing is illustrated in Figure 4.27.

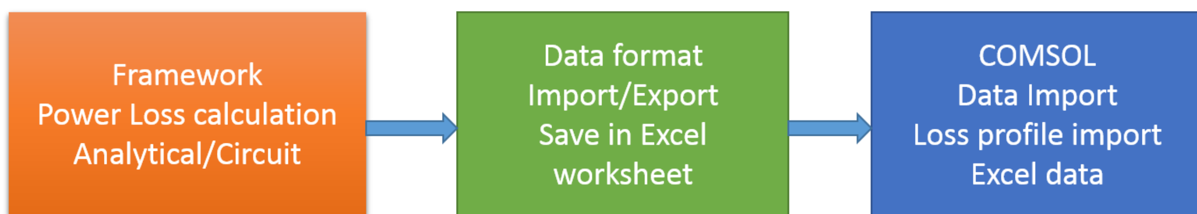


Figure 4.27 Software interfacing.

As for now, the modelling approaches and integrated simulation platform will be adopted to analyse component interaction for three converter applications such as boost converter, inverter and IPT based dual interleaved bidirectional boost converter.

4.7 Case Study

To demonstrate the component interaction, three converter applications will be investigated. The first one considers boost converter topology where the IGBT and diode are mounted on

the same heatsink. The second one considers the three-phase voltage source inverter topology where the component interaction between IGBT and diode in the half-bridge IGBT module will be analysed. The last one is set up to validate the modelling performance in comparison with the experimentally tested converter results. The third converter application considers the topology of IPT-based dual interleaved bidirectional boost converter which is used in a hybrid electric vehicle. Now the design analysis of DC-DC boost converter topology will be discussed.

4.7.1 Design analysis of a DC-DC Boost Power Converter Topology

A DC-DC boost converter has a relatively simple design and it is widely used in power electronics systems such as hybrid electric vehicles, battery regulation systems and more. This section will discuss an analysis on the electro-thermal model integration, the performance and robustness of the proposed electro-thermal analysis framework.

4.7.2 Analysis of a Boost Converter

The DC-DC boost converter topology considered in this work has a power rating of 5kW. The electrical parameters of this topology are listed in Table 14 and the converter specifications are listed in Table 15.

Table 14 Electrical parameters of the DC-DC boost converter topology

Inductance, L	1.021mH
Capacitance, C	50μF
Load Resistance, R_{load}	50Ω
On-resistance of Switch, R_{on-S}	22.3mΩ
On-resistance of Diode, R_{on-D}	60mΩ

Table 15 DC-DC boost converter specifications

Input Voltage, V_{in}	250V
Output Voltage, V_{out}	500V
Output power, P_o	5kW
Efficiency, η	98%
Switching frequency, f_{sw}	20 kHz

To build the converter topology, electrical analysis has been performed by the framework and the electrical parameters are obtained using the converter specifications. Then, by combining the electrical parameters, input voltage source as well as other elements such as the gate drive unit and load etc. the electrical model of the converter topology is built in PLECS. In the converter electrical model, each component is represented by loss model. The semiconductor device of both IGBT and diode is represented by its electrical and thermal properties which are derived from the manufacturers supplied datasheet. This component's loss model will be further integrated into the thermal model of the components combining the effects of both self-heating and cross-heating. Now to derive the thermal network parameters due to self-heating and cross-heating, detailed FEA analysis will be performed.

4.7.3 FEA Analysis of a Boost Converter

To demonstrate the component interaction, initially, a CAD model of the converter is constructed in FEA using the geometric information of the component structure. A schematic of the converter system containing IGBT and diode is shown in Figure 4.28, the dimensions are taken from [169-170] and the material properties are listed in Table16. The converter components of IGBT and diode are labelled as T1 and T2 respectively. Since the components share the same cooling system, the cooling system is also needed to be included in the thermal model. Then the components material properties are assigned. The whole structure is meshed and solved by FEA solver. To record the temperature at the junction node of both chips, the centre point of the top surface of both chips is chosen. The chosen point's temperature can be recorded as T_{j-IGBT} and $T_{j-Diode}$ respectively.

To solve the FEA thermal model, the power dissipation which is used as heat source in the thermal model needs to be calculated. The power losses can be calculated by the framework that analyses the electrical behaviour in PLECS and the value of power losses can be obtained from the component's power loss characteristics. By using the framework, the energy dissipations in the IGBT and the diode can be calculated and these losses are 31.92W and 16.23W respectively. Then these losses are exported to the FEA thermal model by data exchange format and applied at the top surface of the chips. The recorded temperature responses are converted into transient thermal impedance responses. The transient thermal impedance responses are curve-fitted to Equation 4.58.

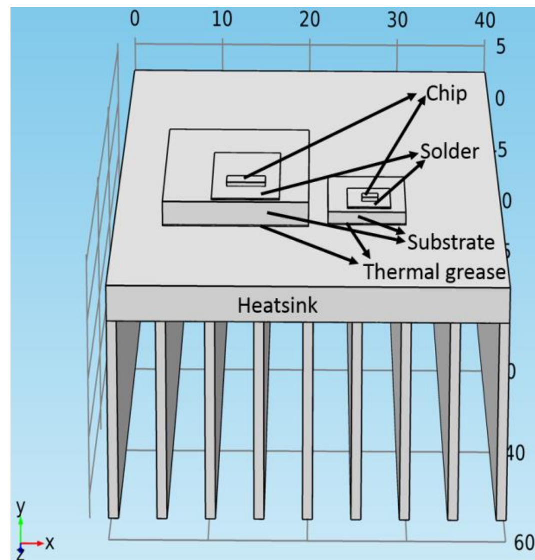


Figure 4.28 The converter components.

Table 16 Converter material properties and dimension details [169-170].

Material	Volume, L*W*t (mm^3)	Density, kg/m^3	Specific heat capacity, $J/(kg.K)$	Thermal Conductivity, $W/(m.K)$
IGBTs(Si)	4*1.72*360e-3	2329	700	150
Diodes(Si)	1.66*1.01*360e-3	2329	700	150
Solder-IGBT	7*0.127*12.5	9000	150	50
Solder-Diode	4.45*0.127*5	9000	150	50
Copper Substrate-IGBT	15*20*2	8700	385	400
Copper Substrate-Diode	8*9.45*1	8700	385	400
Thermal grease-IGBT	15*20*0.13	1180	1044	1.5
Thermal grease-Diode	8*9.45*0.13	1180	1044	1.5
Aluminium	40*60*3	2700	900	201

4.7.4 Modelling of Thermal Interaction

To model the interaction between IGBT and diode in the converter system, electrical model is coupled to the thermal network and the other components in the converters are assumed to be inactive as the components are outside the heatsink.

To extract the parameters for the RC pairs, the thermal impedance between the junction and the ambient is required. These can be extracted from the FEA thermal modelling of the component interaction. The thermal parameter extraction process has been demonstrated in [186] .The method uses transformed thermal impedance responses. FEA simulations have been performed twice to obtain the thermal responses due to self-heating and cross-heating in the IGBT-diode pair. In the first simulation, only the IGBT is active and in the second simulation, only the diode is active. From these results, self-heating and cross-heating thermal impedance response curves at the selected thermal network are derived. The selected nodes correspond to the locations at the centre of the top of the chip and followed vertically the bottom of the chip. The nodes of both IGBT and diode chips are denoted by letters *'p'*, *'q'*, *'r'* and *'s'* respectively (Figure 4.29). Lower subscript *'I'* and *'D'* denote the IGBT and diode respectively. In the following, the lower subscript *'j'*, *'a'* respectively denote the junction, ambient respectively, and the temperatures at these selected locations for the IGBT and diode are T_{jIp}, T_{aIq} , T_{jDr} and T_{aDs} respectively.

The network includes both the self-heating and the cross-heating of the components and the thermal interaction between the IGBT and the diode in the converter can be described by Equation 4.51 as follows:

$$\begin{pmatrix} T_{jIGBT} \\ T_{jDiode} \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} * \begin{pmatrix} P_{loss-IGBT} \\ P_{loss-Diode} \end{pmatrix} + T_a \quad (4.51)$$

where, T_{jIGBT} is IGBT Junction temperature, T_{jDiode} is diode Junction temperature, Z_{11} , Z_{22}: self-heating impedance of IGBT and diode, Z_{12} , Z_{21}: cross-heating impedance of IGBT and diode, $P_{loss-IGBT}$ is the power losses in IGBT, $P_{loss-Diode}$ is the power losses in diode and T_a is the ambient temperature

The self-heating impedances of IGBT and diode can be expressed by Equations 4.52 and Equation 4.53 respectively and the cross-coupling impedances are expressed by Equation 4.54 and Equation 4.55 respectively. The meanings of the impedances are explained in Figure 4.29 and are listed in Table 17.

$$Z_{11} = \frac{T_{JIp} - T_{aIq}}{P_{loss-IGBT}} \quad (4.52)$$

$$Z_{22} = \frac{T_{JDr} - T_{aDs}}{P_{loss-Diode}} \quad (4.53)$$

$$Z_{12} = \frac{T_{JDr} - T_{aDs}}{P_{loss-IGBT}} \quad (4.54)$$

$$Z_{21} = \frac{T_{JIp} - T_{aIq}}{P_{loss-Diode}} \quad (4.55)$$

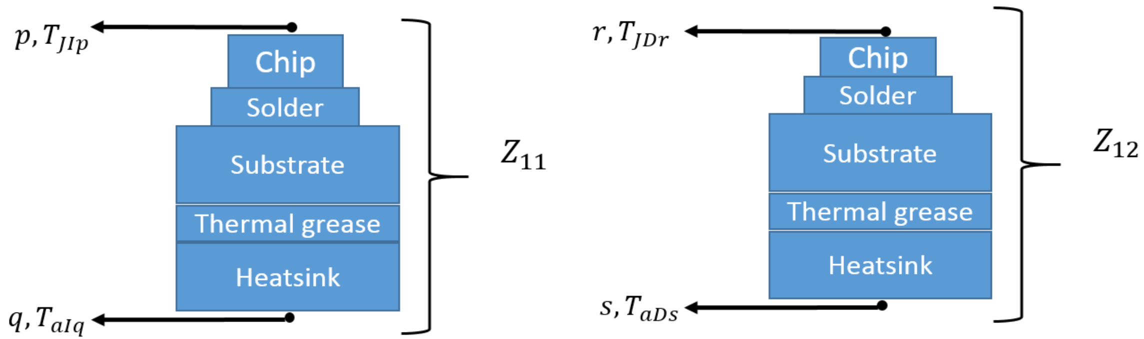


Figure 4.29 The IGBT self-heating and diode cross-heating thermal impedances.

Table 17 Thermal impedance symbols.

Symbols	Meaning
Z_{11}, Z_{22}	Self-heating impedance of IGBT and diode between junction and ambient
Z_{12}, Z_{21}	Cross-heating impedance of IGBT and diode between junction and ambient
T_{JIp}, T_{JDr}	Junction temperature of IGBT and diode at the selected point 'p', 'r' respectively
T_{aIq}, T_{aDs}	Ambient temperature of IGBT and diode at the selected point 'q', 's' respectively

The extraction of RC network parameters from derived transient thermal impedance responses are described in detail in the following sections.

4.7.5 FEA Thermal Analysis and Parameter Extraction Process

To extract the parameters for the RC pairs, the thermal impedance between two nodes is required. These can be extracted from the FEA thermal modelling. The thermal parameter extraction process based on the FEA derived time-dependent temperature responses has been

demonstrated in [186-187]. The process uses the transformed thermal impedance responses. to extract the thermal impedance values for the proposed method, two transient FEA simulations have been performed in which the power loss of either the IGBT or the diode is used as the only heat source. The power loss values are 31.92W and 16.23W for the IGBT and the diode respectively and they are applied to the top surface of both IGBT and diode chips. It is assumed that the components are mounted on a fin type extruded air cooled heatsink. In this simulation, a convective heat transfer boundary condition is applied at the fins of the heatsink and the applied heat transfer coefficient is 57.7 $(Wm^{-2}K^{-1})$ and the ambient temperature is set to 20°C.

The temperature distributions at t=400s simulation time and transient responses at the selected points from the two simulations are shown in Figure 4.30. It is worth mentioning that a time delay occurs in the temperature rise due to cross-heating at the starting time. The reason is that the chips share the same heatsink and it takes time for the heat to transfer from one chip to another. The temperature responses are converted to thermal impedance curves using Equation 4.56 and Equation 4.57 respectively.

$$Z_{th(m-n)}^{self-I} = \frac{T_{mI}(t)-T_{nI}(t)}{P_{loss-IGBT}} \quad (4.56)$$

$$Z_{th(m-n)}^{cross(I-D)} = \frac{T_{mD}(t)-T_{nD}(t)}{P_{loss-IGBT}} \quad (4.57)$$

Where, 'm' and 'n' respectively corresponds to any two consecutive nodes.

By fitting the step response equation to the transient thermal impedance curves, a 3rd order thermal equivalent Foster RC pair parameters can be obtained. Particle Swarm Optimization curve fitting algorithm [188] has been used to fit Equation 4.58 to the impedance data.

$$Z_{th}(t) = \sum_i Rth_i * (1 - e^{\frac{-t}{Rth_i * Cth_i}}) \quad (4.58)$$

where, R_{thi} and C_{thi} respectively corresponds to thermal resistance and thermal capacitance at the ith term.

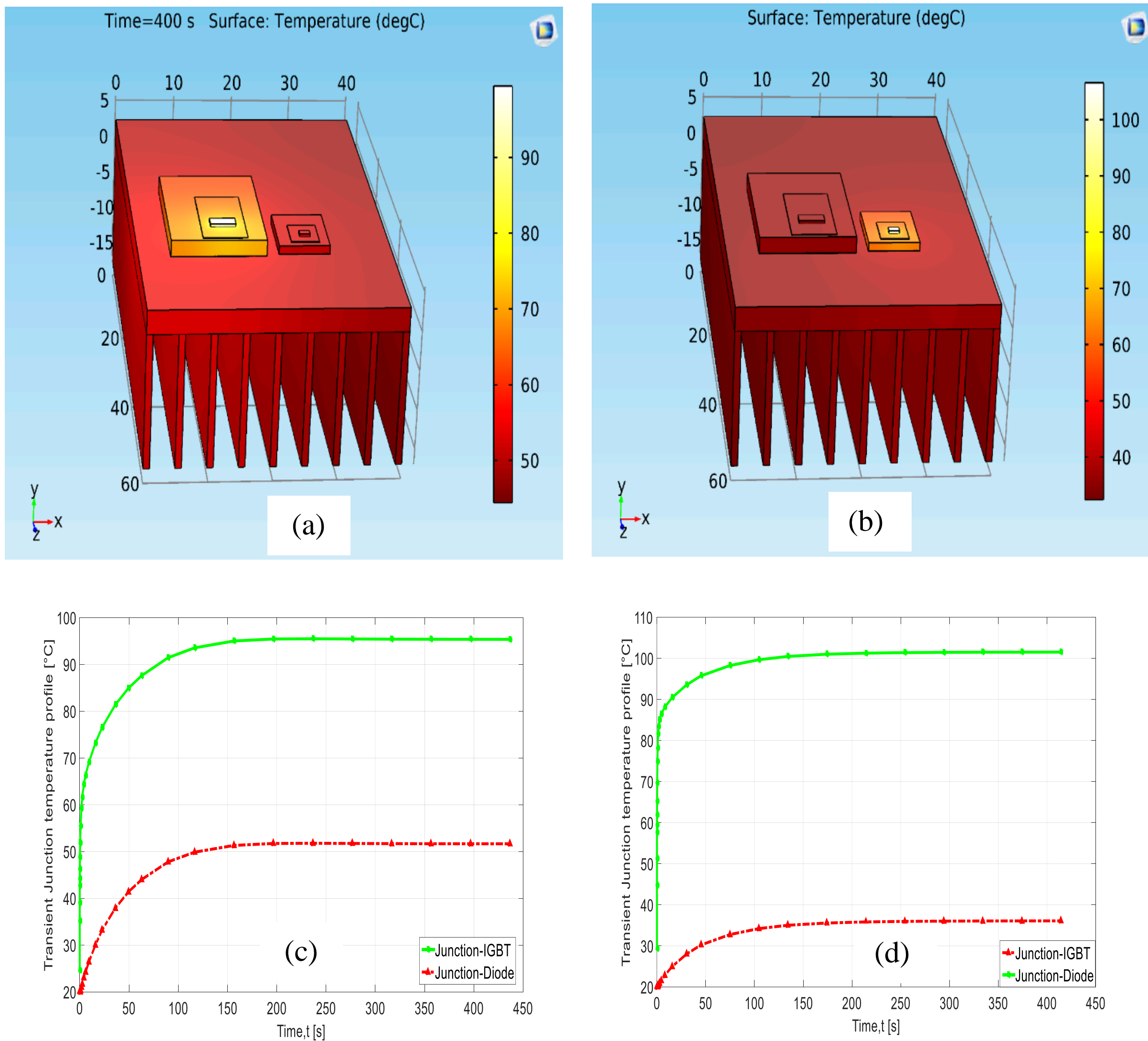


Figure 4.30 (a) Temperature distribution at t=400s. A power loss of 31.92W is applied to the IGBT chip (b) Temperature distribution at t=400s. A power loss of 16.23W is applied to the Diode chip (c) Transient temperature response of IGBT (d) Transient temperature response of Diode.

The set of thermal impedances obtained from the FEA thermal simulation run is stored in a data file and used as an input to the developed tool whose graphical user interface is shown in Figure 4.26 (g). Through the GUI, it is possible to set up the thermal network for the preferred device at the nodes of design interest. The RC thermal network parameters are extracted as Foster-type thermal equivalent circuit. A series of thermal impedance curves can be retrieved and where the extracted thermal network parameters can be used later in building a thermal circuit in PLECS. Once the start button is selected, the tool provides the thermal network parameters in the forms of R and C values of each Foster branch by calling, in the

background, MATLAB framework that performs a series of mathematical fitting operations through built-in optimisation algorithms. Here the thermal resistance and thermal capacitance unit is expressed as $°C/W$ and $J/°C$ respectively.

The analysis of thermal coupling effect has been carried out using a simplified thermal network in which both the self-heating and cross-heating network is modelled using the nodes at the junction and at the heatsink only and the RC pairs of a 3rd order are extracted to represent all the layers between the two nodes. The extracted parameters are listed in Tables 18-21. Figure 4.31 illustrates full temperature distribution when the IGBT and diode dissipate power simultaneously.

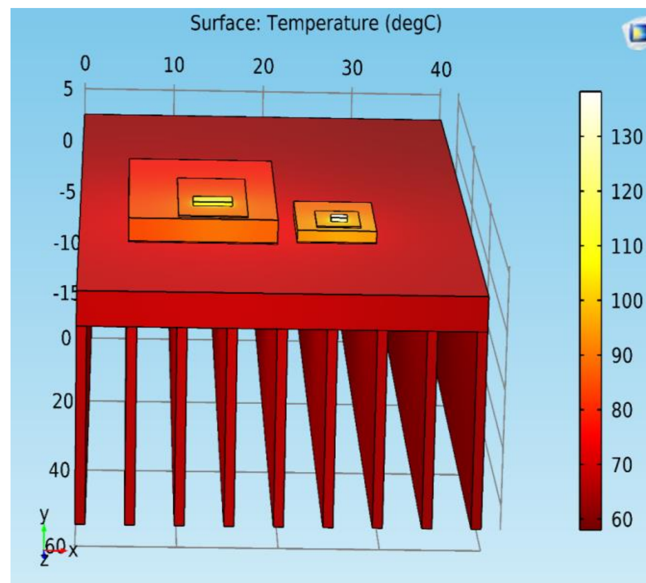


Figure 4.31 Full temperature distribution of the converter system while both chips are dissipating power.

Table 18 Foster network RC parameters for IGBT self-heating

Layer	Term number	1	2	3
Junction-Ambient	$R_{thi}, °C/W$	1.0688	0.5511	0.8568
	$C_{thi}, J/°C$	37.76	1.5184	0.0084

Table 19 Foster network RC parameters for IGBT-Diode cross-heating

Layer	Term number	1	2	3
Junction-Ambient	$R_{thi}, °C/W$	2.2137*10^{-19}	0.9964	1.07*10^{-18}
	$C_{thi}, J/°C$	1.2176	43.4528	5.0567

Table 20 Foster network RC parameters for Diode self-heating

Layer	Term number	1	2	3
Junction-Ambient	$R_{thi}, °C/W$	1.5826	2.6656	1.0615
	$C_{thi}, J/°C$	0.2864	0.0014	36.3567

Table 21 Foster network RC parameters for Diode-IGBT cross-heating

Layer	Term number	1	2	3
Junction-Ambient	$R_{thi}, °C/W$	0.6883	7.1564*10^{-20}	0.3047
	$C_{thi}, J/°C$	83.15	5.36*10^{47}	85.0325

4.7.6 Electro-thermal Analysis of an IGBT-Diode Pair in a Boost Converter

The method described above has been applied to study the thermal coupling effects of an IGBT-diode pair in a DC-DC boost converter. Figure 4.32 describes the DC-DC boost converter that is coupled to the thermal network circuit for the IGBT-diode pair. For the calculation of the power dissipations in the IGBT and diode, the parameters, equations and look-up tables for the modelling converter are constructed as described in section 4.3.3. Figure 4.33 shows the predicted loss profiles in the IGBT and the diode.

For the thermal analysis, the parameters in Tables 18-21 are used in the thermal network circuit model which is shown in Figure 4.34. For the IGBT (or diode), the circuit consists of one branch of a 3rd order RC Foster cells. The thermal branch corresponds to the junction to ambient thermal impedance respectively. The cross-heating has been represented by a 3rd order RC Foster cell for the junction to ambient impedance. As shown in Equation 4.51, the

total junction temperature of the IGBT or the diode consists of the contribution from self–heating, cross-heating and the ambient temperature.

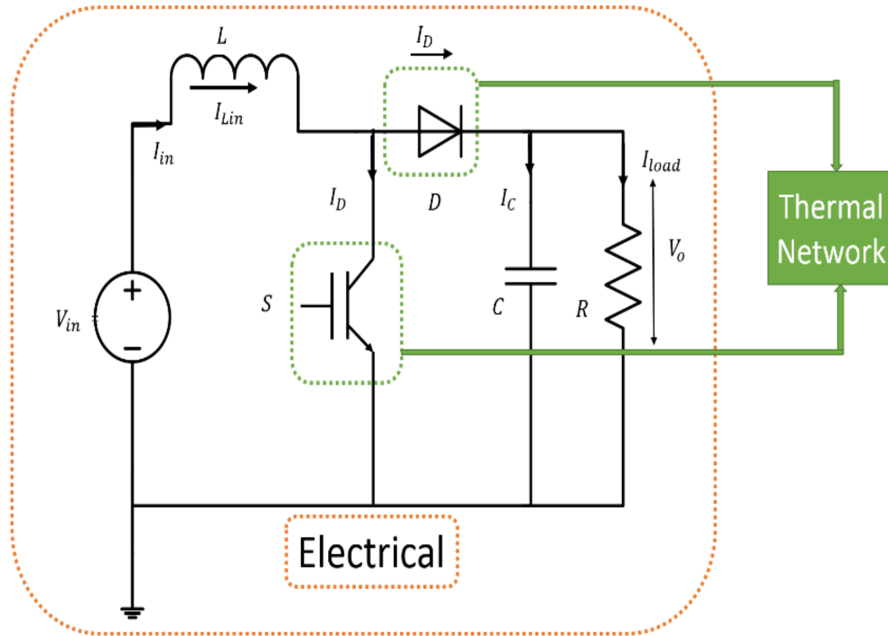
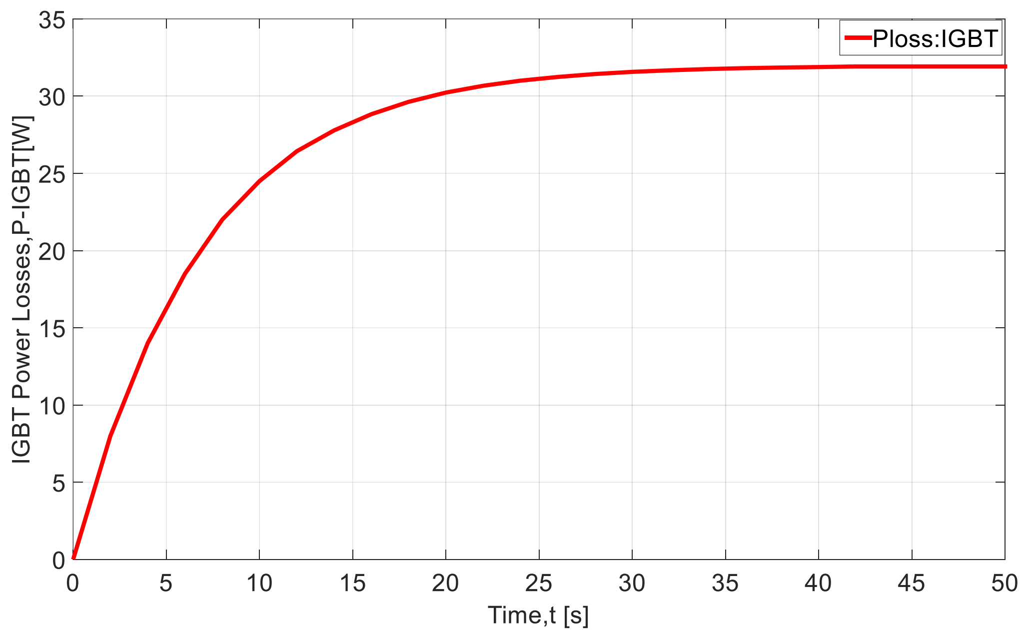
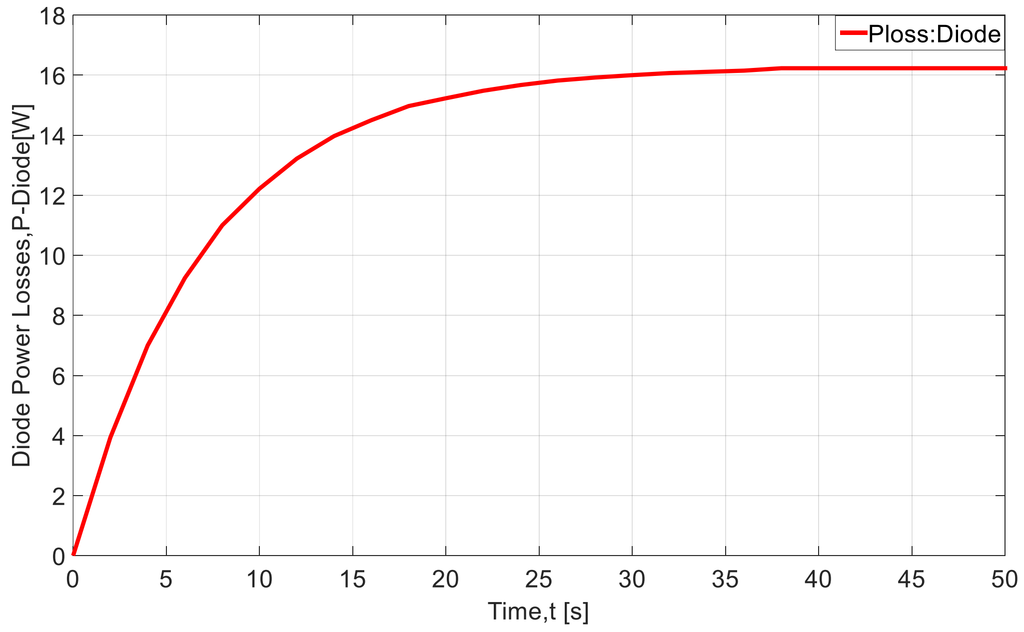


Figure 4.32 Coupled electro-thermal network circuit for a dc-dc boost converter

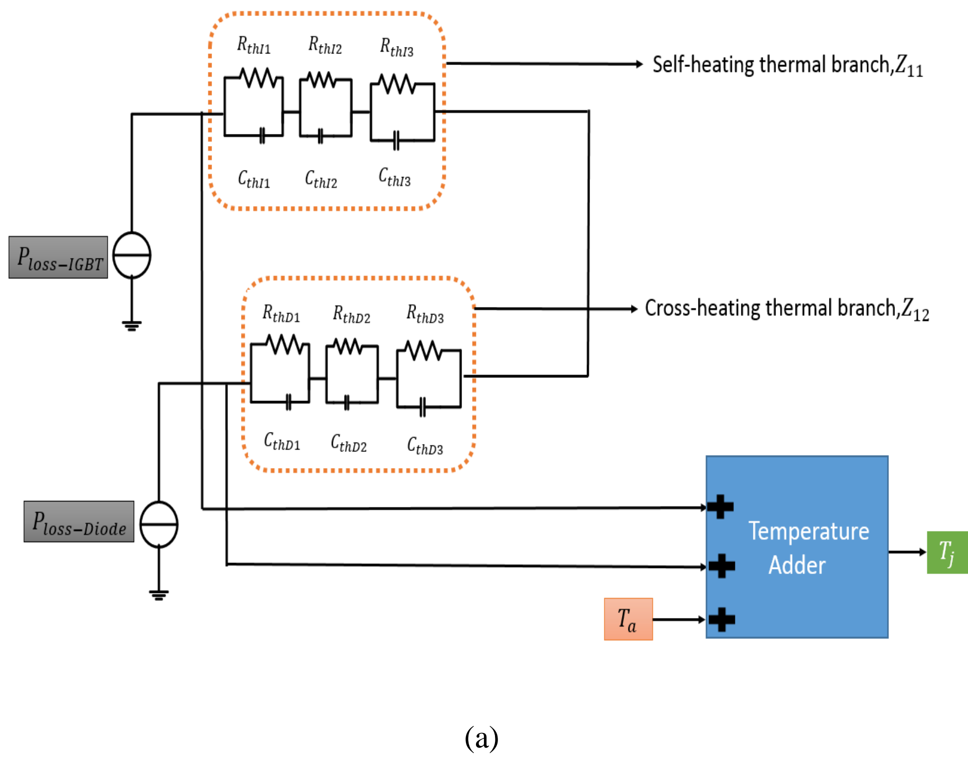


(a)

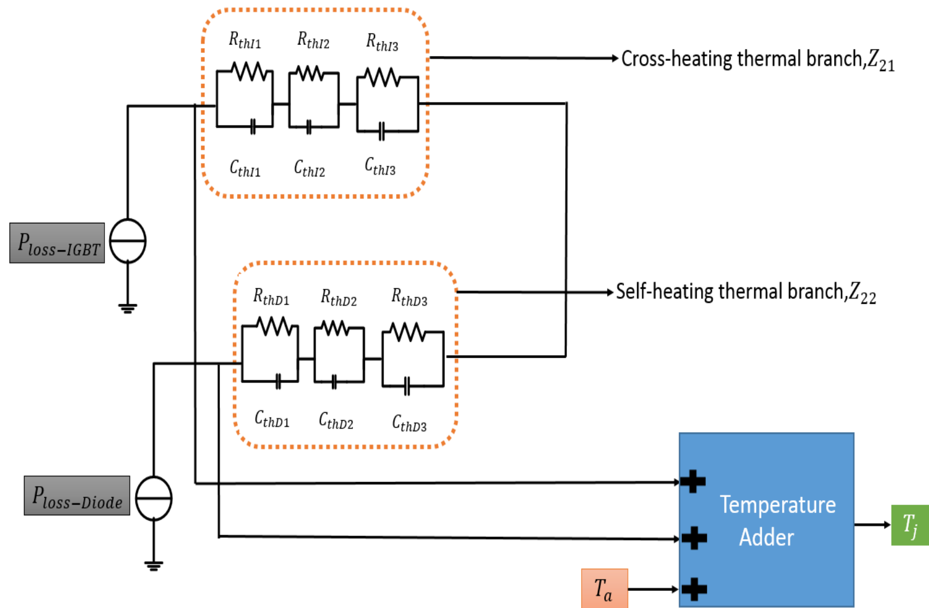


(b)

Figure 4.33 Average loss profiles of (a) IGBT & (b) Diode.



(a)



(b)

Figure 4.34 Thermal network including the thermal coupling between IGBT and diode.

To analyse the impact of the nonlinearity and the thermal coupling effects between components, four models have been analysed: (1) Non-coupled linear model in which electrical properties are not temperature dependent, (2) Non-coupled nonlinear model, (3) Nonlinear coupled, components thermal coupling is taken into account and (4) Nonlinear non-coupled, coupling is not included. In the analysis of the coupled model, the cross-heating impedance is considered while in the non-coupled model, cross-coupling impedance is set as zero to eliminate the influence of the thermal coupling effect. Temperature distribution in the converter component at 400s under transient power dissipation loading condition and a typical dynamic junction temperature history that has been obtained are shown in Figure 4.30 and Figure 4.35 respectively. The temperature histories are compared for models 3 and 4, as well as the FEA results, are shown in Figure 4.35. The yellow curve and cyan curve show the junction temperature of IGBT and diode without thermal coupling effect using the proposed method. They are very different from the results for models with coupling (red and magenta curves). The discrepancy occurs due to not considering the thermal coupling effect. As shown in Figure 4.35, the coupled model results are compared with the FEA and both results conform to each other. A summary of the steady state junction temperatures from all the models are listed in Table 22.

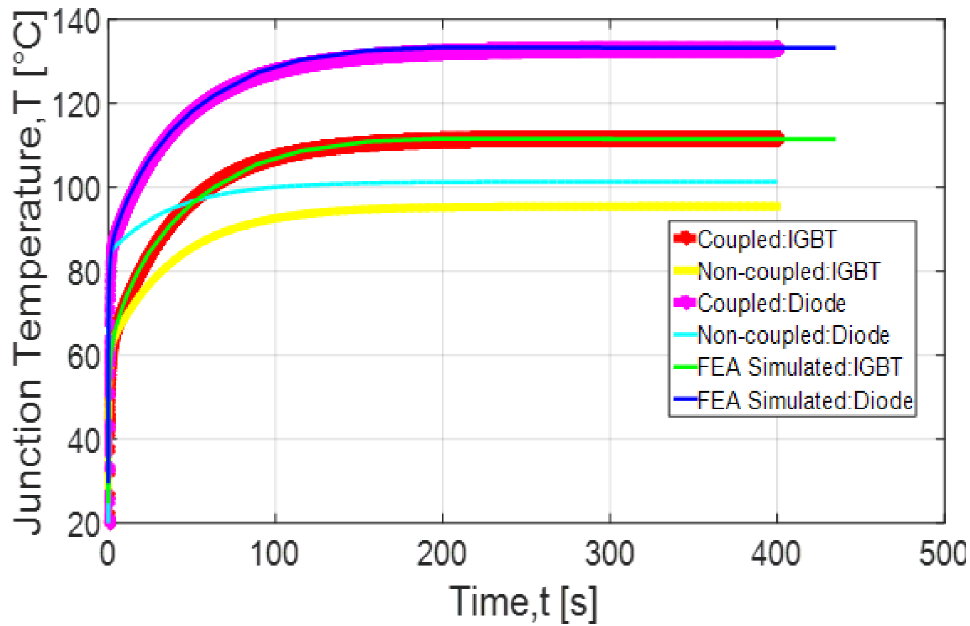


Figure 4.35 Junction temperature profile.

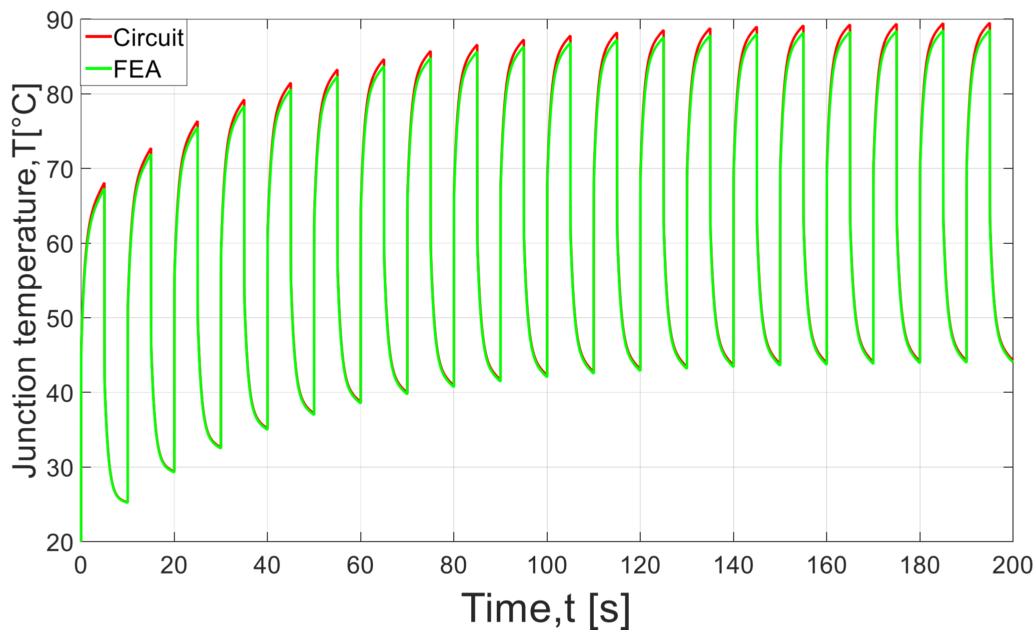
Table 22 The predicted temperature

Model	IGBT (°C)	Diode (°C)
Linear	124.25	124.56
Non-linear	124.85	124.7
Non-coupled	95.43	101.3
coupled	115	138

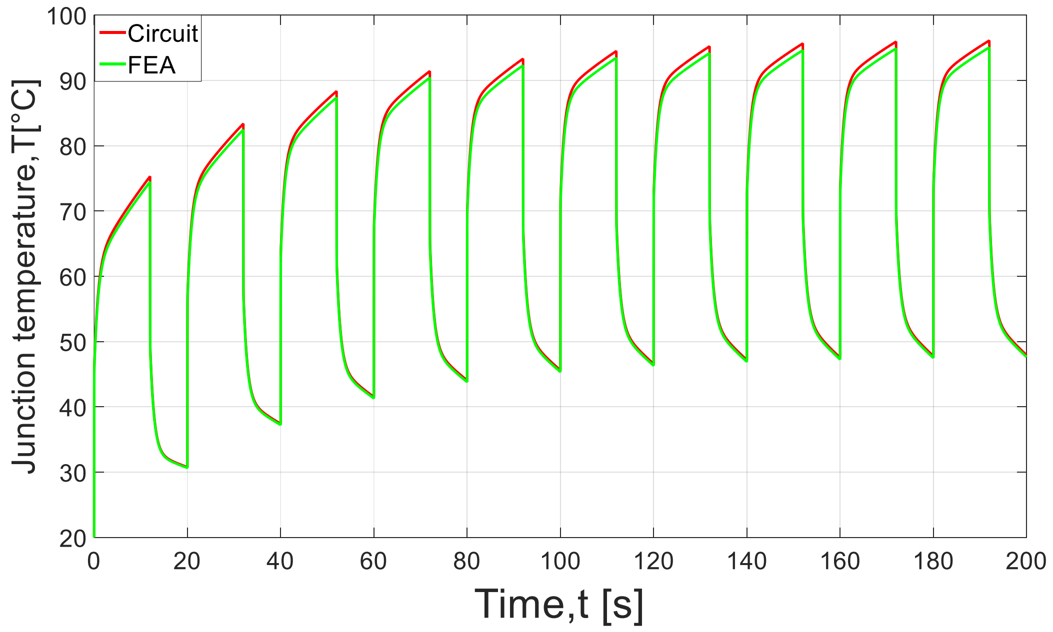
4.7.7 Performance analysis of the proposed modelling method

To apply the proposed thermal model under the changes of mission profile, accuracy and robustness of the model need to be checked. To investigate the performance of the model, four simulations are performed considering the variation of pulse width of the loss profile and variation of the heat dissipation profile and results are compared with the circuit method later. In the first two FEA simulations, the power loss profiles are kept constant and the power loss profile of IGBT and diode is applied 35W and 20W respectively at a duty ratio of 0.5 and 0.6 respectively. Figure 4.36 shows the comparisons of the predicted junction temperature under the variation of duty ratio by the FEA and the circuit equivalent RC network method. It is seen from the figure that the predicted temperature is higher at the duty ratio of 0.6 than that of the loss profile applied at the duty ratio of 0.5. It is expected that the chip gets more time to

be heated up and this results in a temperature rise. The accuracy of the modelling result is high and consistent in comparison to the FEA result. Again, the two FEA simulations have been performed to investigate the modelling performance due to the power loss variation in the chips. In the first simulation, the power loss profile of IGBT and the diode are kept at 60W and 15W respectively and the loss profile is applied at a duty ratio of 0.4. In the second simulation, IGBT power loss is kept similar to first one and only diode power loss is changed and increased double equivalent to 30W and the loss profile is applied at a duty ratio of 0.5. It is seen from the Figure 4.37 that the temperature predicted for both cases by circuit and FEA agrees well with each other. The model can predict the temperature accurately even under the variation of loss profile and variation of pulse width of loss profile. This result suggests that the proposed electro-thermal model can capture the power losses variation and so forth the temperature variation predicted by the proposed model. It can be concluded that the modelling performance is robust and consistent.

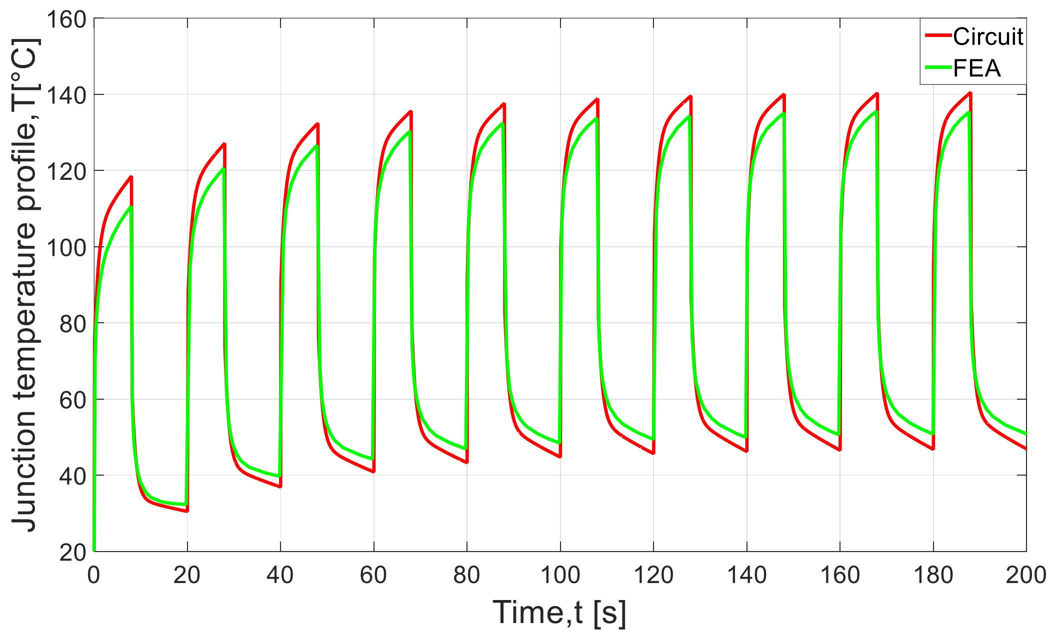


(a)

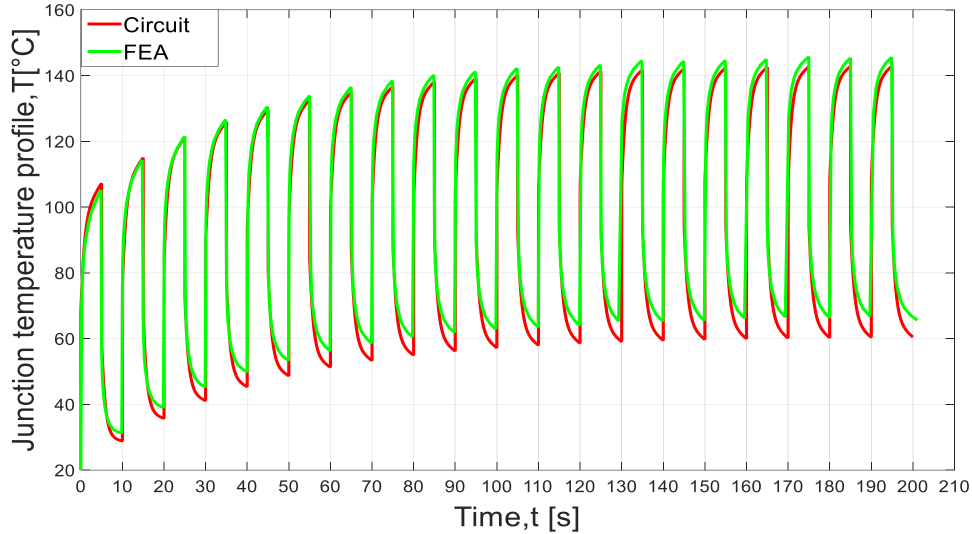


(b)

Figure 4.36 Comparisons of predicted IGBT junction temperature profile by Circuit and FEA method (a) Duty ratio=0.5, (b) Duty ratio=0.6.



(a)



(b)

Figure 4.37 Comparisons of predicted IGBT junction temperature profile by Circuit and FEA method (a) Power Loss Profile (IGBT: 60W, Diode: 15W) at Duty ratio=0.4, (b) Power Loss Profile (IGBT: 60W, Diode: 30W) at Duty ratio=0.5.

4.8 Conclusions

A generalised compact model featuring IGBT-Diode interaction in a DC-DC boost converter at system level has been demonstrated. Summarising all geometric structure and material properties FEA is performed with the power losses in each component. The transformed FEA thermal impedance curves provide the RC compact thermal network covering self-heating and cross-heating. The RC compact model fits well with the time dependent FEA simulation. The proposed method can predict more accurate results than the traditional method. The results indicate that the network models which are based on the lumped parameters derived from the manufacturer-provided data sheet show discrepancy in temperature estimation compared to the results obtained using the proposed method. The predicted temperatures of the thermally coupled models and non-coupled models also differ significantly. The non-coupling model underestimates the junction temperature of IGBT and diode by 19.57°C and 36.7°C respectively comparing to the coupled model, i.e. not taking into account the thermal coupling effects regarding the electro-thermal modelling has resulted in an error of 17% and 26.7% in the estimation of the junction temperature of IGBT and diode respectively.

Chapter 5 Electro-thermal Analysis of IGBT Module of a Three-phase Voltage Source Inverter

In Chapter 4, proposed thermal modelling has been applied to analyse the thermal coupling of the discrete components that share the same heatsink in a 5kW DC-DC boost converter topology. The analysis is performed for short-term electric loading conditions. However, many other factors may have effects on the modelling performance of the components that are mounted on the same substrate and the same heatsink, for example, IGBT modules of a three-phase voltage source inverter in long-term real mission profiles. These factors include the variation of operating cooling boundary conditions, the variation of power losses and the variation of baseplate temperatures etc.

FEA simulations are used for short-term load profiles. However, although accurate, FEA simulations are time consuming and therefore, their use is limited for the analysis of long-term load profiles. In addition to this, a much faster and robust electro-thermal modelling method is required to estimate temperatures for the IGBT module under critical loading. Furthermore, the model needs to consider the thermal coupling effect and it should maintain the accuracy of temperature estimation at the same time. To date, the accurate estimation of the temperature in power modules is still a challenging task. In this chapter, a novel RC parameterised thermal model is proposed for the analysis of thermal coupling between the IGBT and the diode. The method includes a power module’s detailed structure and its constituent material properties. The superposition principle of the thermal model is verified before integrating it into the electrical model. The method also considers the effect of boundary condition. The presented method can be useful for the accurate prediction of temperatures at the critical locations of the components whereas temperature estimation by experimental measurements is difficult.

This chapter is structured as follows: the basics of the thermal modelling and detailed structure of the IGBT module considered are introduced first, the modelling challenges are addressed and operating boundary conditions are explained. Then, the parameter extraction process is described including self-heating and cross-heating. Then, the assumption of linearity of the thermal model is verified. Then, the robustness of thermal model is checked again. Furthermore, the impact of boundary conditions on the thermal model parameters is also discussed. Finally, the performance of the developed thermal model is verified by the

FEA simulation results under the real electric loading conditions in a three-phase voltage source inverter.

5.1 Modelling of Component Thermal Interaction

Based on the proposed electro-thermal model, the component interaction of a three-phase voltage source inverter in this thesis will be studied as an application example. To demonstrate the component thermal interaction, one switch of the half-bridge module is considered as a case study. It contains one IGBT and one antiparallel diode. In this chapter, the step by step thermal modelling procedure will be discussed. To perform an accurate electro-thermal model of the components, components should be represented accurately in a 3D FEA thermal simulation. Therefore, an accurate representation of components in the power module with the real cooling boundary conditions is the most important factor for further analysis.

5.2 Inverter Structure Details and Basics of the Modelling

The IGBT module in the form of a half -bridge configuration under case study consists of two IGBTs and two antiparallel diodes. Both chips are mounted on a substrate to create electrical isolation. The simplified cross-sectional view of an IGBT module is shown in Figure 5.1 (a). The silicon chips are soldered to copper tracks via aluminium wire bonds. The top view of the studied IGBT module (SEMIPAK module SKM75GB123D) is shown in Figure 5.1 (b). To construct inverter three half-bridge modules can be used which has six IGBT chips and six diode chips altogether. In addition, a thermal interface material (e.g. thermal grease) is inserted between the baseplate and the heatsink to improve the physical integrity and heat transfer. In the FEA model of IGBT module the thickness of thermal grease is set as uniform.

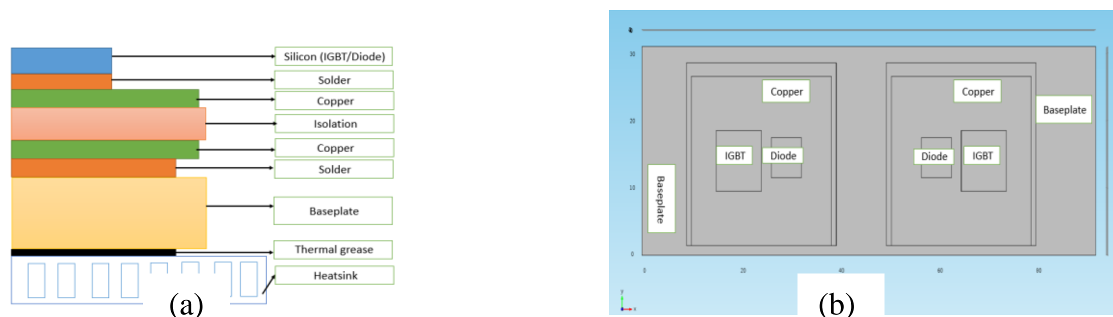


Figure 5.1 (a) Simplified cross-sectional view of IGBT module (b) top view of SKM75GB123D module [189].

5.3 Validation of FEA Thermal Model

Usually, many parameters influence the thermal model and therefore, the accuracy of the model is dependent on these parameters. These parameters include accurate structural configurations, geometric dimensions and material properties, but these parameters are difficult to obtain and verify. However, the manufacturer supplies the transient thermal impedance curves of the power module to the designers and the thermal impedance is affected by all the parameters. Thus, the accuracy of the thermal model can be verified by comparing the FEA derived thermal impedance value to the value provided in the manufacturer datasheet.

To derive the thermal impedance curves, a thermal model for the SEMIPAK IGBT module-SKM75GB123D, rating of 1200V-75A is set up in COMSOL Multiphysics Software as shown in Figure 5.2. As a suitable 3D Numerical simulation tool, the COMSOL Multiphysics [165] is used for determining the detailed temperature distributions including the thermal coupling. The software exploits a finite element method. The geometries and the material properties of the different layers are taken from the reference [189]. The geometric and material properties are listed in Table 23.

The simulation model set up is carried out by the following steps:

First, the geometries of the component are defined. Then, the material properties and appropriate boundary conditions are applied. These first two steps are directly derived from the 3-D thermal FEA setup and the boundary conditions are established according to the cooling conditions of the real system. In the modelling, the heat dissipation is assumed uniform and applied on the top surface of both devices in IGBT or diode. The adiabatic boundary conditions are also applied on the all side surfaces except top surfaces of the chip.

Since the setup of boundary conditions is fundamental to obtain accurate results in FEA simulations, in this study the cooling condition is considered as a forced-liquid cooling mechanism and the corresponding heat transfer coefficient of $h = 3000\ (Wm^{-2}K^{-1})$ is applied. Figure 5.3 illustrates the detailed temperature distribution of IGBT module.

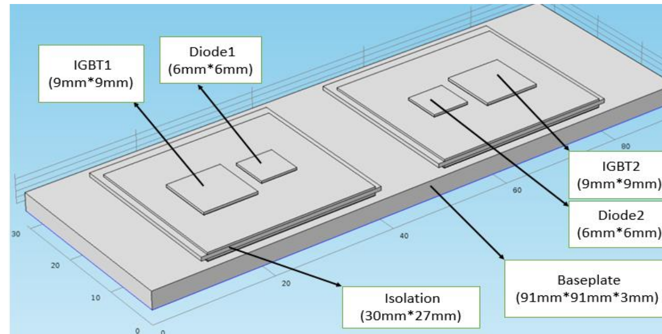


Figure 5.2 Internal structure of power module: detailed 3D FEA model.

Table 23 Dimension and Material Properties of the IGBT Module [189]

Material	Thickness $, t, (mm)$	Area$(L * W)$, $(mm * mm)$	Density, $\rho, kg/m^3$	Specific heat capacity,c, $J/(kg.K)$	Thermal Conductivity, $k, W/(m.K)$
IGBTs(Si)	0.4	9*9	2329	700	140
Diodes(Si)	0.4	6*6	2329	700	140
Solder1	0.053	As chips	0.053	As chips	35
Copper layer1	0.35	28*25	8700	385	360
Ceramic (Al_2O_3)	0.636	30*27	3260	740	100
Copper layer2	0.35	28*25	8700	385	360
Solder2	0.103	28*25	9000	150	35
Baseplate(Cu)	3	91*31	8700	385	280
Thermal grease	0.1	91*31	1180	1044	1

In the IGBT module heat flows from the operating semiconductor device to the baseplate. The hottest spot temperature is noticed around the centre of the top surface of the IGBT chip with the applied power dissipation of 110W. The fixed temperature boundary at the bottom of the baseplate is applied and the baseplate temperature is set to $32.85°C$ for each simulation adapted from [189]. The estimated thermal resistance of the IGBT from the simulation results is equal to $R_{th} = 0.3645°C/W$. The thermal resistance value derived from FEA is well congruous with the value derived from the manufacturer datasheet (see Figure 5.4) $0.3°C/W$ [190]. Similarly, power dissipation equal to 60W is applied in the diodes. The results show

that thermal resistance of the diode is equal to $R_{th} = 0.632°C/W$. This value agrees well with the value derived from the manufacturer datasheet $0.6°C/W$ [190]. The FEA obtained thermal resistance of both IGBT and diode is comparatively little higher than the datasheet thermal resistance. The variation can be attributed to the fact that the measurement boundary conditions have not been applied accurately since the datasheet does not reveal too much information about this. It can be seen that using this FEA derived thermal resistance the temperature calculation error for IGBT and diode is within 10.77% and 2.55% respectively. Therefore, the accuracy of the FEA simulation is quite acceptable which can be applied to the transient thermal analysis of the component interaction in an inverter for further analysis by combining accurate cooling boundary conditions.

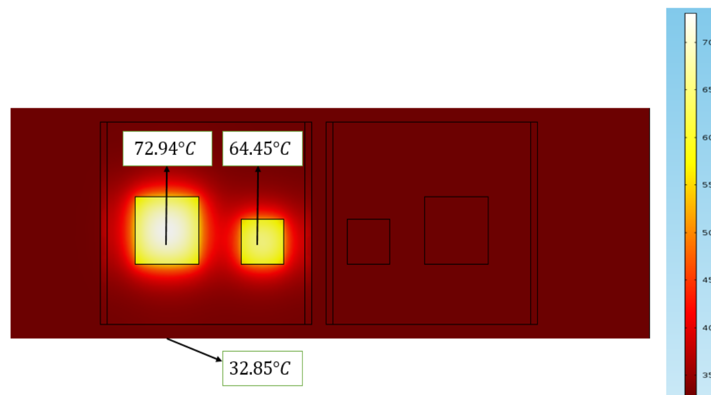


Figure 5.3 Temperature distribution of studied IGBT module.

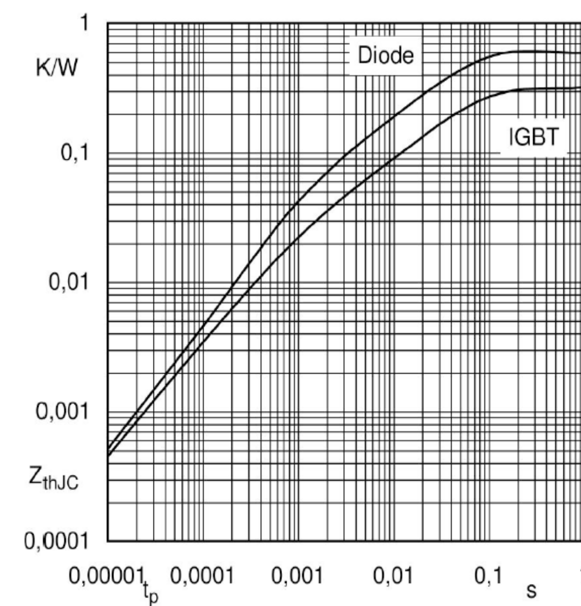


Figure 5.4 Manufacturer provided transient thermal impedance curve of IGBT module [190].

5.4 Analysis of Thermal Interactions of Multichip Power Module

Since the FEA (thermal model) derived thermal impedance value of the power module conforms close to the thermal impedance value of the manufacturer provided datasheet, the component interaction can be investigated by adding the heatsink model. To make the modelling simple, instead of building the whole model only the half bridge module component-IGBT and diode connected with the liquid cooled heatsink model is considered. In Figure 5.5, the inverter structure is presented. The 3-D CAD model of the inverter is constructed using three-half bridge modules. For the sake of reducing the computational load in meshing and solving it fast the model has been simplified and constructed by eliminating unnecessary parts such as the DC link busbar, PWM generator and the external insulating cover of the power module etc. Self-heating and cross-heating effects are predominant in the inverter components. Self-heating occurs due to its own power dissipation whereas cross-heating occurs due to adjacent components power dissipation. To apply the behavioural based RC type network model for analysing the thermal performance of the inverter, the applied techniques to evaluate these two types of coupling effects will be highlighted in this section.

There are three half-bridge power modules in the inverter as it is shown in Figure 5.5 and each half bridge module contains two IGBTs and two antiparallel diode chips. Each half bridge represents a phase of the inverter. Since the thermal parameters of the three half-bridge power modules are identical, the power module of Phase A is taken as an example for analysing the thermal coupling effect. As the inverter contains six IGBTs and six diodes, the chips in one power module can be represented as #1 top-side IGBT S1, #2bottom-side IGBT S2, #3top-side diode and #4 bottom-side diode. In Figure 5.5, top side chips are IGBT, S1 and diode, D1 while bottom side chips are IGBT, S2 and diode, D2.

It has been assumed that chips in either top-side or bottom-side will dissipate heat simultaneously. Since the symmetry is seen in top-side IGBT, the self-heating and mutual heating effects which will be discussed are all based on top-side components.

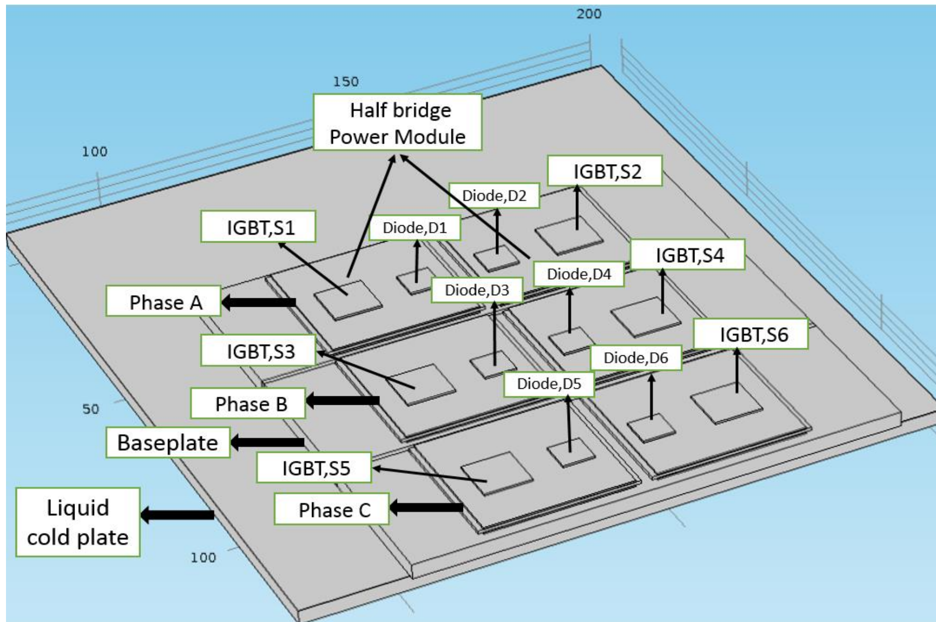


Figure 5.5 3D cad model of the whole inverter.

The temperature rises can be observed in the adjacent diode chip (D1) beside IGBT (S1) in phase A (the same half bridge module). The main reason is that chip S1 and D1 is mounted on to the same substrate which is also connected to the same baseplate of the power module in the system. So, when power dissipation is applied in one chip, the heat starts to flow to the substrate and to baseplate through conduction and thermal spreading. As a result, the neighbouring chip gets thermally hotter. This way of heating up is termed as the mutual thermal cross-heating effect.

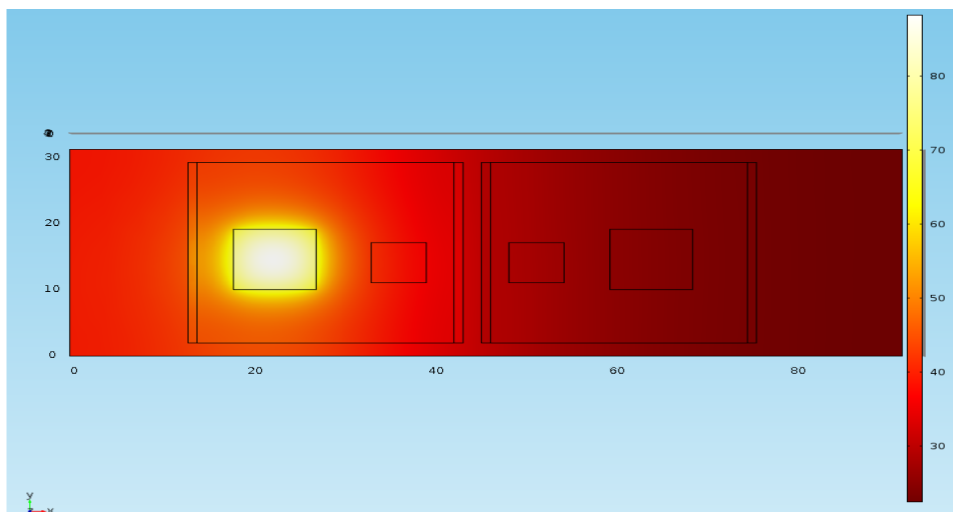


Figure 5.6 Temperature distributions when IGBT chip dissipation is 110W.

Since the thermal coupling effect is inevitable in the adjacent chip, approaches to consider it in the thermal model need to be focused on. Assuming the linear heat conduction in the power module, the model has been developed considering the thermal cross-coupling effect. The developed model considers the mutual-heating impedance and linear superposition. In this thesis linearity of the system has been applied in modelling assuming the linear heat transfer in power module and the performance of assumption of linearity property will be further investigated later in detail.

Two components including both IGBT and diode chips exist in the considered half-bridge module. Due to symmetry, the first component is analysed. The self-heating and mutual-heating thermal impedances can be estimated as it is shown in Figure 5.7.

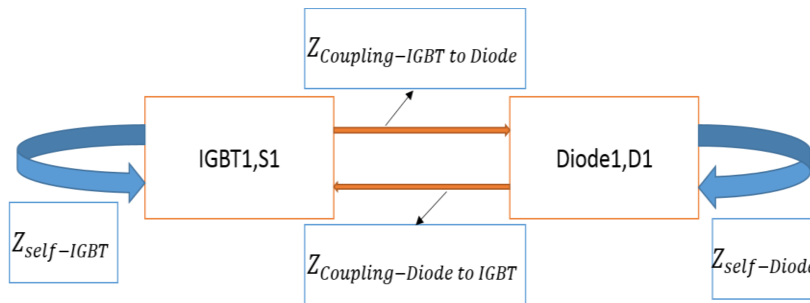


Figure 5.7 Impedance model descriptions due to self-heating and cross-heating effect.

Then the total junction temperature rise of chip IGBT (S1) can be calculated by applying a linear superposition of the temperature rise caused by all the adjacent heat sources around this chip in the half-bridge power module. In this case, diode (D1) is close to the IGBT (S1).

If there is m number of components, n number of heat sources, mathematically temperature rise can be expressed as:

$$\Delta T_m = \sum_{n=1}^{2} Z_{mn} P_n \quad \text{(5.1)}$$

where

P_n is the total power dissipation on chip $\#n$, and Z_{mn} represents the impact of the chip $\#m$ on the chip $\#n$, when $m = n$, Z_{mn} represent the self-heating thermal impedance and when $m \neq n$, Z_{mn} represent the mutual-heating thermal impedance.

In this thesis, mutual heating thermal impedance has been calculated by applying power dissipation to IGBT and recording the thermal step responses of diode chip. The temperature

rises of all the critical layers of the diode chip when IGBT (S1) is powered are shown in Figure 5.6. As per the explanation, the highest temperature rise has been observed in IGBT (S1) itself. Meanwhile, considerable amount of temperature rise has been noticed in adjacent one diode (D1) because it is nearest to IGBT (S1). Temperature rise for IGBT (S2) and diode (D2) are identical and temperature rise is not significant because they are far and not mounted on the same substrate as D1.

5.5 Thermal Interaction Model

In order to ensure the accuracy of temperature prediction at the critical layers of the packages, the RC circuit based thermal model needs to be constructed accurately. It is highly required to represent the self-heating and cross-coupling effects from other chips. Typically, this model should satisfy the superposition principle. To achieve this aim, Foster type lumped RC network parameters are extracted to model the self-heating effects for each targeted location on the chips. The extracted RC network parameters represent the thermal branches starting from the chip to the cooling system including the critical layers, for example, solder layers. On the other hand, cross-coupling effects are included in the coupled model by considering the adjacent one with the self-heating models. This additional thermal network of the adjacent one represents the coupled thermal impedance between two chips. The power dissipation of the adjacent one is included in the thermal network as the heat source. For example, to model the thermal coupling effect, the IGBT is represented by the network which includes the self-heated power dissipation that comes from the electrical model and its corresponding thermal equivalent network layers and in conjunction with this the diode model is connected. To predict temperature in a diode, the thermal model is represented by diode power losses and by its corresponding thermal equivalent network layers. Diode power losses are applied to the diode model as heat source to investigate the mutual thermal coupling effects.

FEA simulations have been performed twice to obtain the thermal responses due to self-heating and cross-heating in the IGBT-diode pair. In the first simulation, only the IGBT is active and in the second, only the diode is active. From the results, the self-heating and cross-heating thermal impedance response curves at the selected thermal network nodes are derived. These selected nodes correspond to the locations at the top and bottom of the chip as well as material interfaces. These nodes that correspond to the top of the chip, the interface of chip and chip solder, the interface of substrate solder and baseplate, the bottom of the baseplate are denoted by letters *‘p’*, *‘q’*, *‘r’* and *‘s’* respectively (see Figure 5.8). Lower

subscript *'I'* and *'D'* denote the IGBT and diode respectively. In the following, the upper subscript *'j'*, *'cs'*, *'bs'* and *'b'* respectively denote the junction, the chip solder, the baseplate solder and the baseplate layers respectively and the temperatures at these selected locations for the IGBT and diode are T_{jIp}, T_{jDp}, T_{csIq}, T_{csDq}, T_{bsIr}, T_{bsDr}, T_{bIs} and T_{bDs} respectively.

The thermal impedance matrix considering the self-heating and cross-coupling effects can be expressed as (5.2) [108], [191-192].

$$\begin{bmatrix} T_{1(t)} \\ T_2(t) \\ \cdots \\ T_k(t) \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1l} \\ Z_{21} & Z_{22} & \cdots & Z_{2l} \\ \cdots & \cdots & \cdots & \cdots \\ Z_{k1} & Z_{k2} & \cdots & Z_{kl} \end{bmatrix} * \begin{bmatrix} P_1 \\ P_2 \\ \cdots \\ P_l \end{bmatrix} + \begin{bmatrix} T_{ref,1} \\ T_{ref,2} \\ \cdots \\ T_{ref,k} \end{bmatrix} \quad (5.2)$$

where

T_p , with $p \in 1, \dots \dots \dots \dots \dots \dots, k$ is the monitoring point temperature, P_q , with $q \in 1, \dots \dots \dots \dots \dots \dots, l$ is the power losses on each chip, $T_{ref,k}$ is the reference temperature at the monitoring point k and Z_{kl} is the coupling thermal impedance between the monitoring point k and the reference point l. In particular, Z_{pp} is the self-heating thermal impedance.

The expanded from of equation (5.1) to the 3D thermal network can be written as equation (5.2), where temperature at the junction, at the chip solder, at the baseplate solder and at the baseplate in both chip IGBT and diode can be calculated using the 3D thermal network.

In matrix form, the relationship between power losses and the IGBT and diode temperatures can be written as

$$\begin{bmatrix} T_{j-I} \\ T_{j-D} \end{bmatrix} = \begin{bmatrix} Z_{thI}^{self} & Z_{thI-D}^{cross} \\ Z_{thD-I}^{cross} & Z_{thD}^{self} \end{bmatrix} * \begin{bmatrix} P_{losses-I} \\ P_{losses-D} \end{bmatrix} + \begin{bmatrix} T_a \\ T_a \end{bmatrix} \quad (5.3)$$

where, T_{j-I} and T_{j-D} are the junction temperature in IGBT and diode respectively, Z_{thI}^{self} and Z_{thD}^{self} are the total self-heating thermal impedance of the IGBT and diode respectively, Z_{thI-D}^{cross} and Z_{thD-I}^{cross} are the total cross-heating thermal impedance of IGBT-diode and diode-IGBT respectively, $P_{losses-I}$ and $P_{losses-D}$ are the losses in IGBT and diode respectively and T_a is the ambient temperature.

The self-heating impedances of the IGBT and the diode can be expressed by Equation 5.4 and Equation 5.5 respectively and the cross-coupling impedances are expressed by Equation 5.6

and Equation 5.7 respectively. The meanings of the impedances are explained in Figure 5.8 and are listed in Table 24.

$$Z_{thI}^{self} = Z_{thI}^{j-cs} + Z_{thI}^{cs-bs} + Z_{thI}^{bs-b} + Z_{thI}^{b-h} \quad (5.4)$$

$$Z_{thD}^{self} = Z_{thD}^{j-cs} + Z_{thD}^{cs-bs} + Z_{thD}^{bs-b} + Z_{thD}^{b-h} \quad (5.5)$$

$$Z_{thI-D}^{cross} = Z_{thI-D}^{j-cs} + Z_{thI-D}^{cs-bs} + Z_{thI-D}^{bs-b} + Z_{thI-D}^{b-h} \quad (5.6)$$

$$Z_{thD-I}^{cross} = Z_{thD-I}^{j-cs} + Z_{thD-I}^{cs-bs} + Z_{thD-I}^{bs-b} + Z_{thD-I}^{b-h} \quad (5.7)$$

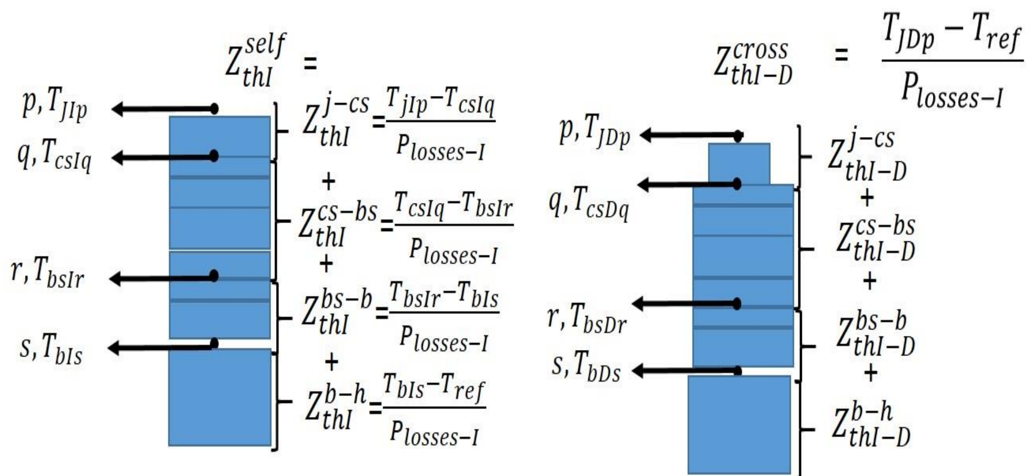


Figure 5.8 The total IGBT self-heating and diode cross-heating thermal impedances and the impedances for the material layers.

Table 24 Thermal impedance symbols.

Symbols	Meaning
$Z_{thI}^{j-cs}, Z_{thD}^{j-cs}$	Self-heating impedance of IGBT and diode between junction and chip solder
$Z_{thI}^{cs-bs}, Z_{thD}^{cs-bs}$	Self-heating impedance of IGBT and diode between chip solder and baseplate solder
$Z_{thI}^{bs-b}, Z_{thD}^{bs-b}$	Self-heating impedance of IGBT and diode between baseplate solder and baseplate
$Z_{thI}^{b-h}, Z_{thD}^{b-h}$	Self-heating impedance of IGBT and diode between baseplate and heatsink
$Z_{thI-D}^{j-cs}, Z_{thD-I}^{j-cs}$	Cross-heating impedance of IGBT-diode and diode-IGBT between junction and chip solder

$Z_{thI-D}^{cs-bs}, Z_{thD-I}^{cs-bs}$	Cross-heating impedance of IGBT-diode and Diode-IGBT between chip solder and baseplate solder
$Z_{thI-D}^{bs-b}, Z_{thD-I}^{bs-b}$	Cross-heating impedance of IGBT-diode and Diode-IGBT between baseplate solder and baseplate
$Z_{thI-D}^{b-h}, Z_{thD-I}^{b-h}$	Cross-heating impedance of IGBT-diode and Diode-IGBT between baseplate and heatsink

The method adopted in deriving thermal network parameters is based on the obtained transient thermal profile from FEA analysis by using step power losses. The transient thermal step responses are converted into transient thermal impedance curves to obtain foster RC equivalent thermal network parameters for the corresponding thermal branches between two consecutive layers.

To obtain the thermal responses, modelling has been performed applying the step power loss inputs individually to each chip named IGBT and diode as S1 and D1 respectively and the transient thermal responses for the desired monitoring points are also recorded. If the self-heating effect on the intended monitoring point is to be analysed, a step response curve is generated, and the generated curve is further processed to derive the equivalent RC thermal network. The superposition principle considering the summation of transient thermal impedance due to both the self-heated and cross-heated coupling from the adjacent chip (considered as another heat source) can be applied for analysing the thermal coupling effect for one node. The step by step process of synthesising thermal network equivalent parameters from the thermal response of the IGBT module is outlined in the following:

- The first step is to build the geometry of the real converter component model in the FEA environment
- For constructing the thermal impedance matrix, step power loss is applied as a constant heat source on a single chip for certain periods and thermal responses on all other intended points on the adjacent chip are monitored. The transient thermal response curves are produced in the form of a series of curves at each interested point on the layer. This step response process is illustrated in section 5.6.
- For extracting the thermal impedance of the specific thermal branch between two layers due to the self-heating effects, the two consecutive vertical points are chosen. The chosen points cover the branches of the junction to chip solder, chip solder to DBC, DBC to baseplate and baseplate to heatsink. To obtain the self-heating transient

thermal impedance between two layers, the obtained temperature curves are subtracted from the adjacent vertical points and divided to the applied same amount of chip power dissipation as heat source. To illustrate the self-heating thermal impedance between junction and solder can be estimated as:

$$Z_{thI}^{j-cs} = \frac{T_j^{Itp1} - T_{cs}^{Itp2}}{P_{losses-IGBT}} \quad (5.8)$$

where, T_j^{Itp1} is the IGBT junction temperature at the intended monitoring point $tp1$ on the IGBT chip, and T_{cs}^{Itp2} is the chip solder temperature in the corresponding monitoring layer at the point $tp2$ and $P_{losses-IGBT}$ is the step power losses of IGBT chip.

- To calculate the coupling transient thermal impedance, the temperature difference between junction and solder on each monitoring point of a chip is recorded, when the step power loss is applied to other chip. Then the temperature difference will be divided to power losses of the other chip. The thermal coupling between IGBT and diode, the temperature rise in the junction and chip solder of diode at the intended monitoring point is recorded and subtracted from each other and later divided to the power losses dissipated in IGBT chip. The impedance generated in this way is called coupled impedance of IGBT to diode due to power losses in IGBT. This can be expressed as the following:

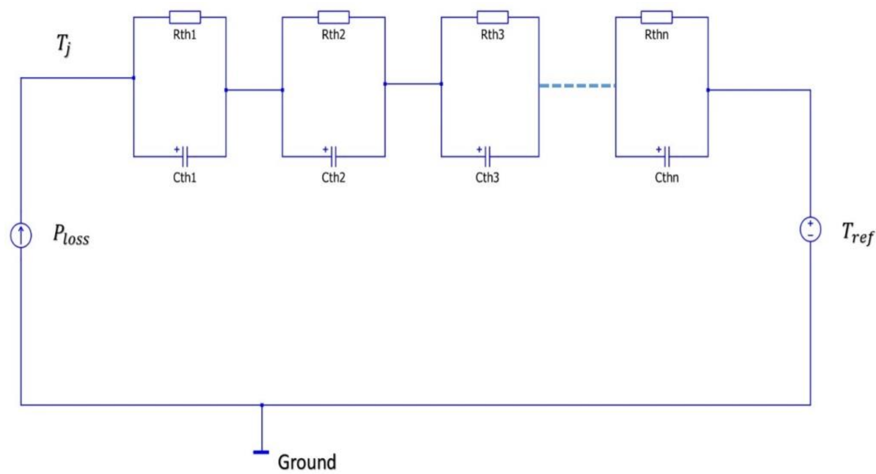
$$Z_{thI-D}^{cross} = \frac{T_j^{Dtp1} - T_h^{Dtp2}}{P_{losses-IGBT}} \quad (5.9)$$

where, T_j^{Dtp1} is the diode junction temperature at the intended monitoring point $tp1$ on the diode chip and T_h^{Dtp2} is the diode heatsink temperature in the corresponding monitoring layer at the point $tp2$ and $P_{losses-IGBT}$ is the step power losses of IGBT chip.

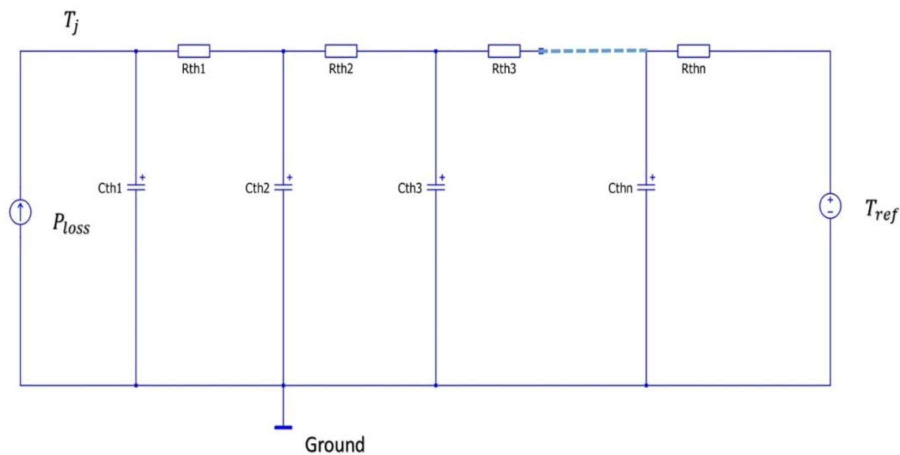
- In order to calculate the temperature from the electro-thermal model developed in the circuit simulator, the transient thermal response curves in each layer of interested point are curve-fitted mathematically to the equation expressed as sum of exponential functions represented in equation 4.58 with a view to extracting an equivalent thermal network to the thermal impedance curve

The Foster equivalent thermal network model, which is shown in Figure 5.9(a), is the most popular method due to its applicability. Its parameters are easy to be extracted from FEA derived data. Each layer in the IGBT module is represented by three RC Foster cells. It is

worth noting that in the Foster network model the voltages at the in-between nodes do not have physical meaning. However, the first and last nodes are meaningful to the adjacent temperature observation points. The RC pairs have been extracted up to the third order to guarantee the accuracy of the fitted $Z_{th}(t)$ curve. It is also clear that although the represented Foster network node voltages do not have any physical meaning, the first and the last nodes are positioned in sub-layers of the thermal network, therefore, they do represent the junction temperature and the reference temperature respectively. The Foster network can be transformed to a Cauer network as shown in Figure 5.9(b).



(a)



(b)

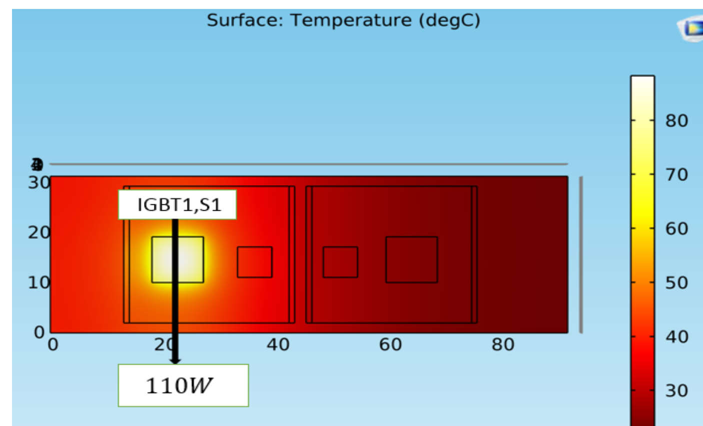
Figure 5.9 The structure of (a) the electrical equivalent Foster network (b) the electrical equivalent Cauer network.

5.6 FEA Thermal Analysis

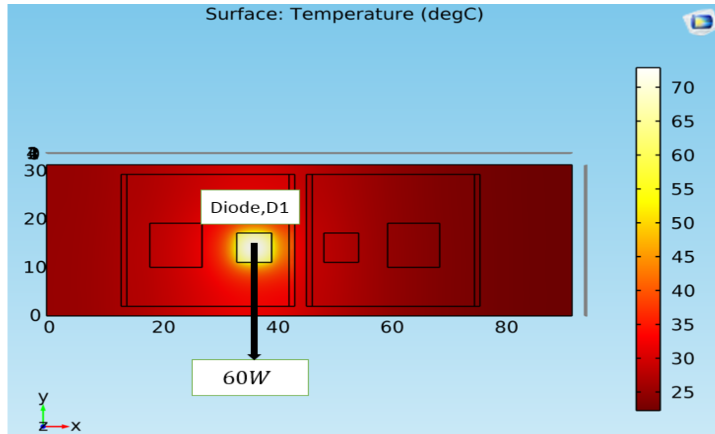
To describe self-heating and cross-heating effects, FEA simulations are performed twice. In the first simulation, IGBT (S1) is heated, and the next one, only diode (D1) is heated. The power losses applied in IGBT and diode are 110W and 60W respectively adapted from [189]. The baseplate is connected to the liquid-cooled cold plate. In this case, water is considered as circulating fluid. Therefore, convective boundary conditions of $h = 3000\, W/(m^2.K)$ is applied at the bottom of the baseplate. Also, reference temperature is set to be 20°C at the bottom of the baseplate. The temperature distributions of all other chips are shown in Figure 5.10. The temperature rises can be monitored at all the chips because of cross-heating effects.

The recorded temperature versus time data is further post-processed to obtain the transient thermal impedance curves for an interested layer. The corresponding transient thermal impedance curves are fitted to the step response equation to obtain the foster thermal parameters. It can be noticed that there is a delay for the cross-heating impedances at the beginning. That is because the chips share the same substrate and baseplate and it takes time for the heat to spread into the adjacent chips.

To obtain the thermal impedance curves of other components say for IGBT2 and diode2 the similar approach can be applied.



(a)



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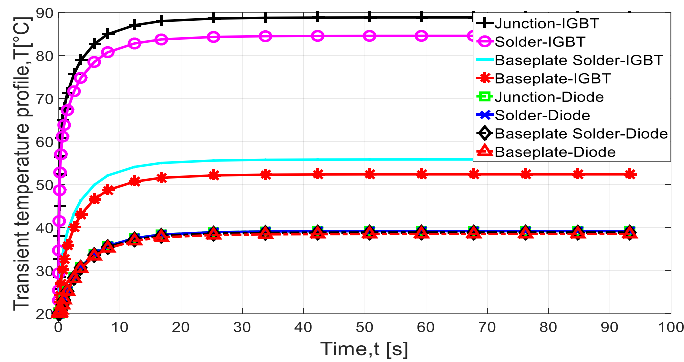

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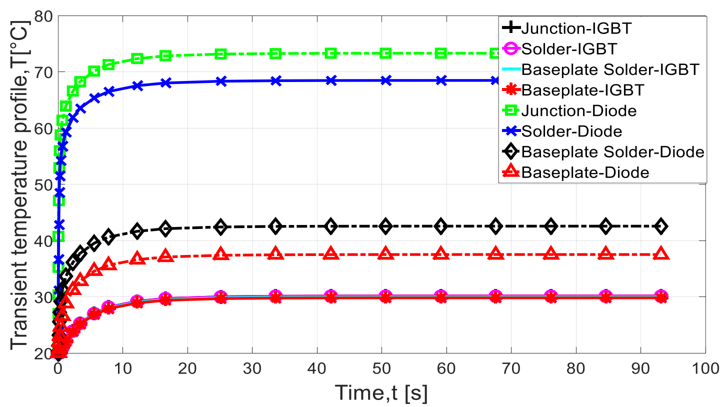
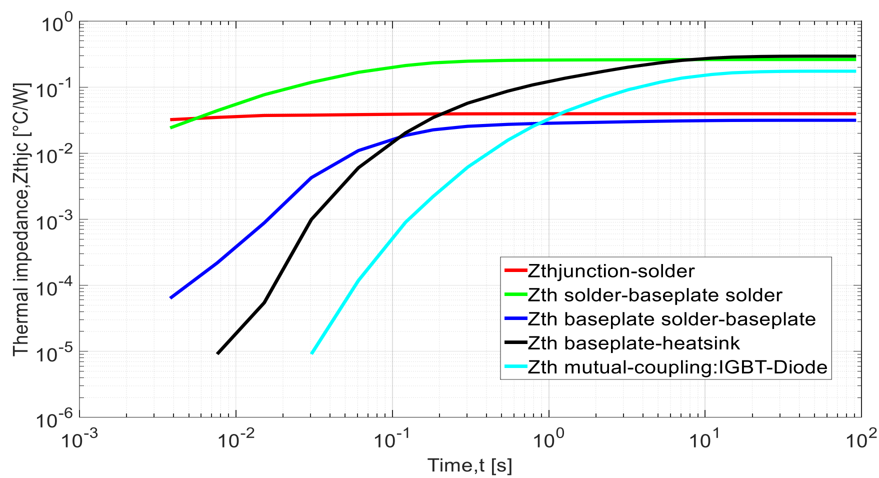


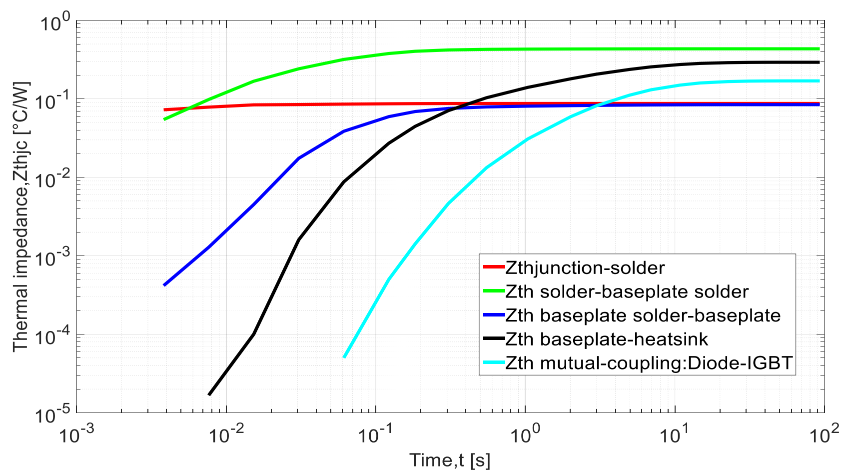
(d)

Figure 5.10 (a) Temperature distribution at t=100s. A power loss of 110W is applied to the IGBT chip (b) Temperature distribution at t=100s. A power loss of 60W is applied to the Diode chip (c) Transient temperature response of IGBT (d) Transient temperature response of Diode.

The obtained temperature responses are converted to thermal impedance curves by using Equation 4.56 and Equation 4.57 respectively as described in section 4.7.5. The self-heating thermal impedance due to power dissipation by itself can be calculated as shown in Figure 5.11(a). Similarly, the mutual-heating thermal impedance can be calculated as shown in Figure 5.11(b). As shown in Figure 5.11 (a) and 5.11(b), it can be noticed that the chip temperature reaches stability at 100s due to the large thermal inertia contributed by the cold plate. For the mutual-heating thermal impedances, a time delay occurs in temperature rise at the beginning because the self-heated chip shares the same DCB layer and time delay also occurs in heating the unheated chips by mutual-heat coupling interaction.



(a)



(b)

Figure 5.11 (a) Self-heating and mutual-heating thermal impedance when heat source is IGBT (d) Self-heating and mutual-heating thermal impedance when heat source is diode.

As has been mentioned in the section of 4.7.5 of Chapter 4, these thermal impedance curves can be fitted into foster equivalent networks by an automatic curve fitting algorithm.

5.7 Foster Thermal Network Parameters Synthesis

Parameters are extracted for both a temperature dependent thermal model and temperature independent electro-thermal model. The thermal model is built with a combination of self-heating and cross-heating thermal network. In case of self-heating, for each layer thermal network of an order of third is extracted. The thermal network contains the layers for example junction to solder, solder to baseplate solder, baseplate solder to baseplate and baseplate to heatsink. To make the analysis of thermal coupling easy and simple, a simplified thermal network is used in which the cross-heating network is modelled using the nodes at the junction and the heatsink only and the RC pairs of an order of third for this network are extracted to represent all the layers between the two nodes. The extracted parameters are listed in Tables 25-32.

It should be noted that C_{th} values for the thermal branches such as DBC solder to baseplate and baseplate to heatsink are larger than any other branches comparatively. This can be readily attributed to the fact that higher thermal mass of the baseplate and water coolant compared to than that of the other layers. The present RC compact thermal model parameters can well represent the structure of power module layers and heat flow paths in the power module more physically significant.

Table 25 Thermal parameter for the IGBT self-heating (temperature dependency)

Layer	Term number	1	2	3
Junction-Solder	R_{thi}, $°C/W$	0.0264	0.0023	0.0109
	C_{thi},$J/°C$	1.13e-34	40.86	0.4713
Solder-DBC solder	R_{thi}, $°C/W$	0.0114	0.0794	0.1708
	C_{thi},$J/°C$	112.37	0.2118	.4804
DBC solder-Baseplate	R_{thi}, $°C/W$	0.0038	6.36e-20	0.0277
	C_{thi},$J/°C$	1.0348e3	0.08	4.44
Baseplate-heatsink	R_{thi}, $°C/W$	0.0973	0.1731	0.0241
	C_{thi},$J/°C$	5.7464	22.67	435.15

Table 26 Thermal parameter for the Diode cross-heating (temperature dependency)

Layer	Term number	1	2	3
Junction-heatsink	$R_{thi}, °C/W$	0.0087	2.17e-47	0.166
	$C_{thi}, J/°C$	2.09e3	1.5e-27	25.97

Table 27 Thermal parameter for the Diode self-heating (temperature dependency)

Layer	Term number	1	2	3
Junction-Solder	$R_{thi}, °C/W$	0.0032	0.0593	0.0248
	$C_{thi}, J/°C$	29.55	8.17e-15	0.2075
Solder-DBC solder	$R_{thi}, °C/W$	0.1081	0.2131	0.1123
	$C_{thi}, J/°C$	0.1011	0.1753	1.2524
DBC solder-Baseplate	$R_{thi}, °C/W$	0.0043	2.51e-19	0.08
	$C_{thi}, J/°C$	902.18	0.0857	1.26
Baseplate-heatsink	$R_{thi}, °C/W$	3.357e-19	0.1645	0.1275
	$C_{thi}, J/°C$	1.52e-10	28.33	4.2

Table 28 Thermal parameter for the IGBT cross-heating (temperature dependency)

Layer	Term number	1	2	3
Junction-heatsink	$R_{thi}, °C/W$	0.1593	0.0062	0.0042
	$C_{thi}, J/°C$	29.1	743.8	6.93e3

Table 29 Thermal parameter for the IGBT self-heating (no temperature dependency)

Layer	Term number	1	2	3
Junction-Solder	$R_{thi}, °C/W$	0.0068	0.0278	0.0042
	$C_{thi}, J/°C$	12.05	0.077	761.1651
Solder-DBC	$R_{thi}, °C/W$	0.0861	0.1675	0.0123

solder	$C_{thi}, J/°C$	0.2004	0.5201	129.97
DBC solder-Baseplate	$R_{thi}, °C/W$	7.8076e-20	0.0268	.0037
	$C_{thi}, J/°C$	9.44e3	4.64	1.05e3
Baseplate-heatsink	$R_{thi}, °C/W$	2.84e-22	0.1044	0.1859
	$C_{thi}, J/°C$	1.32e-12	5.68	24.92

Table 30 Thermal parameter for the Diode cross-heating (no temperature dependency)

Layer	Term number	1	2	3
Junction-heatsink	$R_{thi}, °C/W$	0.1721	9.68e-19	1.56e-19
	$C_{thi}, J/°C$	26.28	3.78	0.0015

Table 31 Thermal parameter for the Diode self-heating (no temperature dependency)

Layer	Term number	1	2	3
Junction-Solder	$R_{thi}, °C/W$	0.0557	0.0021	0.0164
	$C_{thi}, J/°C$	1.81e-15	45.90	0.3599
Solder-DBC solder	$R_{thi}, °C/W$	0.2294	0.0148	0.1858
	$C_{thi}, J/°C$	0.3147	53.5	0.077
DBC solder-Baseplate	$R_{thi}, °C/W$	0.0044	0.0424	0.0371
	$C_{thi}, J/°C$	882.1	2.37	2.71
Baseplate-heatsink	$R_{thi}, °C/W$	0.0367	0.1378	0.1139
	$C_{thi}, J/°C$	256.6	25.82	4.2

Table 32 Thermal parameter for the IGBT cross-heating (no temperature dependency)

Layer	Term number	1	2	3
Junction-heatsink	$R_{thi}, °C/W$	5.12e-19	0.0044	0.1655
	$C_{thi}, J/°C$	5.26e4	6.41e3	27.97

5.8 Challenges of Linear Assumption Based Modelling

To adopt the foster network in dealing with the electro-thermal behaviour in power electronics, linearity of the foster network is assumed. However, power electronics in particular, switching components mounted either on the liquid cooled or air cooled heatsink do not behave linearly. It involves heat convection in the system which is a non-linear problem. Heat transfer in a 3D inverter introduces a 3D thermal spreading at different layers in the structure. This needs to be included in the thermal model. Otherwise, the prediction of temperature will be affected. Also, the material properties are temperature dependent. Therefore, the impact of these non-linear factors on the linear assumption of the foster network needs to be checked.

5.8.1 Validations of Linear Assumption Based Modelling

A system is said to be linear when properties of homogeneity and additivity (principle of superposition) are satisfied. In this section these two criteria will be tested based on the temperature independent material properties. The impacts of temperature on the thermal model will be further assessed in the subsection.

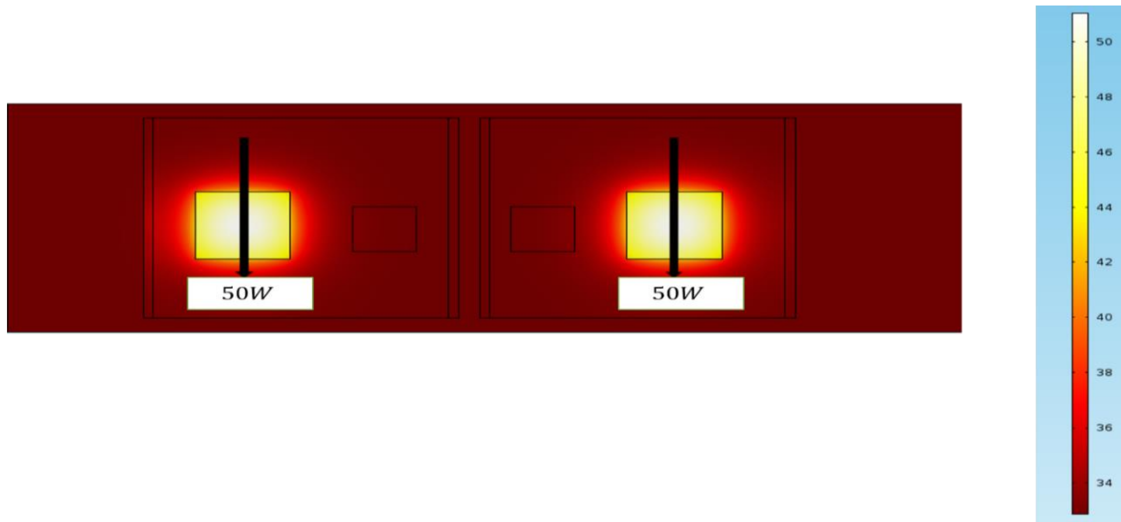
5.8.2 Proof of Homogeneity Conditions

The property of homogeneity states that for a given input $x(t)$ and any scalar C multiplied by the input function F, Equation (5.10) is satisfied.

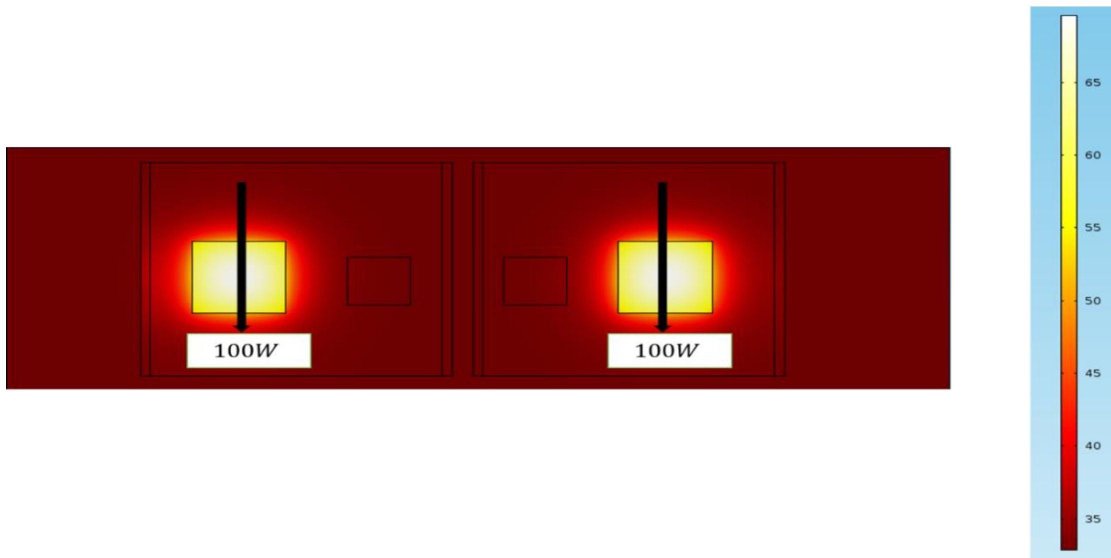
$$F(Cx(t)) = CF(x(t) \quad \text{..... (5.10)}$$

To test the homogeneity of the system, a thermal model including half-bridge module is built in COMSOL. In the modelling power losses are considered as the input and temperature rises are considered as the output. To extract temperature responses, power losses of 50W per chip and 100W per chip in both IGBT of the half-bridge module are applied respectively. The steady state temperature profile is illustrated in Figure 5.12. For the sake of comparison, two transient thermal impedances under these applied power losses are derived and plotted in Figure 5.13. It can be observed that the derived transient thermal impedance for two cases agrees well and show slight variation in the range of 0.5%. Therefore, the system can be supposed to satisfy the homogeneity property. The discrepancy may cause due to the larger power leading to generating large temperature difference between the power device and the baseplate. As a consequence, the blocking behaviour of heat in the area of junction to

baseplate leads to the rise of thermal impedance. Therefore, thermal impedance at 200W shows slight error than at 100W due to the larger amount of power losses.



(a)



(b)

Figure 5.12 Steady state temperature distribution with different power dissipation loading: (a) with 100W, (b) With 200W.

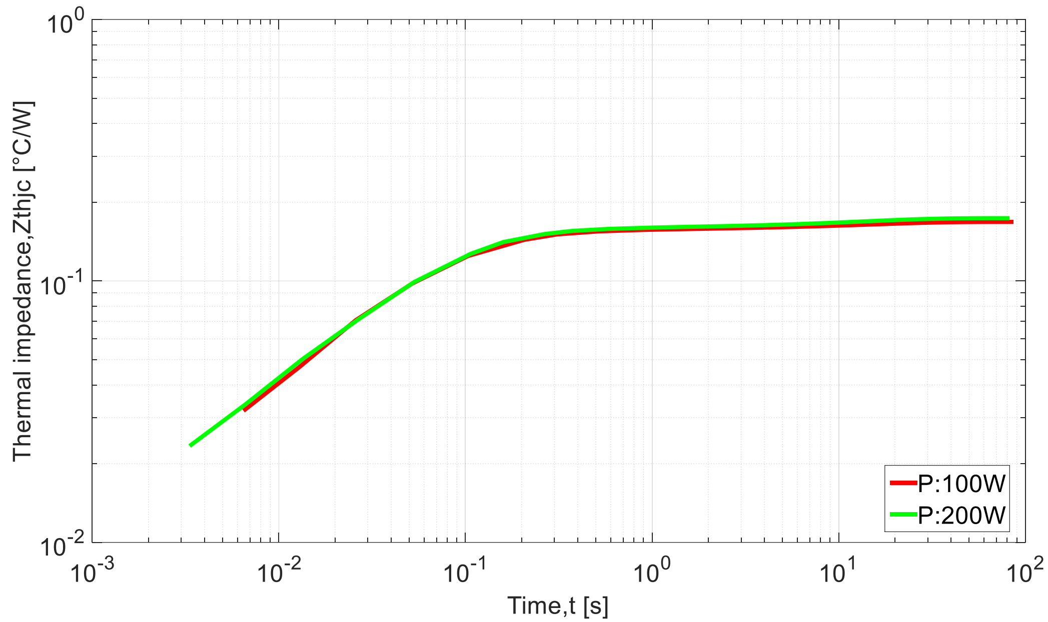


Figure 5.13 Transient thermal impedance curves with 100W and 200W power dissipations.

5.8.3 Proof of Superposition Property

The superposition property states that the response of a linear system to a sum of signals is the sum of the responses to each individual input signal.

Mathematically if input a1 produces response b1 and input a2 produces responses b2 then input (a1+a2) produces response (b1+b2). The superposition states that for different inputs, in the domain of function F, Equation (5.11) should be satisfied.

$$F(x_1 + x_2 + x_3 + \cdots + x_n) = F(x_1) + F(x_2) + F(x_3) + \cdots + F(x_n) \quad (5.11)$$

To test the superposition property, the temperature rises of IGBT (S1) is estimated due to the applied power dissipation of 110W. Similarly, the temperature rises of the diode (D1) can be estimated by applying the power of 60W in the diode chip. To obtain the transient temperature profile both in S1 and D1 respectively, FEA simulations are conducted twice. Then power dissipation of 110W and 60W is directly applied to the both chip simultaneously as shown in Figure 5.14. If the system is said to be linear in the context of superposition property, the temperature rises of the device IGBT and diode $F(x_1 + x_2)$ should be equal to the $F(x_1) + F(x_2)$. The transient temperature rise curves are extracted from FEA transient analysis as depicted in Figure 5.15. It can be observed that the temperature rise due to multiple interacting heat sources is slightly smaller than that estimated by superposition. It is worth pointing out that the discrepancy may originate from the larger thermal spreading

contributed by multiple heat source interaction and thereby result in causing larger temperature difference within increased regions and also contributing to the reduction of thermal impedance due to effective convection cooling from the cold plate to coolant. However, the error is limited to 2%, as shown in Figure 5.15. Therefore, the system can be said to be linear as it satisfies the superposition property. It can be concluded based on the verification results that the thermal model of IGBT components of multichip meets the criteria of LTI properties. Even in case of not considering temperature dependent material properties, the system can be assumed to be linear. It should be mentioned that applied cooling boundary conditions follow the linearity of heat convection.

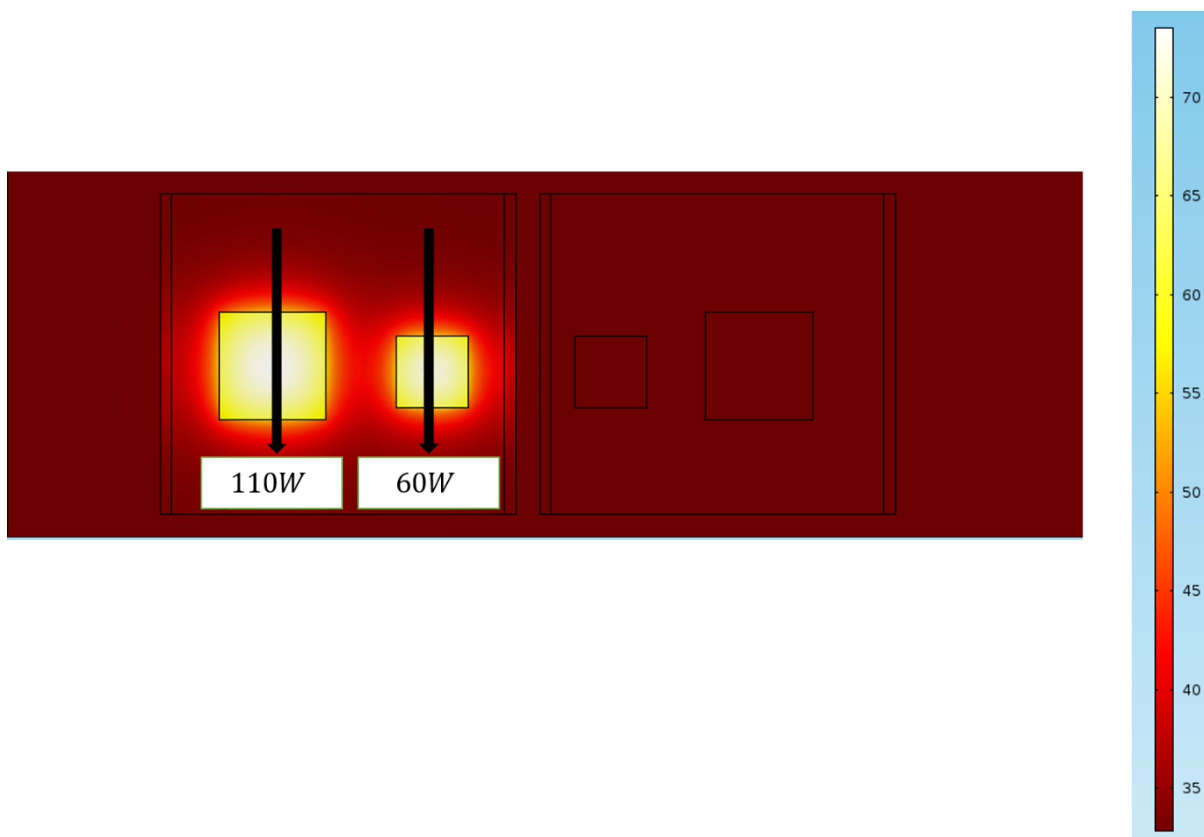


Figure 5.14 Temperature distribution profile when IGBT and diode are heated simultaneously.

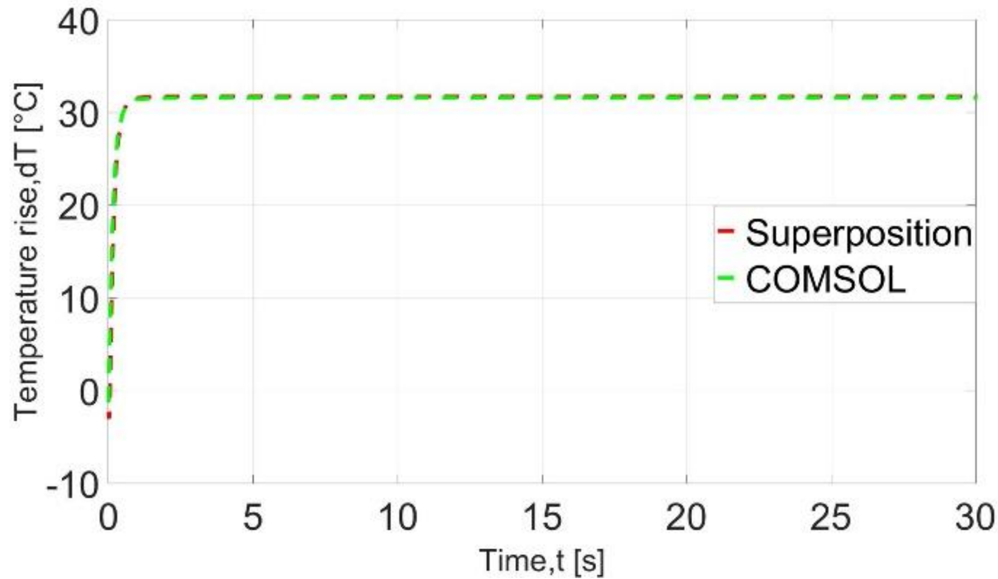


Figure 5.15 Temperature rise due to superposition.

5.9 Thermal Effects Analysis

Many issues contribute nonlinearities in the thermal model. These issues include thermal spreading, a convection cooling mechanism and temperature dependent material properties etc. The impact of first two issues has already been discussed in the previous section and the last issue will be addressed in this section.

5.9.1 Temperature Dependence of the Materials

At present, temperature effects on thermal parameters are not considered in thermal models and this leads to causing an error ranging from 4% to 12% [102], [193] .

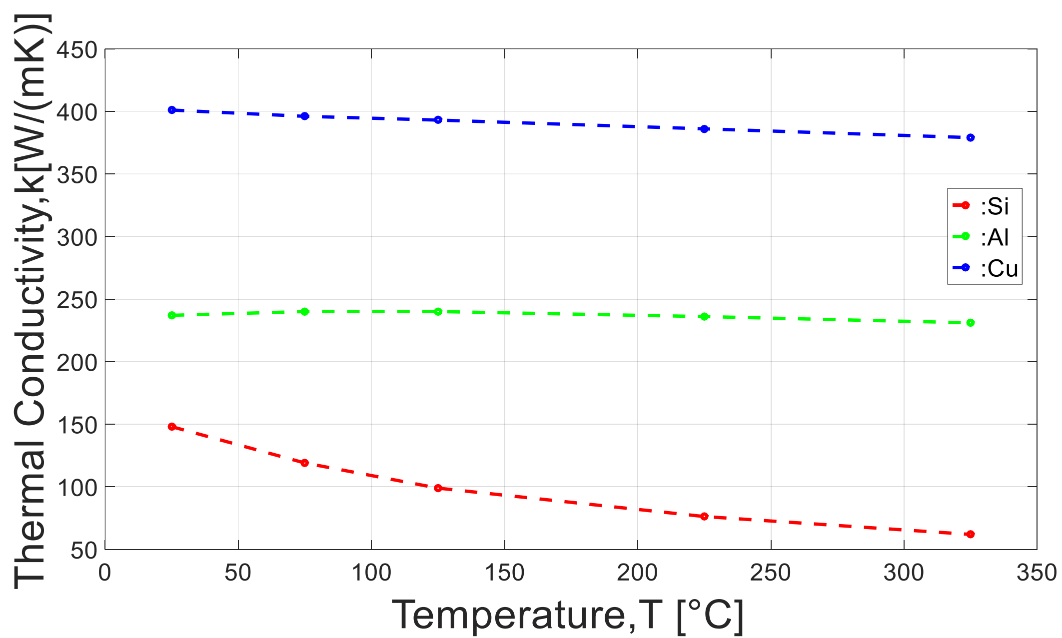
Since the variation of the density of the various materials which constitute power semiconductor devices with the relevant working temperature range (from 25°C to about 200°C) is low, the temperature dependency of heat capacity can be ignored.

In IGBT power modules the materials such as Silicon (Si), Aluminium (Al) and Copper (Cu) etc. are common. Table 33 reports the detailed information for thermal conductivity and specific heat of the materials (Si, Al and Cu) [194]. Temperature dependent material properties of Si, Al and Cu are plotted in Figure 5.16. From Table 33 and Figure 5.16, it is obvious that the decreasing trend is observed in the thermal conductivity of silicon with increasing temperature and the increasing trend is observed in the case with the specific heat capacity. According to the handbook, the thermal conductivity of silicon decreases around

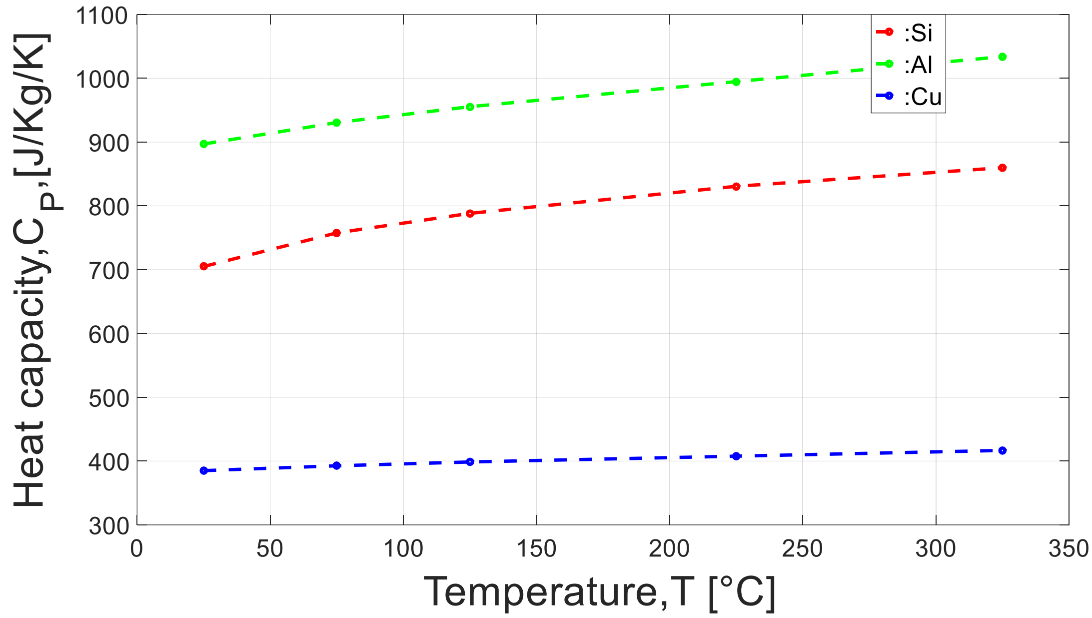
250°C almost half of the silicon thermal conductivity around 25°C [194]. Based on this, the thermal behaviour of the power module depends directly on the local temperature.

Table 33 IGBT module materials thermal properties at different temperature [194]

Temperature		$25°C$	$75°C$	$125°C$	$225°C$	$325°C$
Silicon(Si)	$Thermal\ conductivity, K, Wm^{-1}K^{-1}$	148	119	98.9	76.2	61.9
	$Heat\ capacity, C_P, JKg^{-1}K^{-1}$	705	757.7	788.3	830.7	859.9
Aluminium(Al)	$Thermal\ conductivity, K, Wm^{-1}K^{-1}$	237	240	240	236	231
	$Heat\ capacity, C_P, JKg^{-1}K^{-1}$	897	930.6	955.5	994.8	1034
Copper(Cu)	$Thermal\ conductivity, K, Wm^{-1}K^{-1}$	401	396	393	386	379
	$Heat\ capacity, C_P, JKg^{-1}K^{-1}$	385	392.6	398.6	407.7	416.7



(a)



(b)

Figure 5.16 Temperature effects on material's thermal properties (a). Thermal conductivity, (b) Specific heat capacity of Si, Al, Cu. [194].

To take into account temperature dependency in the thermal model properties like material thermal conductivity and heat capacity have been expressed as temperature-dependent expressions through curve fitting the curves of Figure 5.16. Table 34 shows the listed temperature-dependent thermal conductivity and heat capacity of the IGBT module materials.

Table 34 IGBT module materials thermal properties and heat capacity at different temperature

Material name	$Thermal\ conductivity, K, Wm^{-1}K^{-1}$	$Heat\ capacity, C_P, JKg^{-1}K^{-1}$
Silicon	$k(Si) = 148 * \left(\frac{300}{T}\right)^{1.3}\ Wm^{-1}K^{-1}$ $149.47 * \exp(-0.003 * \left(T\left[\frac{1}{K}\right]\right))[Wm^{-1}K^{-1}]$	$714.03 * \exp(0.0006 * \left(T\left[\frac{1}{K}\right]\right))[JKg^{-1}K^{-1}]$
Al	$240.63 * \exp(-1 * 10\text{^}(-4) * \left(T\left[\frac{1}{K}\right]\right))[Wm^{-1}K^{-1}]$	$895.31 * \exp(0.0005 * \left(T\left[\frac{1}{K}\right]\right))[JKg^{-1}K^{-1}]$
Copper	$402.21 * \exp(-2 * 10\text{^}(-4) * \left(T\left[\frac{1}{K}\right]\right))[Wm^{-1}K^{-1}]$	$384.4 * \exp(0.0003 * \left(T\left[\frac{1}{K}\right]\right))[JKg^{-1}K^{-1}]$

5.9.2 Influence of Temperature Dependent Material Properties on the Thermal Model

To evaluate the errors caused by avoiding the temperature dependency of thermal properties, a full non-linear thermal model is solved in COMSOL by using the temperature-dependent materials properties, i.e. thermal conductivity. The transient simulation is performed on several occasions with the changing coolant temperatures. Typically, the coolant temperature ranges from 306K (32.85°C) to 366K (92.85°C) for power electronic inverter. Initially, linear model that uses constant temperature material properties is solved at different ambient temperatures. Similarly, the non-linear model that uses temperature dependent material properties is solved with different ambient temperatures. Finally, a comparison between the linear model and non-linear model is made and results are plotted together in Figure 5.17.

As shown in Figure 5.16, since the thermal conductivity of Si decreases with the rise of ambient temperature, the thermal impedance increases. The error is found to be around 7% comparing linear model at $T_{amb} = 306K$ to the non-linear model at $T_{amb} = 366K$. This error occurs due to the temperature dependence of thermal conductivity. Therefore, if the model is solved using constant material properties at 306K, the largest error in the worst case is around 7%. The error in thermal impedance is mainly caused by the variation of the thermal conductivity of silicon and the smaller active area of silicon layer compared to aluminum layer. Therefore, the thermal resistance of the silicon layer contributes a little amount to the total thermal resistance of the entire system and its impact on the total thermal system can be considered negligible.

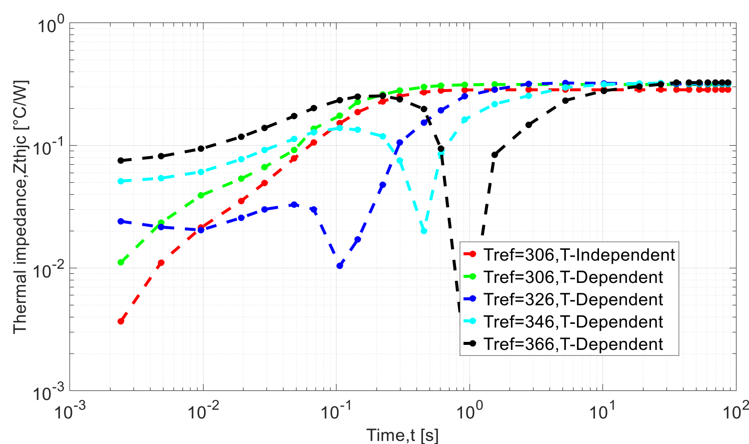


Figure 5.17 Thermal impedance curves under different ambient temperatures.

Currently, no ideal solutions to this problem exist. In order to tackle this problem, an average thermal impedances curve at various temperatures is applied to solve this. In this research, a simplified temperature dependent material property at average temperature is used. The average temperature has been calculated considering the highest junction temperature and the lowest cooling temperature. Finally, the model is solved using the material properties at this estimated average temperature. A comparison of the proposed simplified thermal model and full temperature dependent with the coolant inlet 306K and 366K is shown in Figure 5.17 compared to the worst case (the curve with the legend $T_{amb} = 366\text{K}$), the error is around 2% at 100 seconds. Therefore, by using the material properties at average temperature the error is reduced from 7% to 2%.

5.10 Thermal Model for the Component Interaction Analysis

The linearity of the thermal model of the inverter has been validated in section 5.8.1, the errors caused by the non-linear issues have also been discussed in section 5.9.2 and thus, the thermal model for the analysis of component interaction can be developed based on the behaviour based RC thermal network method.

In section 5.4, it has been mentioned that Phase A contains two IGBTs and two parallel diodes. As the devices in the module show symmetry, there will be two self-heating and mutual-thermal impedances. These thermal impedances can be obtained by repeating the simulation for two times with each chip group heated respectively. The temperature rise of any chips can be obtained by a linear superposition of all the heat sources in the same module. To simplify the problem, a 2x2 impedance matrix is used to describe the model. The modelling equations are described in section 5.4. The thermal network model of the corresponding to the thermal impedance matrix of phase A is shown in Figure 5.18.

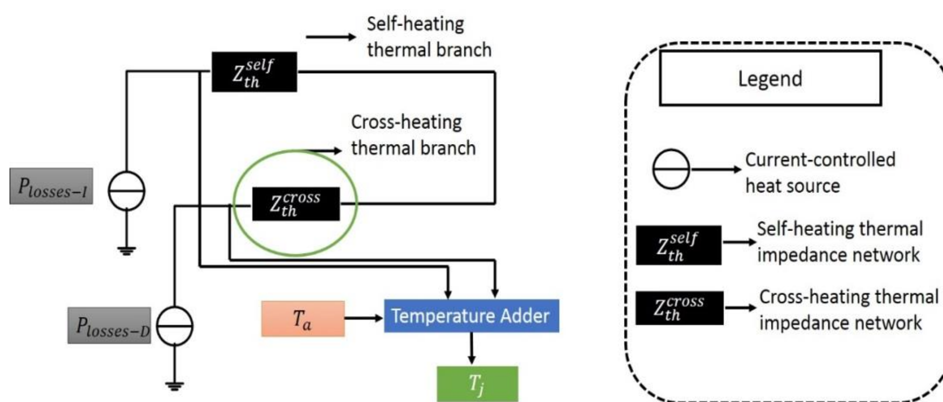


Figure 5.18 Thermal network model for phase A.

5.10.1 Inverter Electro-thermal Analysis

To develop an electro-thermal model of the Phase A switch (IGBT, S1 and Diode, D1) in a three-phase inverter, the power losses of the IGBT module are analysed and the thermal model parameters derived in section 5.7 have been used here to construct the thermal model. The inverter under study is the power rating of 7.8 kW. Table 35 summarises the inverter specifications.

Table 35 Three-phase voltage source inverter specifications

DC-link Voltage	600V
Load Current	25A
Output power	7.8kW
Modulation index	0.8
Power factor	0.8
Maximum Junction temperature	125°C
Switching frequency, f_{sw}	10 kHz
R-L Load	R-5.29**Ω**, L-13.5mH

The method detailed above has been used to analyse the thermal behaviours of an IGBT-diode pair in an IGBT module which has been used in a conventional three-phase voltage source inverter. Figure 5.19 illustrates the converter electrical circuit that is coupled to the thermal network circuit for the IGBT-diode pair.

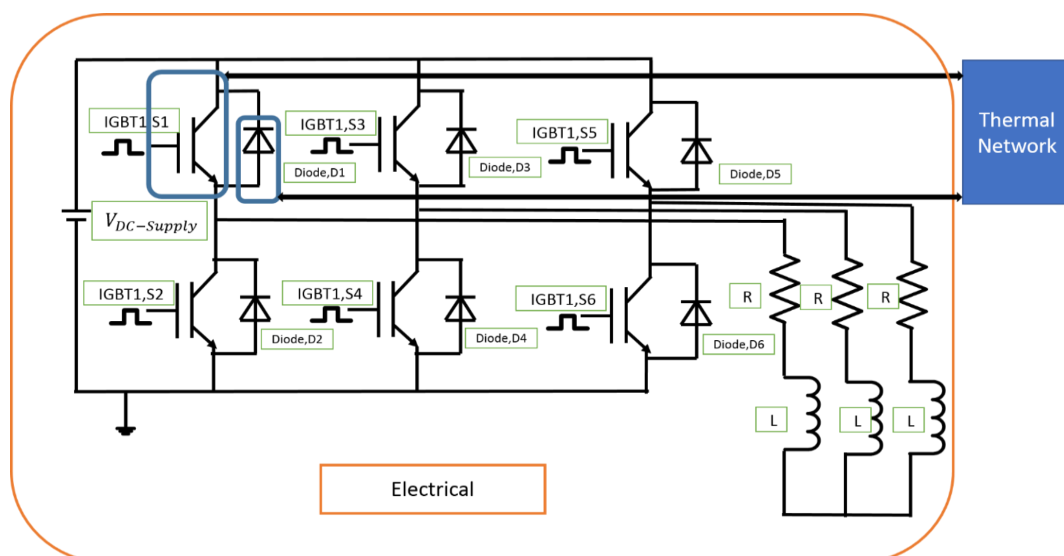


Figure 5.19 Thermal network model for phase A.

5.10.2 Power Loss Model

Two basic factors are common in building an accurate electro-thermal model of power electronic components: loss calculation and loss integration into the model represented by the self-heating and cross-heating. Therefore, it is important to model the device power losses accurately. To calculate the power losses accurately, the loss model must include detailed knowledge of power semiconductor device including forward current/voltage characteristics over a range of temperatures between 25°C-125°C and loading current waveform.

The studied inverter is composed of three power modules and one power module is selected. The module under study containing the power devices such as IGBT is subjected to repetitive turn-on and turn-off and thus, dissipates electric energy during the pulse width modulation. The total loss is estimated as the sum of conduction and switching losses.

The instantaneous power loss obtained by PLECS circuit simulation is derived from parameters, equations and look-up tables given in the manufacturer datasheet. For the IGBT, the voltage drop in the device V_{CE} can be approximated as a linear function of the collector current I_C. To take into account the temperature dependency in the model, multiple characteristics curves for a range of different operating temperatures are included to build a look-up table [195]. The voltage drop of IGBT under different temperatures is plotted in Figure 5.20. The power module investigated in this thesis is an IGBT power module, for which the voltage characteristics curves are given for $T = 25°C$ and $T = 125°C$.

Conduction power losses are estimated by multiplying the obtained voltage with the collector current. The upper switch S1 experiences the conduction losses when the line current is positive and the gate signal is 1. Similarly, the conduction losses for the anti-parallel diodes can also be obtained. The voltage drop of diode under different temperatures is plotted in Figure 5.21.

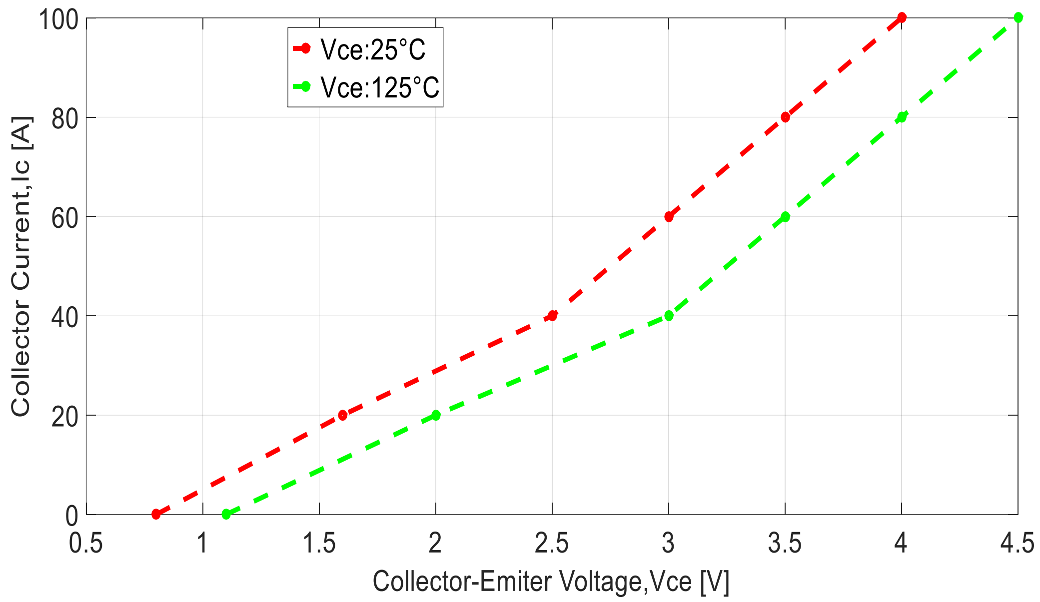


Figure 5.20 The voltage drop of IGBT under different temperatures.

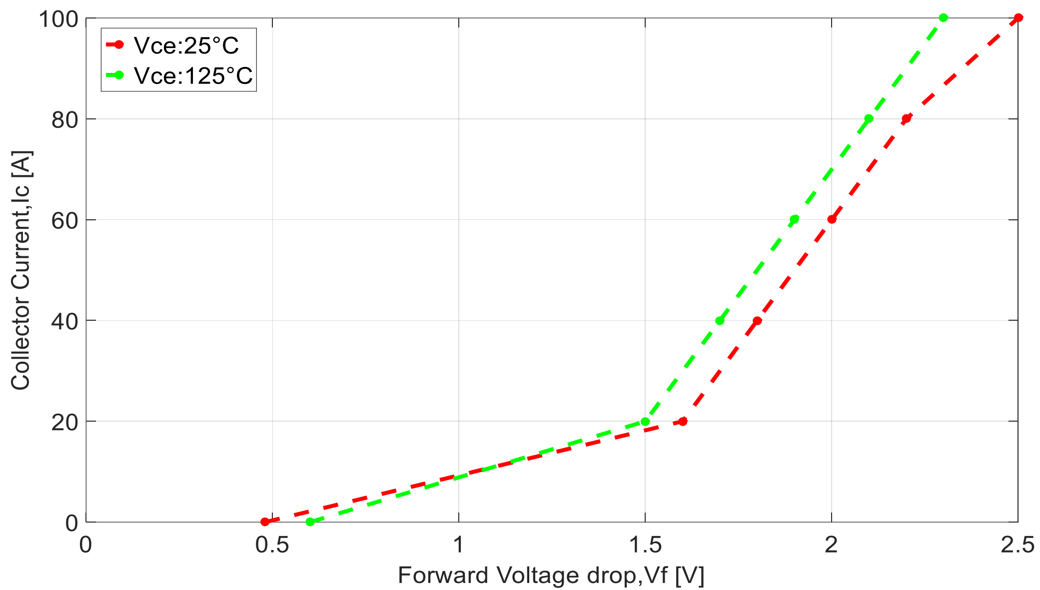


Figure 5.21 The voltage drop of diode under different temperature.

Switching losses are modelled taking into account the temperature effects on the losses due to both turn-on and turn-off switching events. To build a switching loss map in PLECS, a look-up table has been built using the given datasheet parameters describing both turn-on and turn-off energy dissipation.

As the input voltage is fixed DC link voltage 600V, switching energy dissipation of IGBT has been modelled and calculated under different currents and junction temperatures considering the 600V DC link voltage. To improve the accuracy of the loss model, other voltage is also considered. The switching energy both including turn-on and turn-off dissipation expressed as $E_{turn-on}$ and $E_{turn-off}$ respectively are shown in Figure 5.22. Switching losses are found increasing with the elevated junction temperature. As the switching losses are dependent on the factors like DC-link voltage, the current and the junction temperature, a 4-D look-up table combining these factors are required to obtain the switching loss which is not straightforward to build and computationally burdensome. To solve this problem, a simplified look-up table has been constructed considering the switching losses under different voltages, currents and junction temperatures. The whole switching losses are plotted in Figure 5.23. Under the same current and temperature, it can be noticed that the switching losses are proportional to the DC-link voltage. For example, at 25°C, the total switching loss at 1200V is around two times that at 600V. Therefore, the 3D look-up table with 600V DC-link voltage can be applied to calculate the switching loss. The total energy dissipations of IGBT at DC-link voltage can be calculated by multiplying the obtained switching losses at 300V with the coefficient $V_{dc}/600$. Similarly, the obtained reverse recovery energy dissipation under 600V is shown in Figure 5.24. The reverse recovery energy dissipation of diode at DC-link voltage V_{dc} can be calculated by multiplying the obtained E_{rec} at 600V with the coefficient $V_{dc}/600$. Therefore, by using the look-up table shown in Figure 5.24, E_{rec} at different DC-link voltages is obtained. By using the measured switching energy dissipations, the average switching loss of the IGBT and the diode can be represented as (5.12) and (5.13) respectively.

$$P_{switching\ loss-IGBT} = \frac{E_{turn-on}+E_{turn-off}}{T_s} = \left(E_{turn-on} + E_{turn-off}\right) * f_{sw} \cdots\cdots\cdots\cdots\cdots (5.12)$$

$$P_{switching\ loss-Diode} = \frac{E_{rec}}{T_s} = E_{rec} * f_{sw} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5.13)$$

Where $P_{switching\ loss-IGBT}$ and $P_{switching\ loss-Diode}$ are the switching power losses of the IGBT and the diode, respectively, T_s is the switching period.

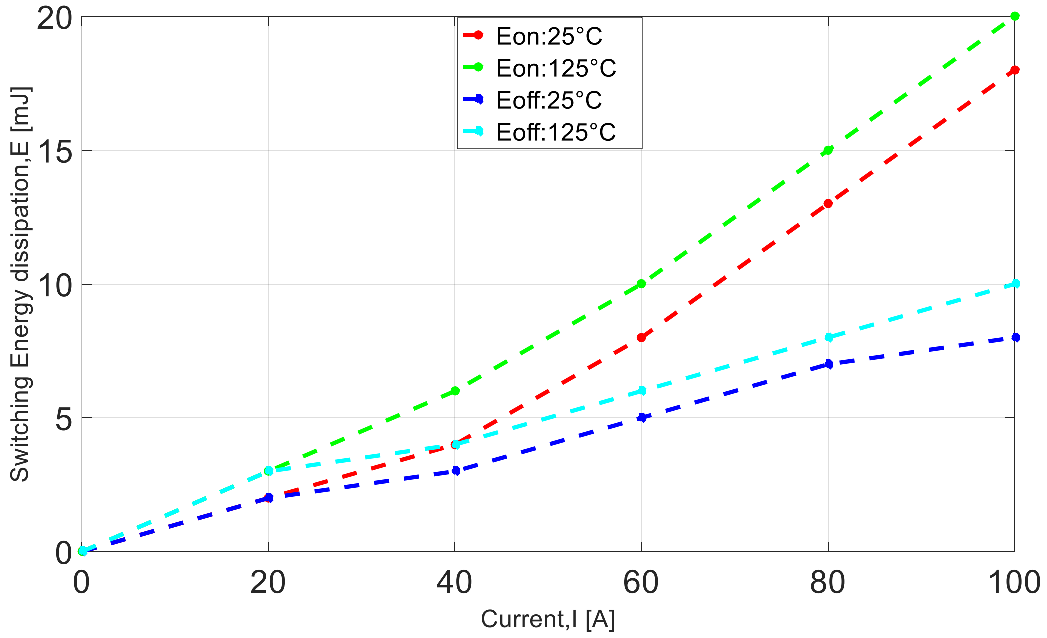


Figure 5.22 The switching energy losses of IGBT with 600V DC-link voltage.

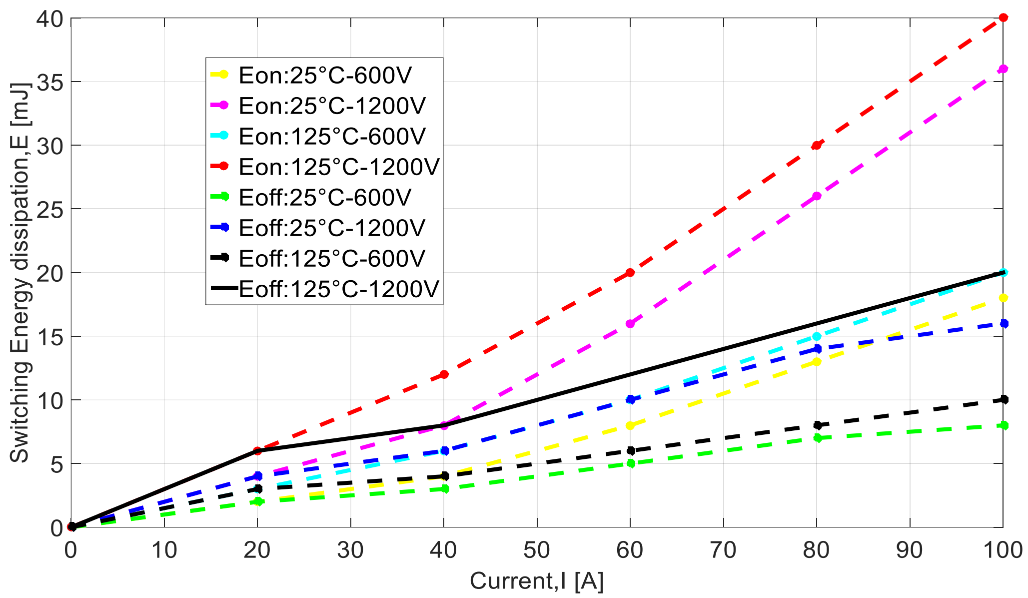


Figure 5.23 The switching energy losses of IGBT under different conditions.

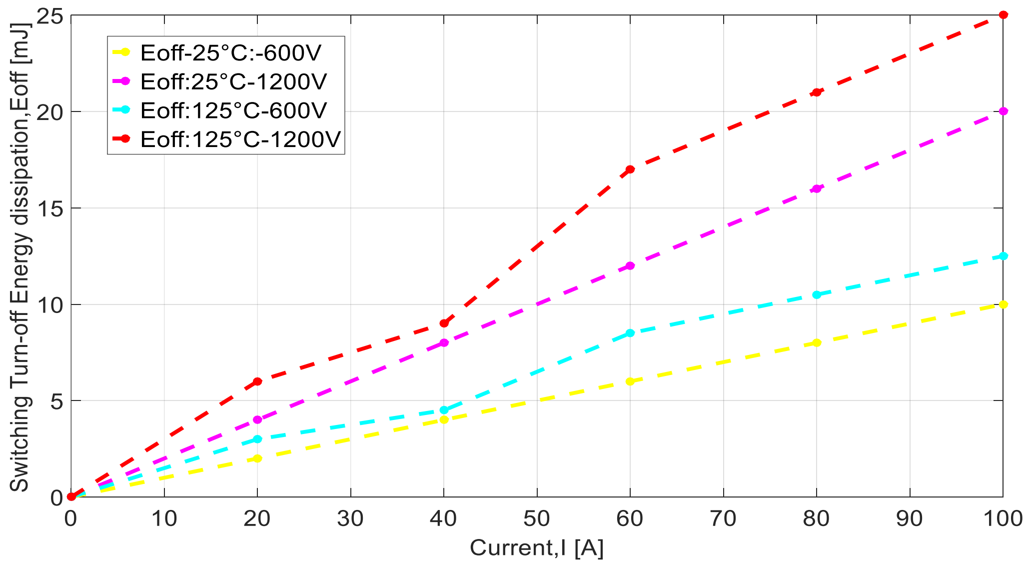
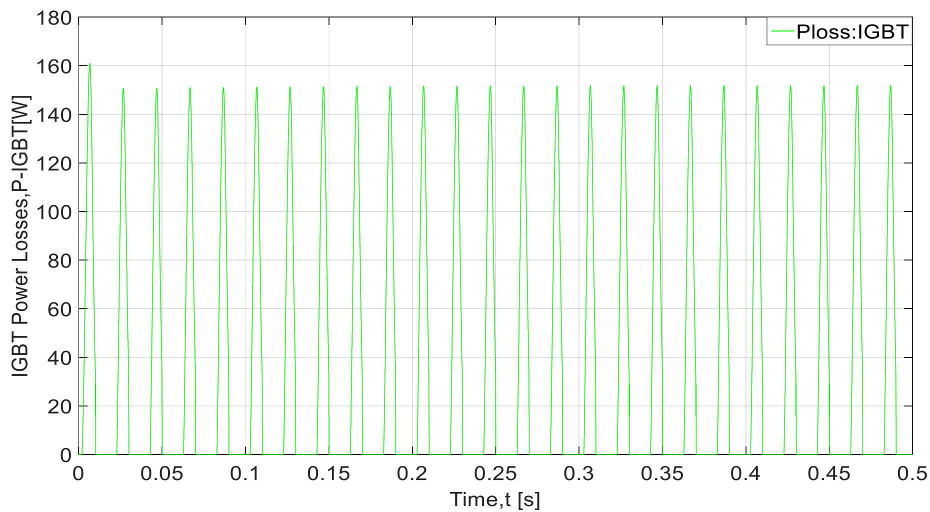


Figure 5.24 The switching turn-off energy losses of diode with different conditions.

Inclusion of a detailed switching loss model in PLECS may decrease the simulation speed. A powerful computer with high memory configuration is needed to capture the fast switching events in the power electronic switch and thereby, calculate the switching losses. To reduce computational time, time-averaged smoothed switching power loss on each switching period (described in section 4.3.3) is adopted in this present work. The equations are described in Appendix H.

Combining the loss model described above with the electrical inverter model losses in the IGBT and the diode can be estimated. Figure 5.25 shows the predicted loss profiles in the IGBT and the diode respectively.



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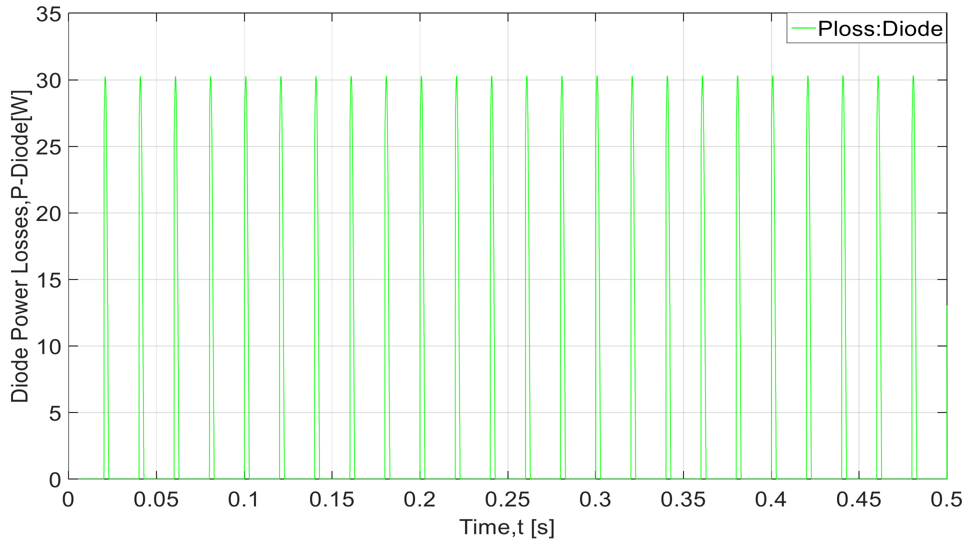


(b)

Figure 5.25 Simulation results of the power losses in (a) IGBT and (b) diode in the electro-thermal model.

5.10.3 Power Loss Verification with the Analytical Method

The loss estimation techniques developed based on the analytical loss model can help to fulfil the purpose to aid the designers with device selection and comparison by performing power losses and temperature calculations. Basic power loss equations are given in Equations (5.14)-(5.17) [196]. In the framework, several user inputs are needed to provide such as the total power flow through the converter, voltage on the DC capacitors, output RMS current, voltage and current at the AC terminals, etc. in order to calculate the average power loss on the device.

$$P_{conduction\ loss-IGBT} = V_{CE} * I_0 * \left(\frac{1}{2\pi} + \frac{m*cos\theta}{8}\right) + r_C * {I_0}^2 * \left(\frac{1}{8} + \frac{m*cos\theta}{3\pi}\right) \quad (5.14)$$

$$P_{conduction\ loss-Diode} = V_D * I_0 * \left(\frac{1}{2\pi} - \frac{m*cos\theta}{8}\right) + r_D * {I_0}^2 * \left(\frac{1}{8} - \frac{m*cos\theta}{3\pi}\right) \quad (5.15)$$

where , m is the modulation index, $cos\theta$ is the power factor, V_{CE} is voltage drop in the device, is the on-state characteristic resistance of IGBT, I_{cav} is the IGBT average current, I_{crms} is the IGBT RMS current, V_D is voltage drop in the diode, r_D is the on-state characteristics of resistance of diode, I_{Dav} is the average diode current, I_{Drms} is the diode

RMS current, I_0 is peak output current of the inverter and a positive sign implies the loss calculation for IGBT and negative sign implies diode.

Average switching loss calculation

$$P_{switching\ losses-IGBT} = f_s * E_{on+off} * \frac{\sqrt{2}}{\pi} * \frac{I_C}{I_{ref}} * (\frac{V_{DC}}{V_{ref}})^{K_V} * (1 + C_T * (T_j - T_{ref})) \ldots. (5.16)$$

$$P_{switching\ losses-Diode} = f_s * E_{rr} * (\frac{\sqrt{2}}{\pi} * \frac{I_C}{I_{ref}})^{K_I} * (\frac{V_{DC}}{V_{ref}})^{K_V} * (1 + C_T * (T_j - T_{ref})) \ldots. (5.17)$$

where I_{ref}, V_{ref} , T_{ref} are the references values that the characteristic curves are based on for loss calculation, I_C is the RMS output current, V_{DC} is the dc-link voltage and K_I , K_V and C_T are constants.

Power losses both for IGBT and diodes are illustrated in Figure 5.26 with the dashed red lines indicating circuit and the green lines indicating analytical. It is seen that the results show the discrepancy in the switching loss estimation of IGBT and diode. The analytical model uses the simplified parameter to calculate the switching losses. However, this analytical loss modelling will cause the difference to the total power loss or the trend of temperature change with operating points. Input parameters for loss estimation by the analytical method are listed in Table 36 and the results obtained using the analytical method are listed. The power losses are given for the individual IGBT and diode losses including conduction and switching losses. The results obtained with the analytical method are compared to the results obtained from PLECS listed in Table 37.

An important feature of the analytical model is its flexibility of fast paced calculation performance. It is very easy to take into account power devices characteristics, modulation scheme and operating conditions etc. Furthermore, with the proposed model it is suitable to change the modulation index from 0 to 1 and the power factor from 0 to 1. In this case the modulation index is considered 0.8 and power factor is considered 0.8. Figure 5.26 shows the power losses obtained for the IGBT and diode respectively inverter operating conditions maintaining constant the RMS value of the output current (25A).

Table 36 Predicted losses of IGBT and diode by analytical method

Input parameters		Estimated Losses	
IGBT: $V_{CE} = 1.6V, m = 0.8$, $p.f = 0.8, r_C = 30m\Omega$, $E_{on} = 8mJ, E_{off} = 5mJ.$ Diode: $V_D = 1.2V, r_D = 17m\Omega$, $E_{rr} = 8.6\mu J$	Switching frequency, $f_{sw}, (kHz)$	IGBT Losses	Diode Losses
	2	95.65W	8.33W
	4	121.65W	10.92W
	6	147.65W	13.5W
	8	173.65W	16.1W
	10	199.65W	18.65W

Table 37 Predicted losses of IGBT and diode by circuit method

Switching frequency, $f_{sw}, (kHz)$	IGBT Losses	Diode Losses
2	90W	13.5W
4	106W	17.6W
6	120W	21.5W
8	135W	26W
10	160W	30W

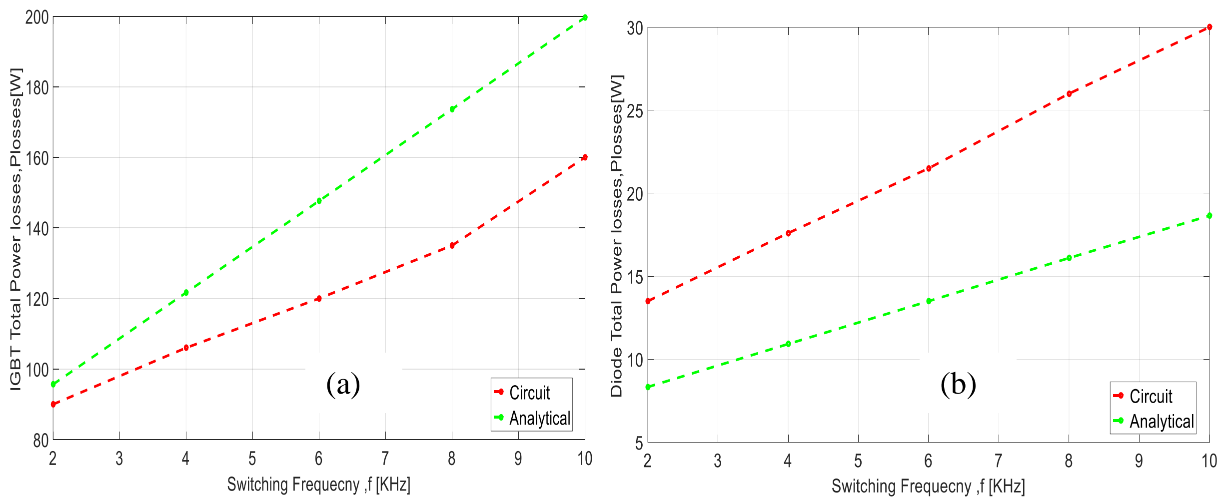


Figure 5.26 Predicted power Losses of (a) IGBT and (b) Diode by Analytical & Circuit Method.

As seen from Figure 5.26, the averaged loss model is compared with an analytical loss model. The analytical loss model is simulated in MATLAB as a simple code including the inverter input information such as power output, dc-bus voltage, RMS ac voltage, current and power factor. The analytical loss model can provide the average losses. The dynamic losses obtained by circuit simulation are averaged for a load cycle to obtain the mean losses. This then can be compared with the results of analytical model at different loading conditions. As seen in Figure 5.26, five sets of results differ. The discrepancy gets generated since the analytical model assumes the steady-state simplified electrical parameters. Also, the switching process does not consider the accurate switching voltage, accurate switching current and the reverse recovery process of freewheeling diode. The turn-on and turn-off losses due to increased switching frequency may contribute to the variation of losses. Since PLECS estimates the average power losses based on the utilisation of the predicted device current and voltage waveforms and switching details, it is more accurate compared to analytical model. This indicates that PLECS predicted loss can be applied in thermal network to estimate temperatures.

5.11 Integration of Electro-thermal Model

The thermal network for the converter electro-thermal interaction analysis has been established according to the derived RC parameters from FEA analysis. The model considers the interaction between IGBT and diode in a switch of a half-bridge module contained by the inverter.

Since the thermal model based on a datasheet-derived RC lumped parameter cannot predict the temperature at the critical material interface layer in IGBT modules, it is important to include the interface material layer in the thermal model to identify hotspot accurately and improve the design. Combining datasheet derived RC thermal parameter with the parameters for thermal interface and heatsink materials in the thermal model results in an inaccurate estimation of temperature profiles. Although the model can be solved in many cases by applying the fixed case temperature boundary, it is important to consider the heat flow from the chip to ambient to analyse long load mission profiles accurately.

To represent the self-heating Foster RC cells are derived for each heat conduction path from one layer to another layer. Here, the thermal losses via radiation are neglected. Losses in IGBT and diode can be coupled to the thermal network. It is observed that heat transmission is gradual and it can take time to reach steady state. Owing to the chain type connection of

the Foster RC cell is faster as because heat will directly flow to the heatsink. Although Cauer network transformation could give more accurate temperature prediction, still the Foster network can be used in the prediction of temperature profiles because it corresponds to the physical node in the real structure.

To analyse the coupling effect, three separate models have been built. First, two model considers the self-heating and cross-heating. The difference is that the first one uses the parameters using the temperature dependent thermal model while the second one uses temperature independent model parameters. The last one only considers the self-heating.

Self-heating is modelled considering the self-power dissipation and thermal network of itself. Figure 5.27 and Figure 5.28 presents the non-coupled thermal model network of IGBT and diode respectively. The model describes the heat conduction from junction to case and the heat convection from baseplate to heatsink. The convection process is also included into the model considering the baseplate to heatsink thermal network. Heat conduction from junction to baseplate is modelled with the help of thermal network consisting of junction to solder, solder to baseplate solder and baseplate solder to baseplate.

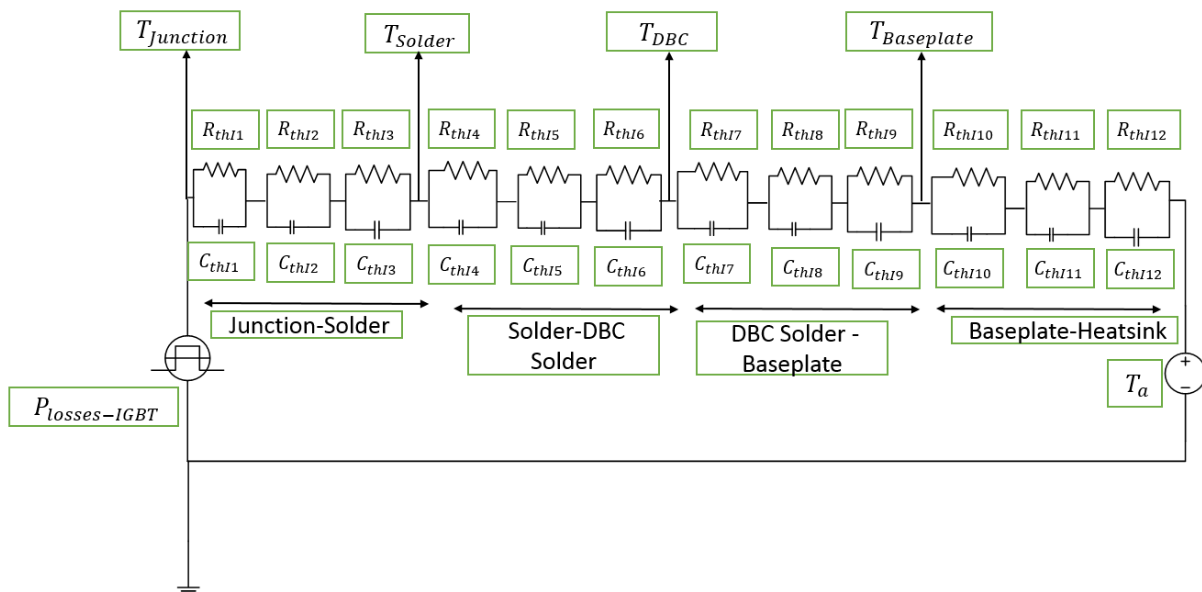


Figure 5.27 Thermal network for IGBT –self heating

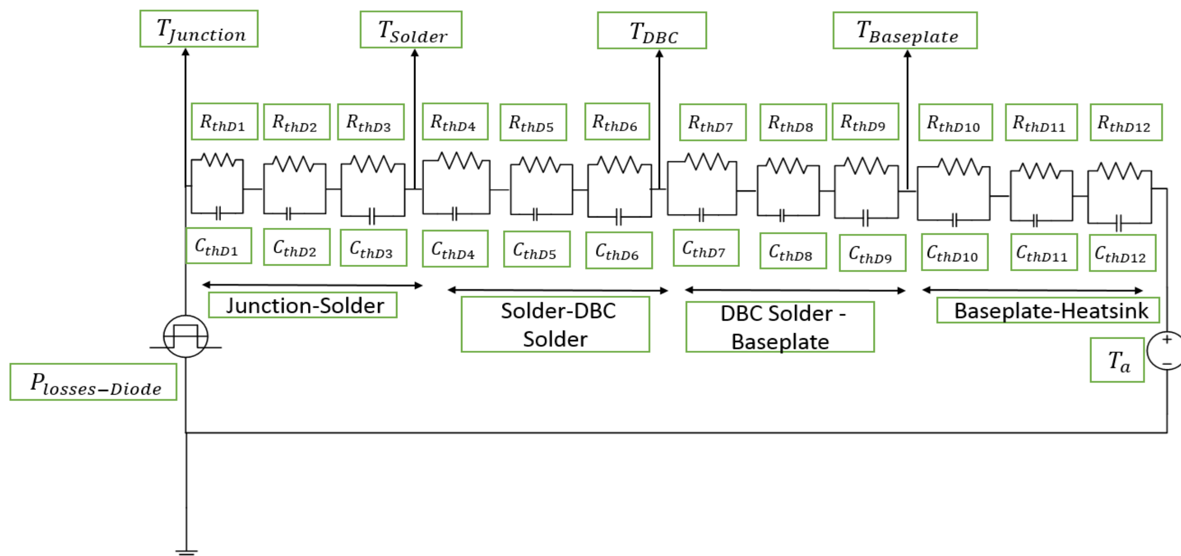


Figure 5.28 Thermal network for Diode –self heating.

To take into account the thermal coupling effect, a thermal model of cross-heating contribution is added considering the adjacent components model. Figure 5.29 and Figure 5.30 presents the coupled thermal model network of IGBT and diode respectively. The adjacent model is built with power dissipation is connected as a heat source to the thermal network that includes junction to heatsink thermal network. The ambient temperature is set as reference temperature.

To perform the integrated electro-thermal analysis, the electrical model of the inverter in PLECS is coupled with RC thermal network model. The coupled simulation can estimate temperature profile at locations like junction, solder, baseplate solder and baseplate etc. of the multichip power module at steady state level.

IGBT self-heating thermal network provides the temperature at the nodes such as junction, solder, baseplate solder and baseplate without considering the coupling effect. When diode-cross heating is connected in the thermal model then temperature obtained at the nodes such as junction, solder, baseplate solder and baseplate takes thermal coupling effect. It is worth to point that the IGBT self-heating model describes the heat transfer from the device to heatsink and does not consider lateral thermal spreading from layer to layer which is responsible for generating the wrong estimation of temperature. The contribution of diode-cross heating network with the self-heated IGBT thermal network causes the prediction of temperatures

different than that by IGBT self-heated thermal network. The superposition principle is maintained by the self-heating and cross-heating thermal network.

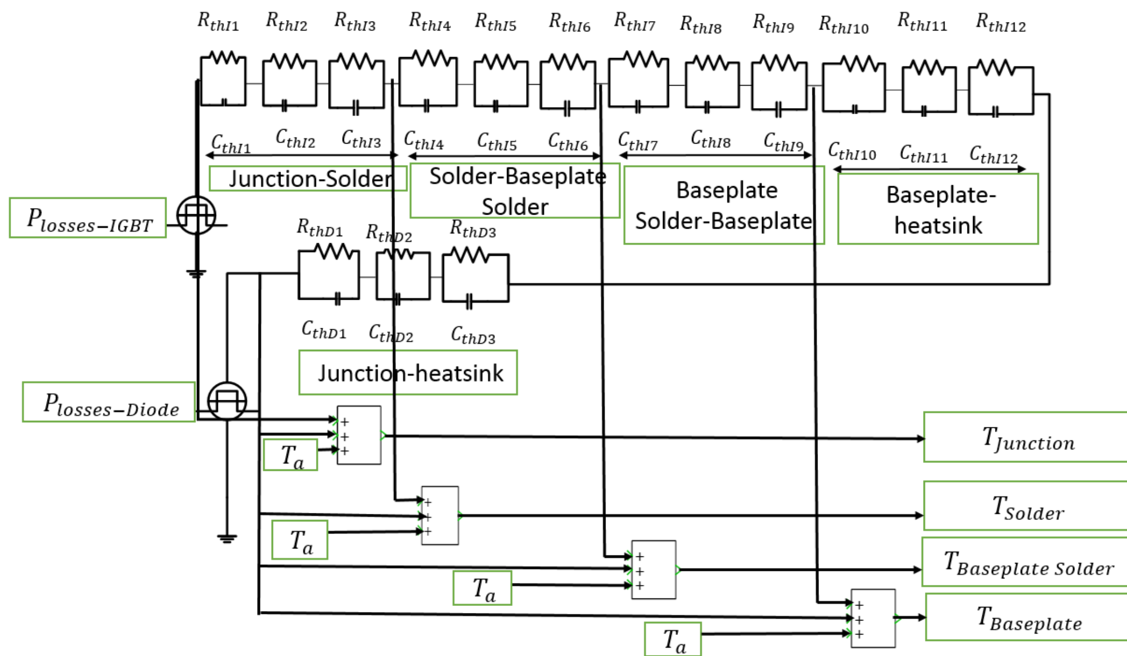


Figure 5.29 Thermal network for IGBT –self heating and Diode-cross heating

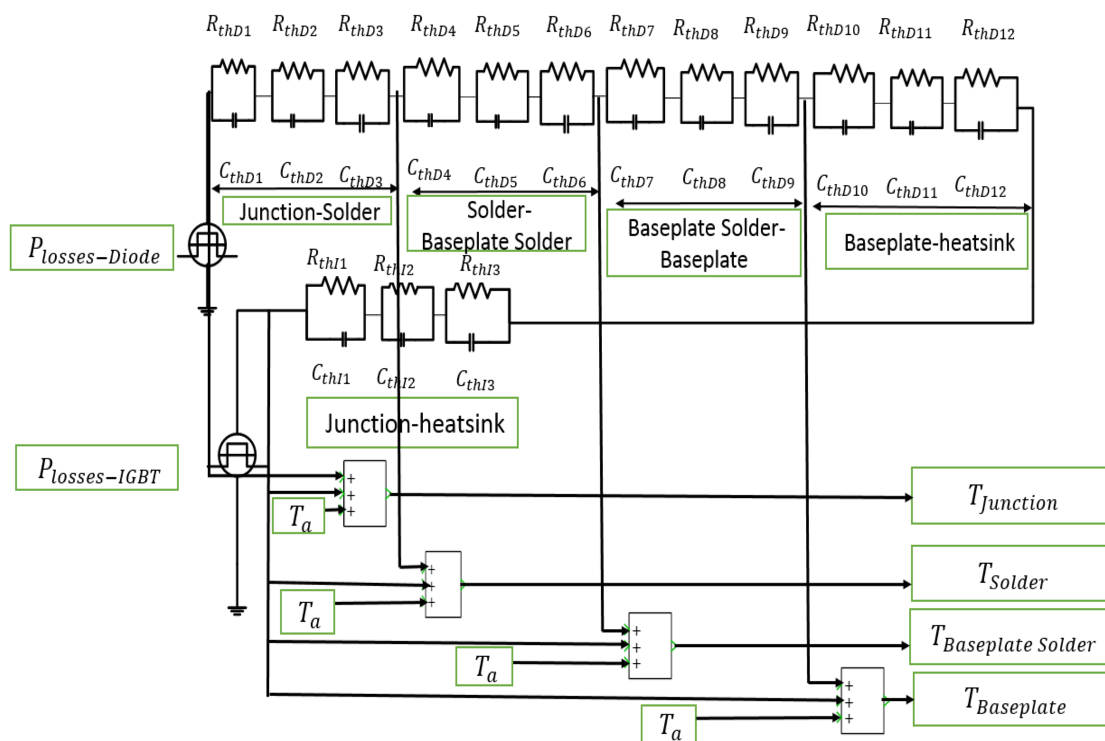


Figure 5.30 Thermal network for Diode –self heating and IGBT-cross heating.

5.12 Analysis of Coupling Effect under Different Power Losses and Varying Chip Distance

Since the thermal interaction is influenced by the power losses and the distance between two chips, it is interesting to discuss in how much degree the power losses and distance will influence the junction temperature prediction and the coupling factor.

For the inverter component IGBT (S1) and diode (D1) studied in this thesis, the power losses variation is maintained in the range of 20-120W and the distance between chips is varied in the range of 1-6mm. The power losses are assumed to investigate the thermal influence on each other. For six different power losses, simulations are performed six times. The reference temperature is set at 32.85°C. The simulations are performed the six times by varying distance between chips. The junction temperature is recorded for the IGBT, the diode and the coupling resistance is calculated by using the equation 4.57.

For each distance change and each power loss variation, the simulations are performed, and results are listed in Table 38-Table 43. Figure 5.31 shows the curve fitted expression of coupling resistance factor with respect to power loss variation when chip to chip distance is kept at 1mm.

Table 38 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 1mm

Power Level, (W)	$T_{j-IGBT}, (°C)$	$T_{j-Diode}, (°C)$	$R_{th-coupling}(°C/W)$
20	38.533	33.6	0.0375
40	44.233	34.349	0.037475
60	49.95	35.098	0.037467
80	55.683	35.845	0.037438
100	61.432	36.592	0.03742
120	67.197	37.338	0.0374

Table 39 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 2mm

Power Level, (W)	$T_{j-IGBT}, (°C)$	$T_{j-Diode}, (°C)$	$R_{th-coupling} (°C/W)$
20	38.541	33.322	0.0236
40	44.249	33.794	0.0236
60	49.974	34.266	0.0236
80	55.716	34.736	0.023575
100	61.473	35.207	0.02357
120	67.245	35.677	0.023558

Table 40 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 3mm

Power Level, (W)	$T_{j-IGBT}, (°C)$	$T_{j-Diode}, (°C)$	$R_{th-coupling} (°C/W)$
20	38.544	33.151	0.01505
40	44.255	33.451	0.015025
60	49.983	33.751	0.015016667
80	55.728	34.051	0.0150125
100	61.488	34.351	0.01501
120	67.263	34.65	0.015

Table 41 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 4mm

Power Level, (W)	$T_{j-IGBT}, (°C)$	$T_{j-Diode}, (°C)$	$R_{th-coupling} (°C/W)$
20	38.545	33.043	0.00965
40	44.258	33.236	0.00965
60	49.987	33.429	0.00965
80	55.733	33.622	0.00965
100	61.494	33.815	0.00965
120	67.27	34.007	0.009642

Table 42 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 5mm

Power Level, (W)	T_{j-IGBT}, $(°C)$	$T_{j-Diode}$, $(°C)$	$R_{th-coupling}(°C/W)$
20	38.545	32.975	0.00625
40	44.258	33.1	0.00625
60	49.988	33.226	0.006267
80	55.734	33.351	0.006262
100	61.496	33.475	0.00625
120	67.273	33.6	0.00625

Table 43 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 6mm

Power Level, (W)	T_{j-IGBT}, $(°C)$	$T_{j-Diode}$, $(°C)$	$R_{th-coupling}(°C/W)$
20	38.546	32.932	0.0041
40	44.259	33.014	0.0041
60	49.989	33.095	0.004083
80	55.735	33.177	0.004087
100	61.497	33.259	0.00409
120	67.274	33.34	0.004083

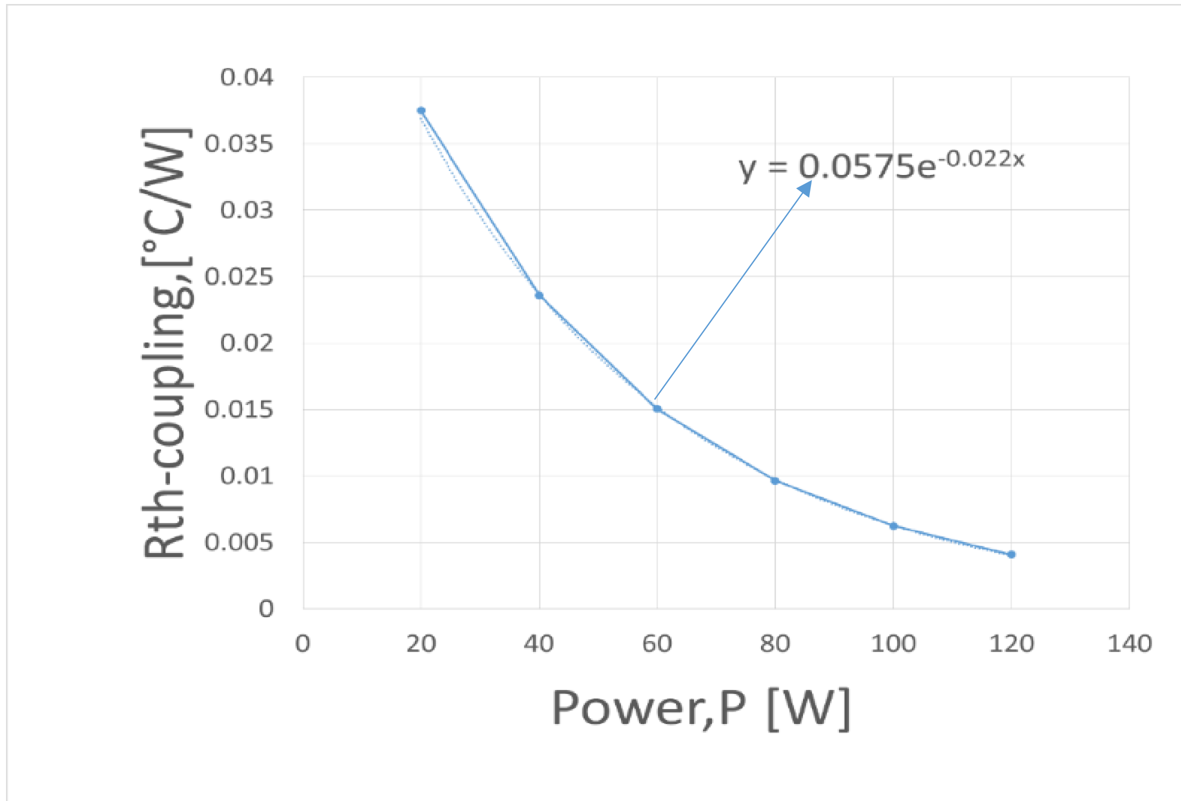


Figure 5.31 Curve fitted expression of coupling resistance factor with respect to power loss variation when chip distance is kept 1mm.

From the Figure 5.31 above it is clear that the mutual coupling resistance factor decreases with the increase of power dissipation. The simulation has been performed varying power dissipation from 20W to 120W in IGBT chip, S1. Most of the heat dissipates in self-heating of the component, S1 and thereby increase temperature rise in S1. The temperature gets increased at the adjacent component, D1 increases slightly with the increased power dissipation. It can be pointed out that although the temperature rise is high, but the coupling resistance factor gets decreased due to the temperature difference divided by the increased power dissipation.

Another simulation is performed to investigate the coupling effect of diode1 (D1) on IGBT1 (S1), diode2 (D2) and IGBT2 (S2). To perform this, power is varied from 10W to 60W at the D1 chip and the distance between the chips is kept at 6mm. The recorded junction temperature at each device is listed, mutual coupling resistances are calculated, and results are listed in Table 44. Figure 5.32 shows the coupling resistance factor between Diode1-IGBT1, and Diode1-Diode2 respectively with respect to power loss variation.

Table 44 Predicted temperature and mutual coupling resistance when the distance between IGBT chip and diode chip is 6mm

Power Level, (W)	$T_{j-IGBT1}$, $(°C)$	$T_{j-Diode1}$ $(°C)$	$T_{j-Diode2}$, $(°C)$	$R_{th-coupling}(°C/W)$: $Diode1 - IGBT1$	$R_{th-coupling}(°C/W)$: $Diode1 - Diode2$
10	32.878	39.208	32.853	0.0028	0.0003
20	32.906	45.611	32.855	0.0028	0.00025
30	32.934	52.058	32.858	0.0028	0.00026
40	32.962	58.547	32.86	0.0028	0.00025
50	32.991	65.077	32.863	0.00282	0.00026
60	33.019	71.646	32.865	0.00281	0.00025

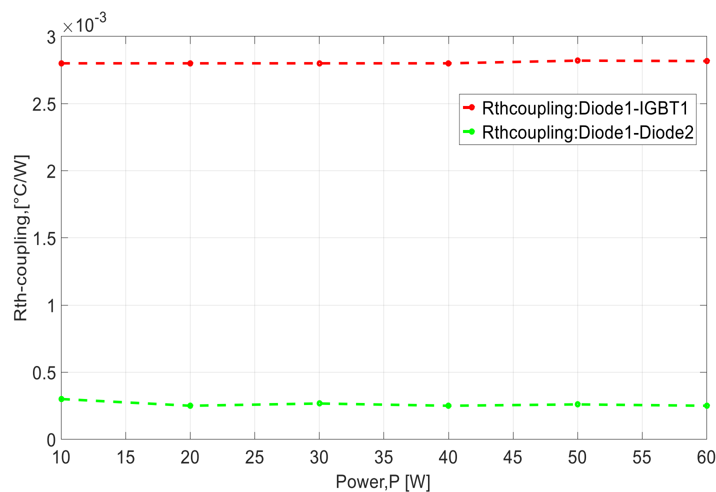


Figure 5.32 Coupling resistance factor between Diode1-IGBT1, and Diode1-Diode2 respectively with respect to power loss variation

From the Figure 5.32 above it is clear that the mutual coupling resistance factor decreases with the increase of power dissipation. The simulation has been performed on varying power dissipation from 20W to 60W. It is seen from Figure 5.32 that D1 affects the S1 as it is close compared to D2 and S2. Consequently, the mutual resistance between D1 and S1 becomes slightly lower than that of D1 and D2 and D1 and S2 respectively.

IGBT-IGBT interaction:

Simulations are performed to investigate the effect of IGBT1 (S1) on IGBT2 (S2) due to thermal interactions. To perform this power is varied from 20W to 120W at IGBT1 and the chip distance is varied from 1 to 6mm. Results of the temperature difference between IGBT1 and IGBT2 are listed in Table 45 and Table 46 respectively. Thermal influence of IGBT1 on IGBT2 is shown in Figure 5.33.

Table 45 Predicted temperatures of IGBT1 and IGBT2 when the distance at varying distance

Power, (W)	$T_{j-IGBT1}$, (°$\boldsymbol{C}$)						$T_{j-IGBT2}$, (°$\boldsymbol{C}$)
	Distance (mm)						
	1	2	3	4	5	6	
20	38.533	38.541	38.544	38.545	38.545	38.546	32.85
40	44.233	44.249	44.255	44.258	44.258	44.259	32.85
60	49.95	49.974	49.983	49.987	49.988	49.989	32.85
80	55.683	55.716	55.728	55.733	55.734	55.735	32.85
100	61.432	61.473	61.488	61.494	61.496	61.497	32.85
120	67.197	67.245	67.263	67.27	67.273	67.274	32.85

Table 46 Predicted temperature difference between of IGBT1 and IGBT2 at varying distance

Power, (W)	Distance (mm)					
	1	2	3	4	5	6
	$\Delta T1$, (°C)	$\Delta T2$ (°C)	$\Delta T3$ (°C)	$\Delta T4$ (°C)	$\Delta T5$ (°C)	$\Delta T6$ (°C)
20	5.683	5.691	5.694	5.695	5.695	5.696
40	11.383	11.399	11.405	11.408	11.408	11.409
60	17.1	17.124	17.133	17.137	17.138	17.139
80	22.833	22.866	22.878	22.883	22.884	22.885
100	28.582	28.623	28.638	28.644	28.646	28.647
120	34.347	34.395	34.413	34.42	34.423	34.424

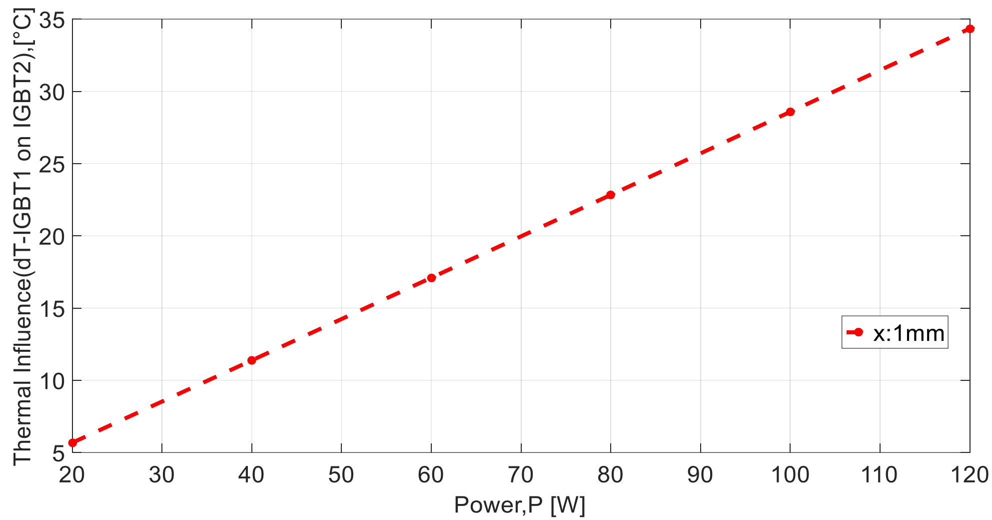


Figure 5.33 Thermal Influence of IGBT1 on IGBT2.

From the Figure 5.33 above it is clear that the thermal influence causes to temperature rise with the increase of power dissipation. The simulation has been performed varying power dissipation from 20W to 120W. The increased power dissipation increases the junction temperature, so the temperature difference between two components become high and by this, mutual thermal influence becomes higher. It is seen from the Table 46 that with the increase of distance at fixed power results in slight variation of thermal influence as the junction temperature increases slightly S1 compared to S2 while with the increased power at fixed distance results in higher thermal influence as the junction temperature increases at S1 compared to S2.

5.13 Performance Analysis of the Coupling Factor

The coupled electro-thermal developed in this thesis has taken into account both the issues like the temperature dependence of the power loss model and the thermal interactions in the thermal model. Since the thermal model is simplified usually assuming the effect of these factors negligible, a study subjected to evaluation of the errors generated by these simplifications will be of importance to the power electronics system designers.

To investigate the effect of avoiding temperature dependency and the thermal interaction, simulations are conducted for three cases. Case 1 considers the RC thermal network parameters that have been derived from FEA simulation using the temperature-dependent material properties. Case 2 considers the RC parameters that are derived from FEA

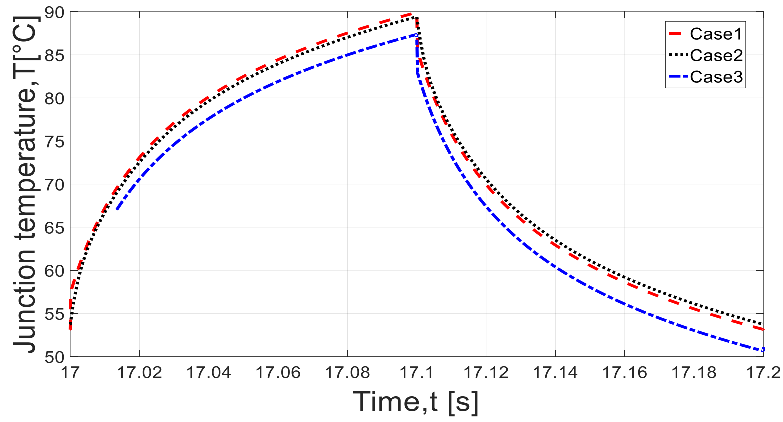
simulation using temperature-dependent material properties. In both cases, the cross-heating impedance terms are included in the IGBT thermal network model. In the third case, the RC parameters do not include cross-heating thermal impedance terms. To evaluate the performance of the temperature dependent electro-thermal coupled method, a comparison is made with the temperature independent model and the non-coupled model.

The obtained simulation results are plotted together as shown in Figure 5.34 to make fair comparisons. It can be observed that the impact of the temperature dependence of the power loss to the junction temperature is not significant and comparing to the temperature dependent model the temperature at locations such as at the junction, at the solder, at the baseplate solder and at the baseplate is in the range of 0.2°-0.8°C. This result is reasonable because the effect of temperature on the power losses in an IGBT is relatively small.

Figure 5.34 shows the IGBT and diode temperatures at critical locations for the three cases for the time duration between 17 and 17.2 s simulation time when steady state has been reached. It can be seen in Figure 5.34(a), the IGBT junction temperatures for case 1 and 2 differ by about 1.3 °C and for case 1 and 3 differ by about 2.42°C. This shows that both thermal coupling and nonlinearity of material properties affect the temperature predictions but thermal coupling has a much greater effect. The discrepancy is also observed at the solder, at the baseplate solder, and at the baseplate. The difference is about 2.59°C, 2.56°C and 2.63°C respectively at the chip solder, at the baseplate solder and at the baseplate respectively (see Figure 5.34 (b-d)). Figure 5.34 (e) shows the junction temperature of the diode. Once again, the effects of material property and thermal coupling are significant. However, the temperature difference between case 1 and 3 is about 13.2°C which is much greater than for the IGBT. The difference is about 13.4°C, 13.3°C and 13.6°C respectively at the chip solder, at the baseplate solder and at the baseplate respectively (see Figure 5.34 (f-h)).

The difference is higher in chip solder to baseplate solder area and the main reason is that the thermal spreading is higher and interaction of the cross-thermal spreading is dominant. But the heat blocking also occur in the baseplate solder since the heat capacity dominates and the baseplate temperature variation is observed since the thermal grease is simplified in the model. The comparisons indicate the proposed thermal model predicts the temperature profile accurately because the inclusion of coupling effect in the model permits to more accurately predict the losses of the adjacent component and the cross-heating effect. This clearly

demonstrates that the temperature analysis by considering the thermal coupling factor would give us an accurate estimation not only in junction node but also in other locations of the component.



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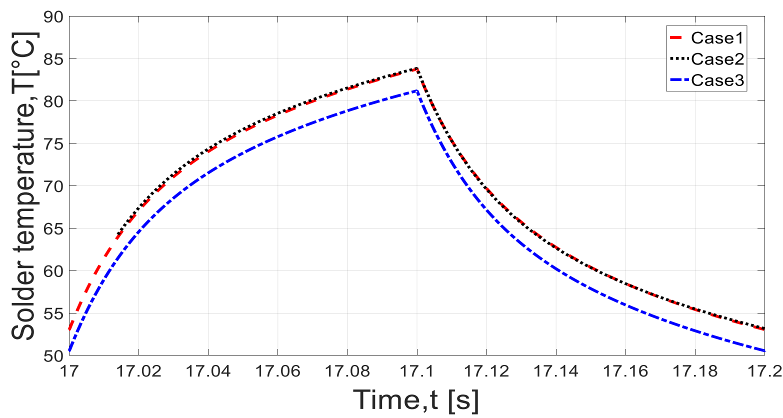

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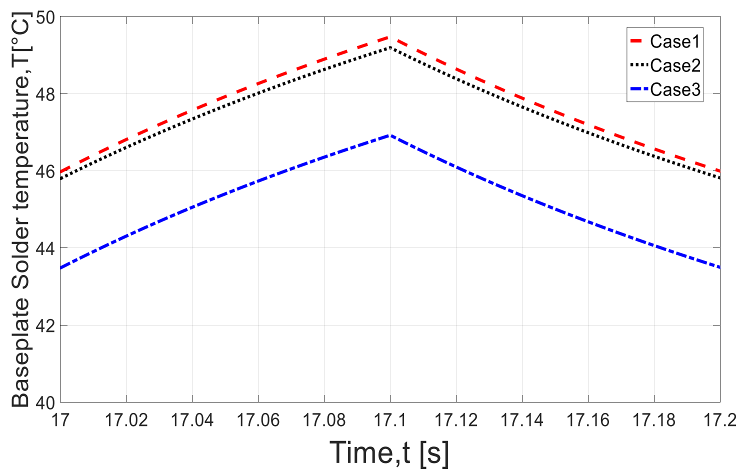

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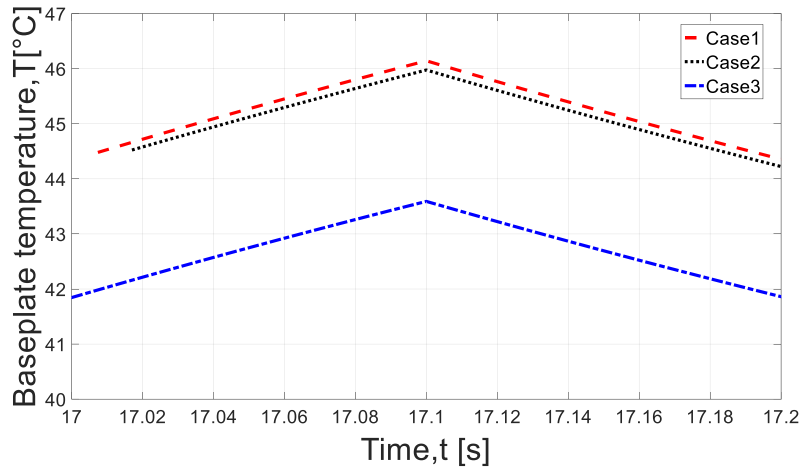

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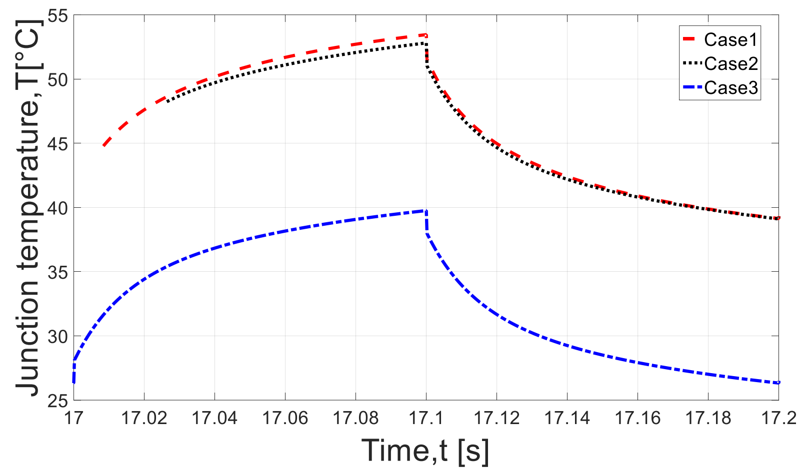

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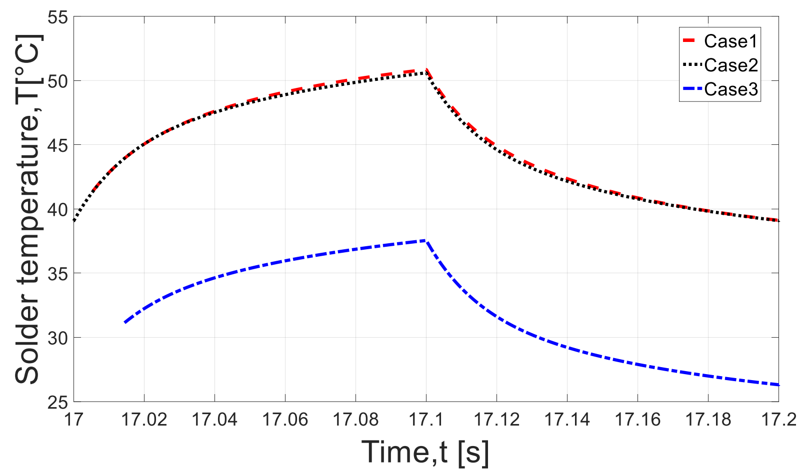
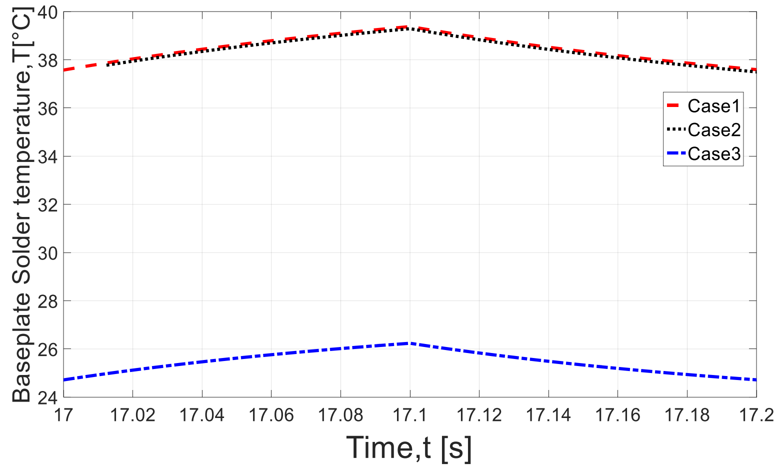
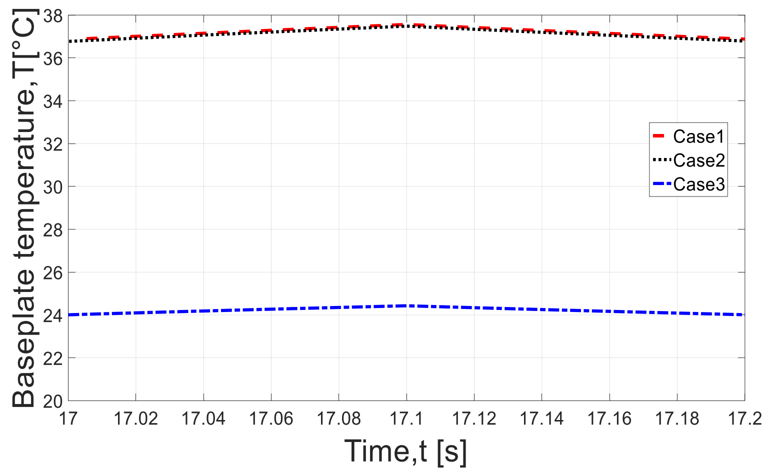


(f)



(g)



(h)

Figure 5.34 Dynamic Temperature Profile (a) Junction temperature-IGBT (b) solder temperature-IGBT(c) baseplate solder temperature-IGBT (d) baseplate temperature-IGBT (e) Junction temperature-diode (f) solder temperature-diode (g) baseplate solder temperature-diode (h) baseplate temperature-diode.

5.14 Effect of load frequency variation on the prediction of junction temperature

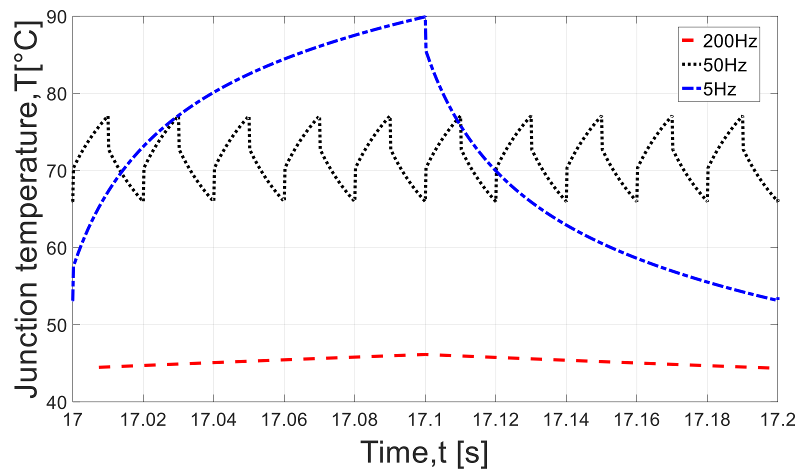
Since the fluctuation of power losses at the fundamental frequency causes the temperature fluctuation, it is important to investigate the influence of variation of load frequency on temperature estimation particularly the junction temperature estimation.

The coupled electro-thermal developed in this thesis has taken into account the issues of load frequency variation. The load frequency variation is assumed running a motor load by the power inverter and usually, this varies in the range of 0-200Hz and therefore, three values 200Hz, 50Hz and 5Hz have been selected. To keep the same power losses, load current is maintained the same in all the cases. To investigate the load frequency variation the simulations are tested by feeding the power losses at 200Hz, 50Hz and 5Hz respectively into the thermal network. Figure 5.35 shows the impact of load frequency variation on temperature estimation.

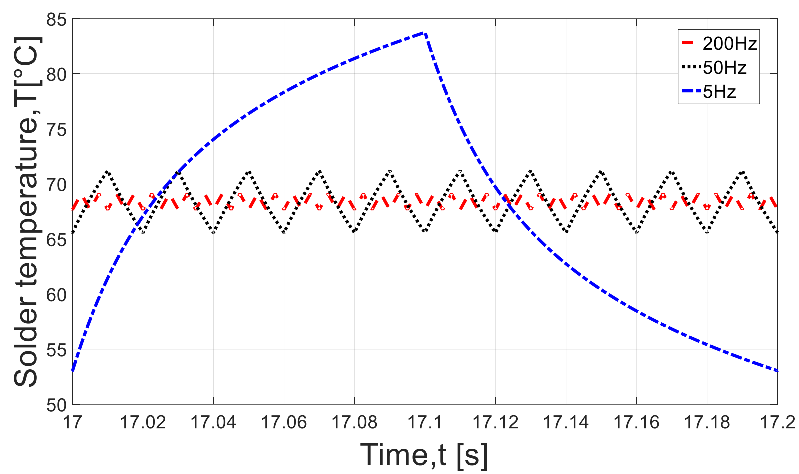
The obtained simulation results are plotted together as shown in Figure 5.35 in order to make fair comparisons. It can be seen that the effect of load frequency variation on temperature estimation is pretty significant and comparing to each other the temperature fluctuations are higher at the low frequency of 5 Hz than that by 200Hz and 50Hz respectively. The main reason is thought to be that the injected power losses at low frequency results in increased heating on time and off time. The increased heating on time results in increased temperature rise and the temperature fluctuations shows high gradients during cooling time.

The amplitude of peak junction temperature ripples at 5Hz varies by 45°C and 29°C compared to than that of 200Hz and 50Hz respectively. The amplitude of peak temperature ripples of solder at 5Hz vary by 15°C and 12.6°C respectively compared to than that of 200Hz and 50Hz respectively. The amplitude of peak temperature ripples of baseplate solder at 5Hz vary by 1.8°C and 0.35°C respectively compared to than that of 200Hz and 50Hz respectively. The amplitude of peak temperature ripples of baseplate at 5Hz vary by 1°C and 0.8°C respectively compared to than that of 200Hz and 50Hz respectively. The variation at the junction and the chip solder is prominent compared to than that of baseplate solder and baseplate. This happens due to thick layered structure of baseplate solder and baseplate contributing to higher thermal mass and thereby, causes slow variation in the temperature ripple. These results demonstrate the importance of load frequency variation on the performance of transient electro-thermal analysis during the design stage of the inverter. The peak junction temperature could be much higher in low frequency loading. The temperature fluctuations are pretty obvious and could be significant in reliability estimation since the power semiconductor device operating lifetime is influenced directly by the maximum junction temperature and the temperature fluctuations due to loading. Exceeding the safe operating thermal limit will cause the component to fail permanently and the temperature cycling will result in repetitive continuous thermal stresses and fatigue of the components.

The situation may be even worse by increasing this temperature fluctuation higher when the load frequency goes down below this fundamental frequency.



(a)



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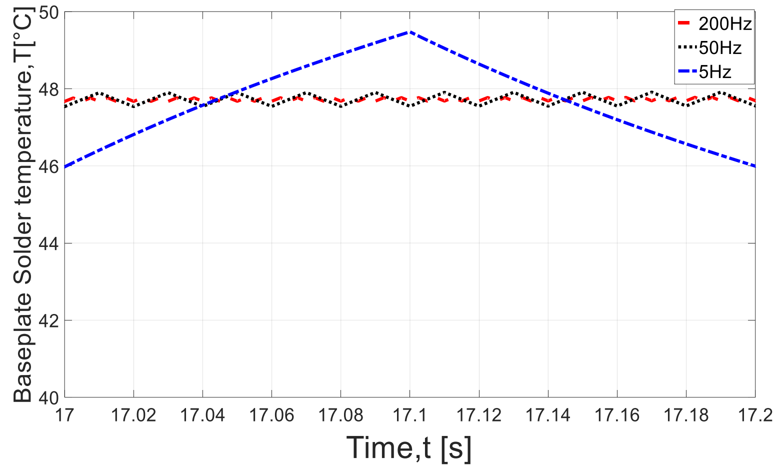

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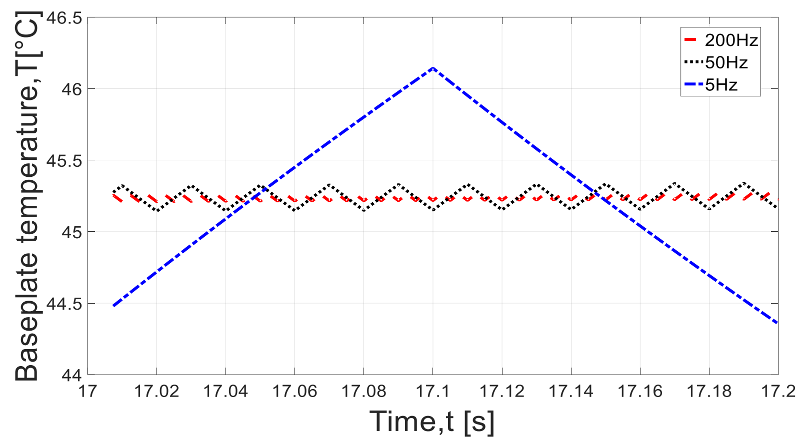


(d)

Figure 5.35 Dynamic Temperature Profile of IGBT (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature.

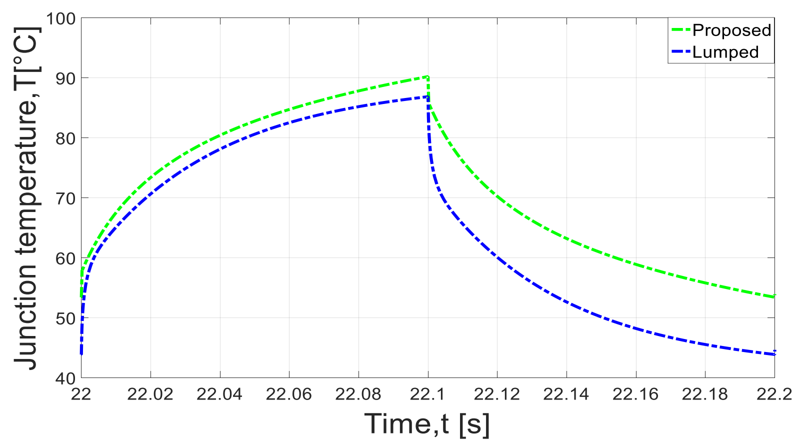
5.15 Evaluation of error analysis of the proposed model comparing to the analytical lumped model

The proposed electro-thermal model in this thesis has included both the temperature dependency and the component interaction in the thermal model. Since the analytical lumped model parameters do not take into account the thermal spreading and the coupling factors, it will be worth to determine the errors caused by this simplified lumped model parameters.

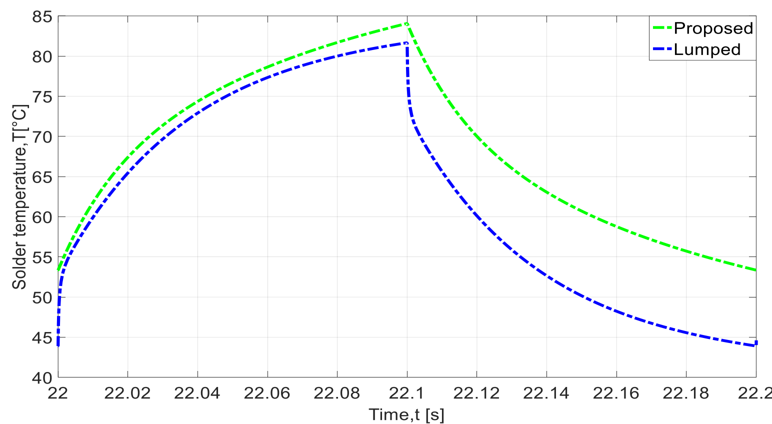
A comparison of these simulation results for junction and solder layers are plotted in Figure 5.36. It can be observed that the IGBT temperature is underestimated by the analytical

lumped model at the junction and the chip solder by 3.34°C and 2.35°C respectively. The temperature difference in IGBT is noticed at the baseplate solder and the baseplate by 2.69°C and 2.60°C respectively. Similarly, the diode temperatures at the junction and the chip solder differ by 13.06°C and 12.72°C respectively in comparison to the proposed model. The temperature difference in the diode is found at the baseplate solder and the baseplate by 14.01°C and 13.29°C respectively. It can be seen that the impact of non-linearity and coupling effect is significant. The discrepancy in temperature prediction by lumped model comparing to the proposed model can be described by the fact that the non-linearity and coupling effect affects significantly.

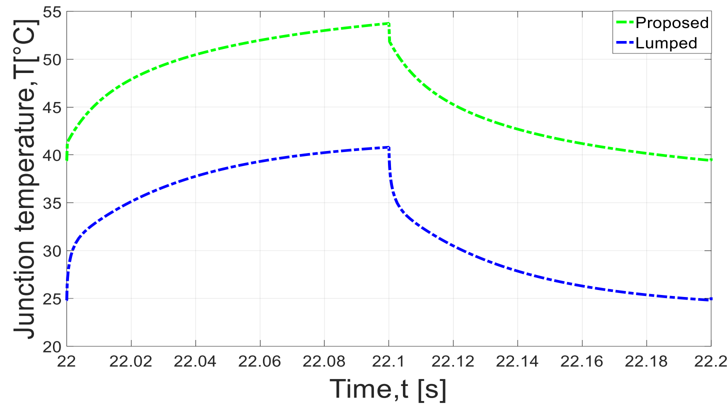
So, it can be concluded that it is highly important to take into account the effect of non-linearity and coupling effects when constructing the thermal model at the early design stage of the inverter to help maintain the accuracy in temperature prediction.



(a)



(b)



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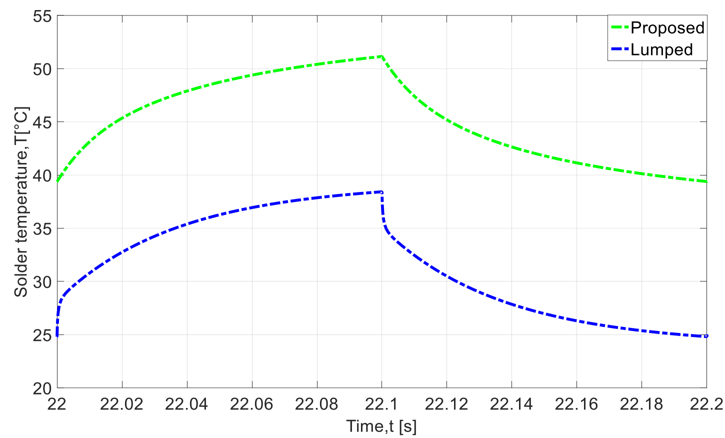


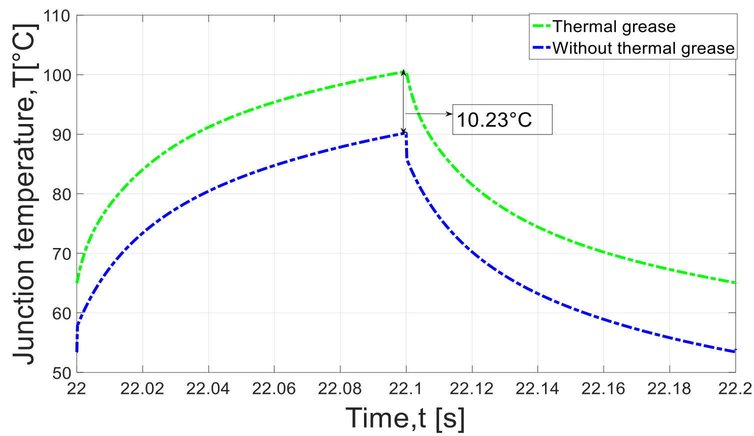
(d)

Figure 5.36 Dynamic temperature profile (a) IGBT Junction temperature (b) IGBT solder temperature (c) diode Junction temperature (d) diode solder temperature

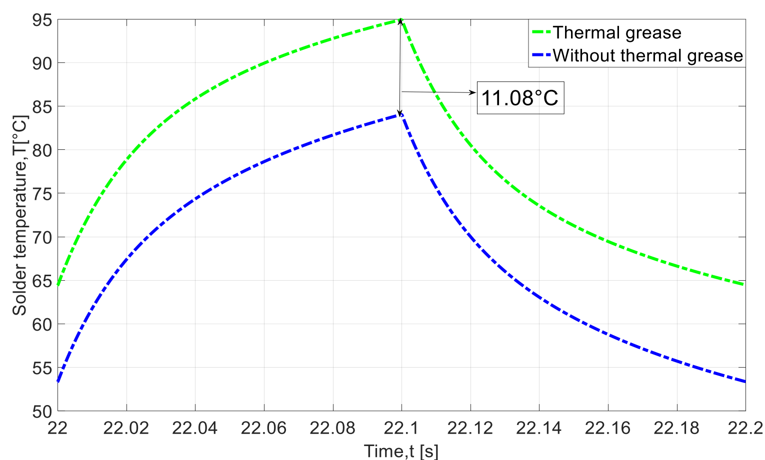
5.16 Analysis of the impact of thermal grease layer on the thermal model

To evaluate the impact of thermal interface material layer on the thermal model, a case study is setup including the thermal grease layer in the model. The thermal network model is built then using the extracted parameters for this case. A comparison is made with the model that does not include the thermal grease layer. The results of temperature prediction of IGBT and diode are plotted in Figure 5.37 & 5.38 respectively. Comparing to the results of the thermal model, the discrepancy of temperature in IGBT at the junction, at the chip solder, the at baseplate solder and at the baseplate is seen by 10.23°C, 11.08°C, 13.64°C and 11.14°C respectively (see Figure 5.37). In diode, temperature differs at the junction, at the solder, at the baseplate solder and at the baseplate by 10.97°C, 11.38°C, 12.05°C and 11.92°C

respectively (see Figure 5.38). It can be seen that the impact of thermal grease layer and material non-linearity is significant. This result is reasonable that the insertion of thermal grease layer contributes to the thermal resistance and thermal capacitance in the thermal branch baseplate to ambient layer. The discrepancy is thought to be caused by the heat transfer blocking behavior in the baseplate. Heat in upper layers remains and changes slowly in the bottom layer due to the contribution of higher thermal capacitance in the bottom layers such as at the baseplate and at the thermal grease layer. It can be concluded that by taking into account the thermal grease layer, non-linearity, thermal coupling and by extracting RC parameters from FEA thermal analysis results junction temperatures can be predicted more accurately than using lumped parameter thermal network model alone.



(a)



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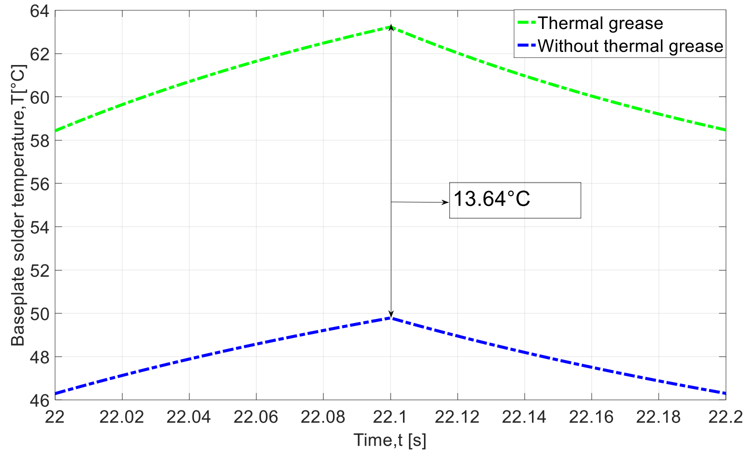
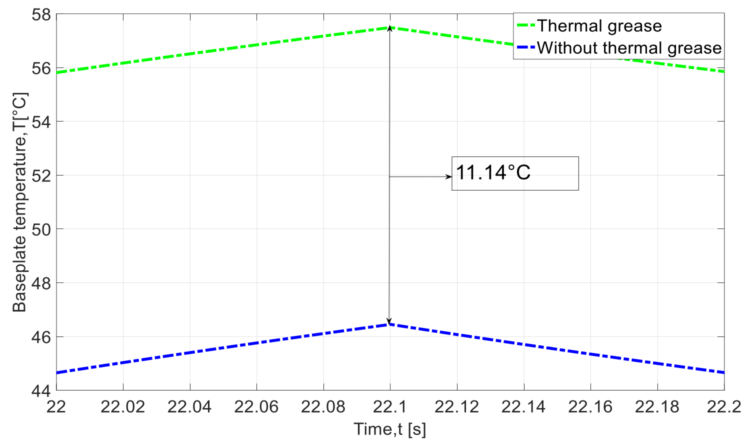
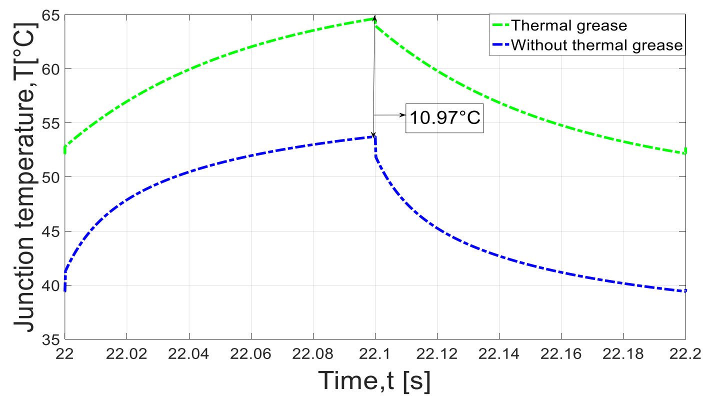


(c)

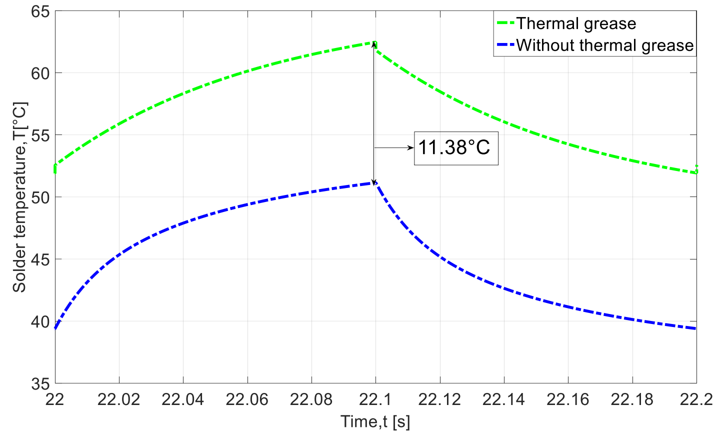


(d)

Figure 5.37 Dynamic temperature profile of IGBT (a) junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature



(a)



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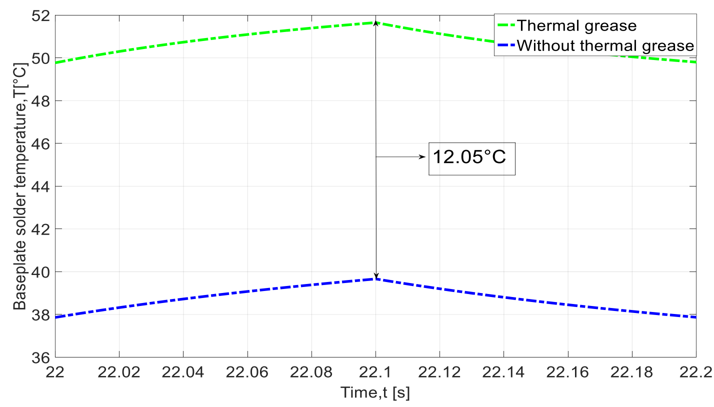

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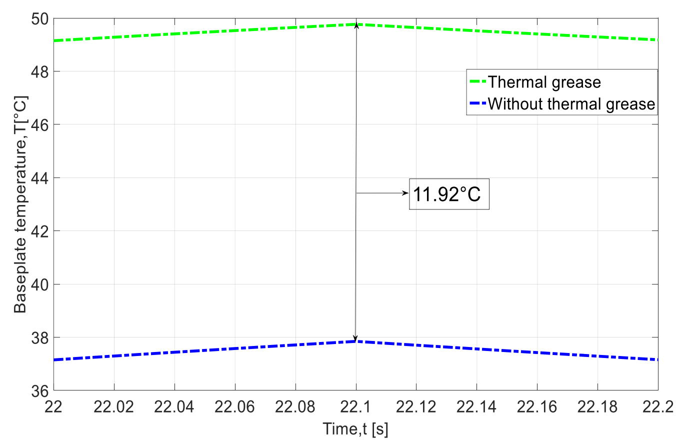


(d)

Figure 5.38 Dynamic temperature profile of Diode (a) junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature

5.17 Robustness of the Modelling

To gain confidence in the RC parameterised model, the simulation has been performed under varying loss profile and then compared to FEA simulations. The average loss profiles of 158W and 30W respectively are assumed both at the IGBT and the diode. The same loss profiles are applied both the circuit model and FEA model under varying duty ratio. The on-time duration for the applied power losses is chosen to be as 1s, 5s, 8s, 10s and 12s respectively. The dynamic temperature profile of IGBT estimated by both the circuit model and FEA model including junction temperature, solder temperature, baseplate solder temperature and baseplate temperature are shown in Figure 5.39, Figure 5.40, Figure 5.41, Figure 5.42 and Figure 5.43 respectively. It is clear from the all figures that the circuit model results are consistent with the FEA model results in all cases and the highest variation is in the range of 2-3°C. Therefore, it can be concluded that the circuit model is robust and can be used in any loading profile as it maintains the modelling accuracy 95%.

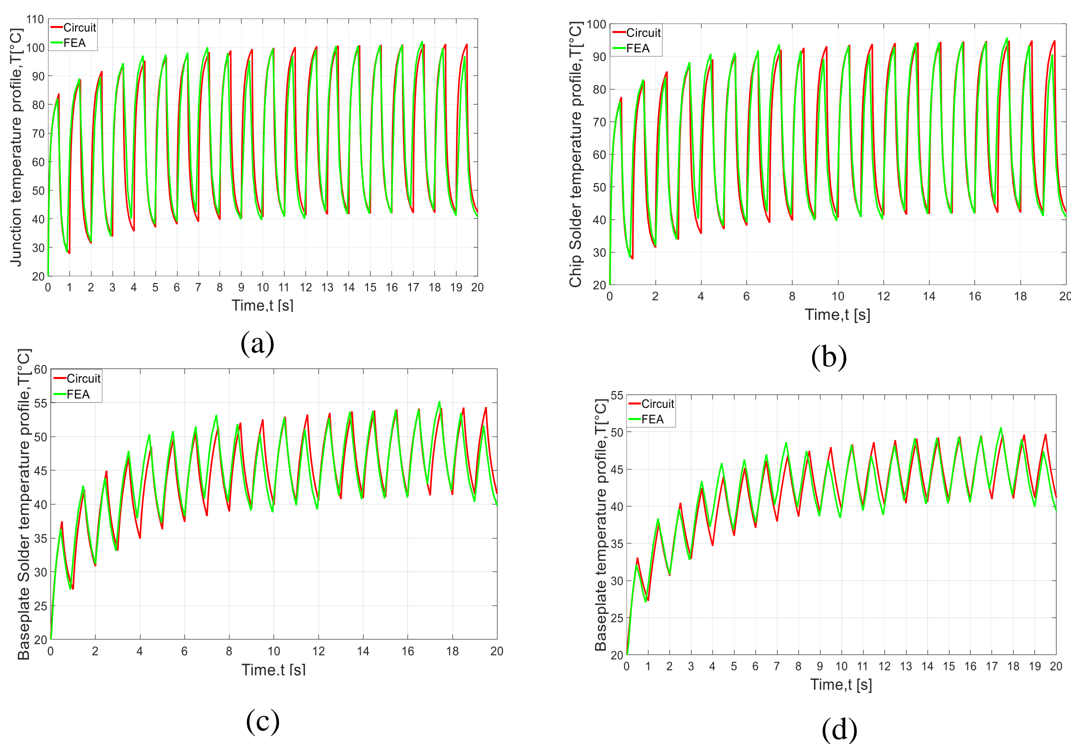


Figure 5.39 Dynamic temperature profile of IGBT at 1Hz pulsed power profile, Duty ratio-0.5 (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature.

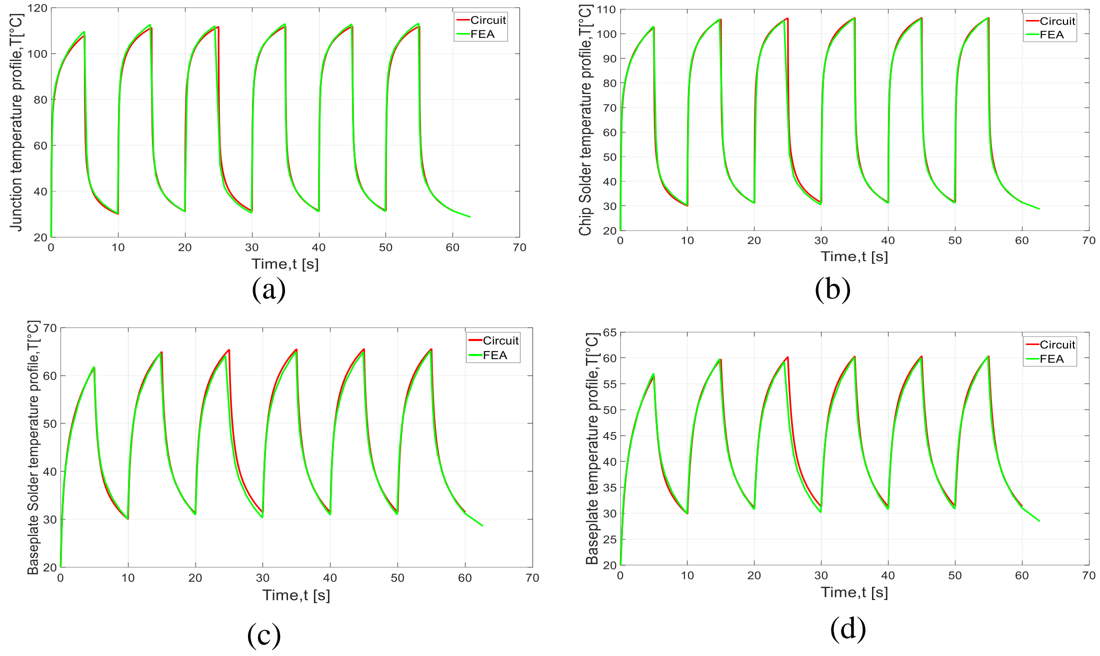


Figure 5.40 Dynamic temperature profile of IGBT at 0.1Hz pulsed power profile, Duty ratio-0.5 (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature.

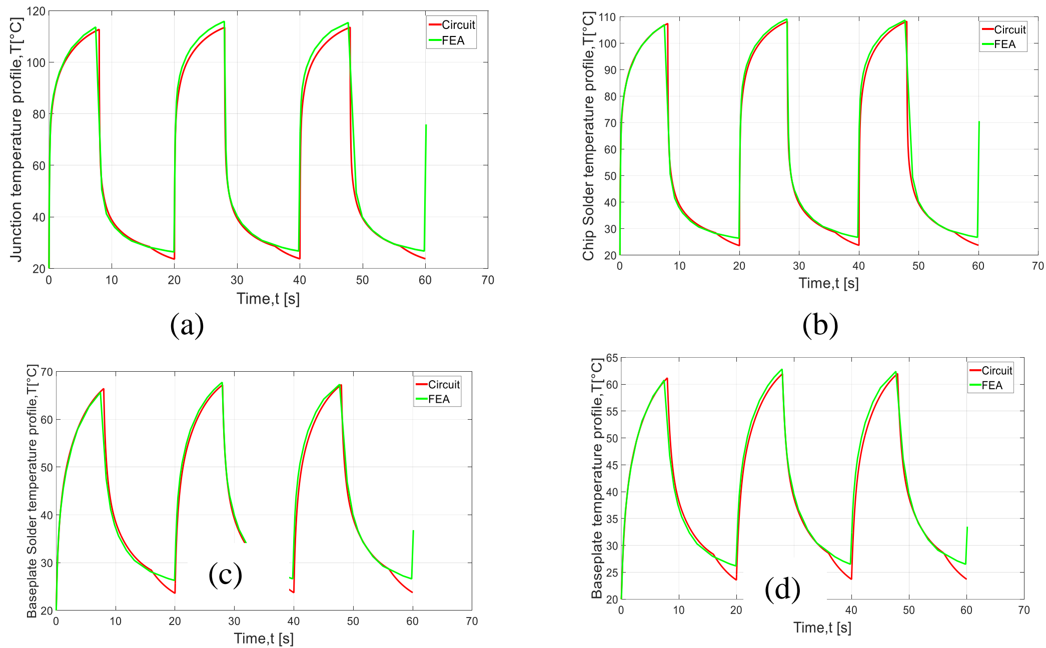


Figure 5.41 Dynamic temperature profile of IGBT at 0.05Hz pulsed power profile, Duty ratio-0.4 (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature.

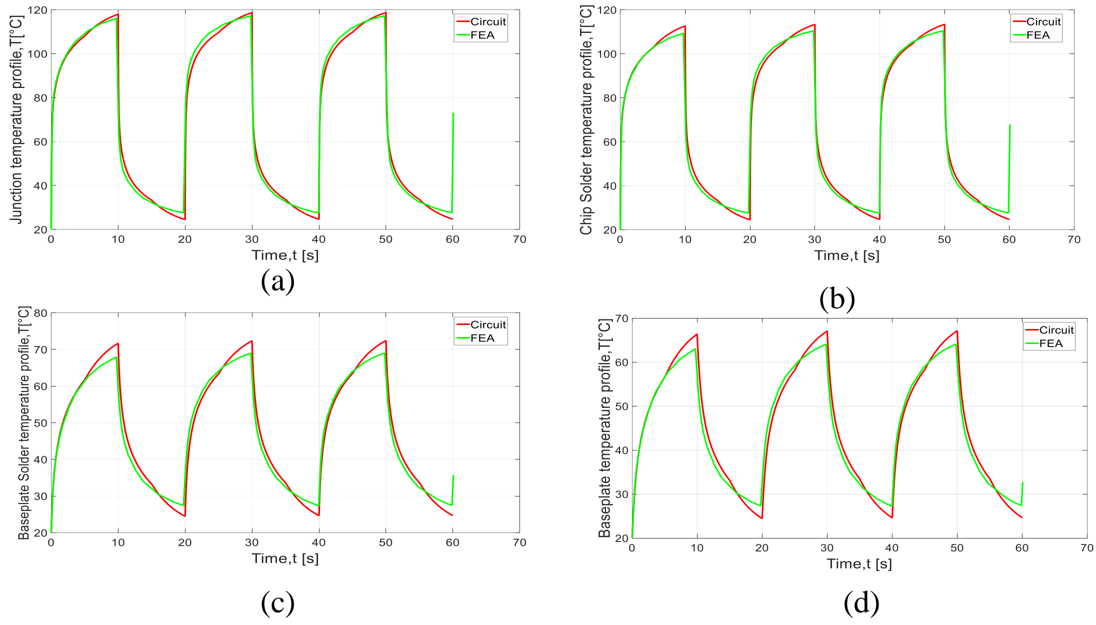


Figure 5.42 Dynamic temperature profile of IGBT at 0.05Hz pulsed power profile, Duty ratio- 0.5 (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature

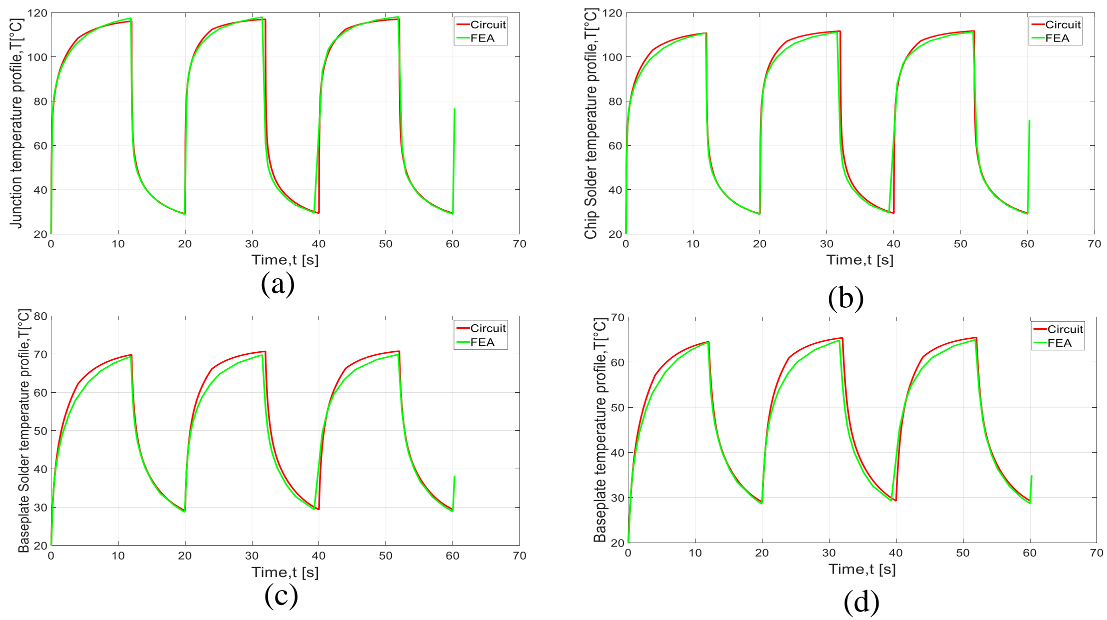


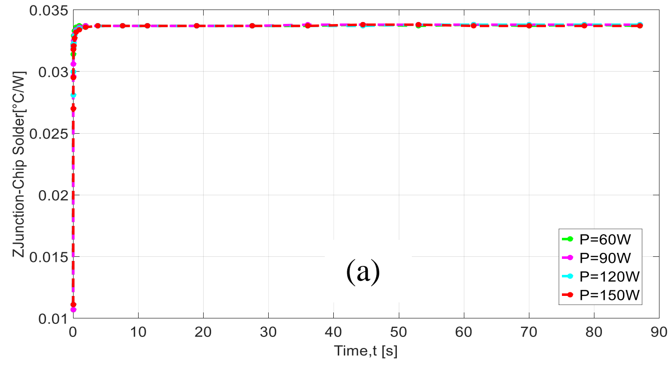
Figure 5.43 Dynamic temperature profile of IGBT at 0.05Hz pulsed power profile, Duty ratio-0.6 (a) Junction temperature (b) solder temperature (c) baseplate solder temperature (d) baseplate temperature.

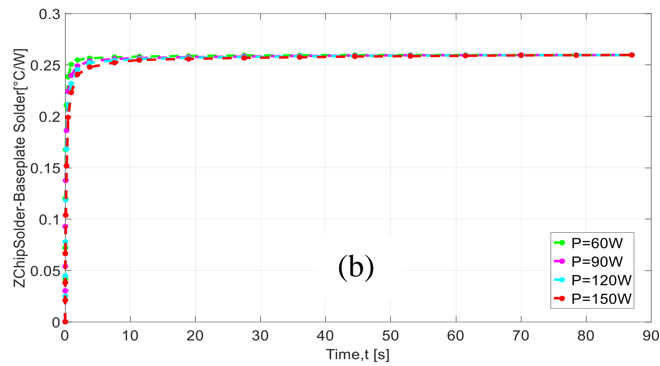
5.18 Impact of Boundary Condition on the Thermal Model

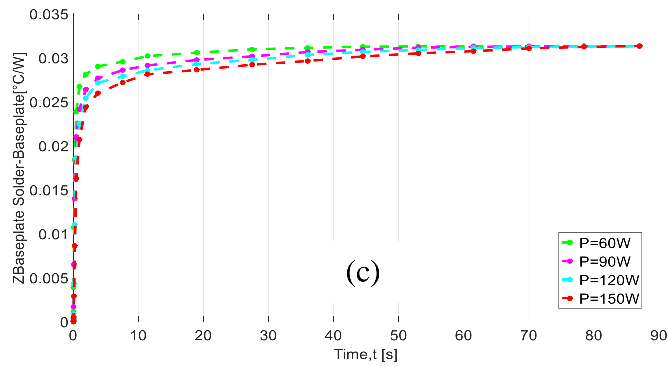
The above presented thermal model ensures detailed thermal information in the IGBT module but does not consider the impact of boundary conditions in the model. Obviously, in practice, the thermal boundary conditions vary. The neglected boundary conditions in the thermal model may generate discrepancies. The boundary conditions refer to the certain specific conditions which are needed to be satisfied at all or one part of the boundary of a design geometry in which a set of differential equations are to be solved. In general, boundary condition refers to the power dissipation and cooling system in the thermal model. Power dissipation in the IGBT and diode chips and the cooling system can be considered as the boundary conditions in the IGBT module. In order to evaluate the effect of thermal boundary conditions in the thermal impedance of IGBT module, firstly FEA simulations are conducted considering the variation of power losses and variation of cooling system boundary conditions and temperature responses are extracted in the corresponding nodes in the thermal network.

5.18.1 Study of Variation of Power Losses

FEA simulations are conducted to analyse the effect of heat sources on the thermal impedance of IGBT module. Simulation is performed with the fixed heat transfer coefficient equivalent to 3000 $Wm^{-2}K^{-1}$, different power loss profiles are applied in the IGBT chip, and it varies from 60W to 150W. The thermal impedance of the IGBT and diode under the different power losses loading are shown in Figure 5.44 and Figure 5.45 respectively. As it can be seen, the effect of variation on thermal impedance is more prominent in the thermal branches starting from chip solder to baseplate solder, baseplate solder to baseplate and baseplate to ambient. The reason is considered in this case that top layer is less thick than bottom layers, this results in low thermal impedance at top layer (from junction to chip solder) compared to bottom layers (from chip solder to ambient) and since the insulation layer has a high thermal capacitance, it slows down the heat transfer from upper layers to the heat sink. This heat blocking phenomenon causes the temperature difference between the upper and lower layers of the IGBT module which ultimately increases the thermal impedance.







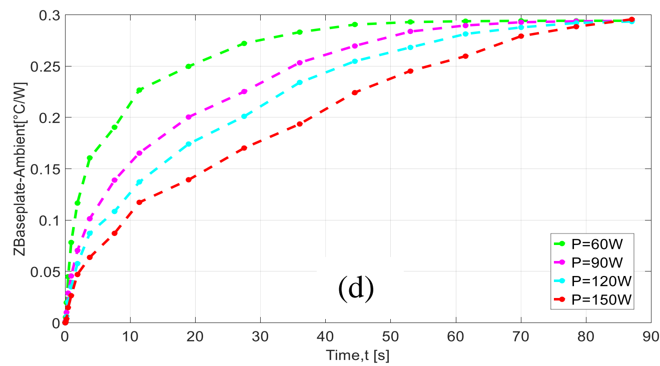


Figure 5.44 Transient thermal impedances of IGBT at interested layers for different power losses: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate (d) baseplate to ambient.

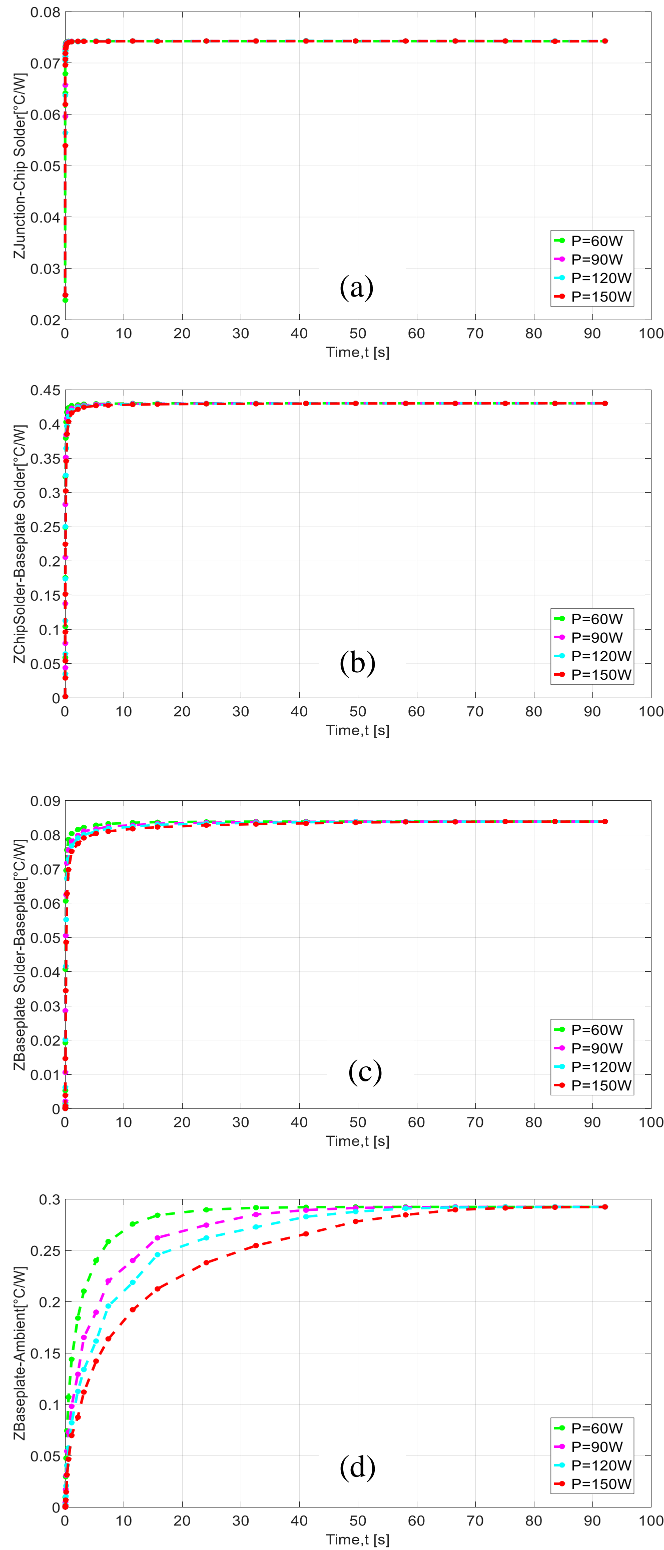


Figure 5.45 Transient thermal impedances of Diode at interested layers for different power losses: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate (d) baseplate to ambient.

5.18.2 Study of Variation of Cooling system

In this section, thermal impedances of IGBT module are studied under the variation of the cooling system. In all cases, power dissipation of 110W is applied at the top surface of IGBT chip as heat source boundary conditions and conditions for representing the varying fluid cooling systems heat transfer coefficient is varied. It is applied at the base plate as convective boundary condition. It is varied in the ranges of $1000 < h < 10000\ Wm^{-2}K^{-1}$. The transient thermal impedances of the IGBT and the diode under different h are shown in Figure 5.46 and Figure 5.47 respectively. As it is seen, the changes of thermal impedance are more prominent in the thermal branches starting from baseplate node to reference node (cooling fluid temperature) due to its proximity to the heat sink.

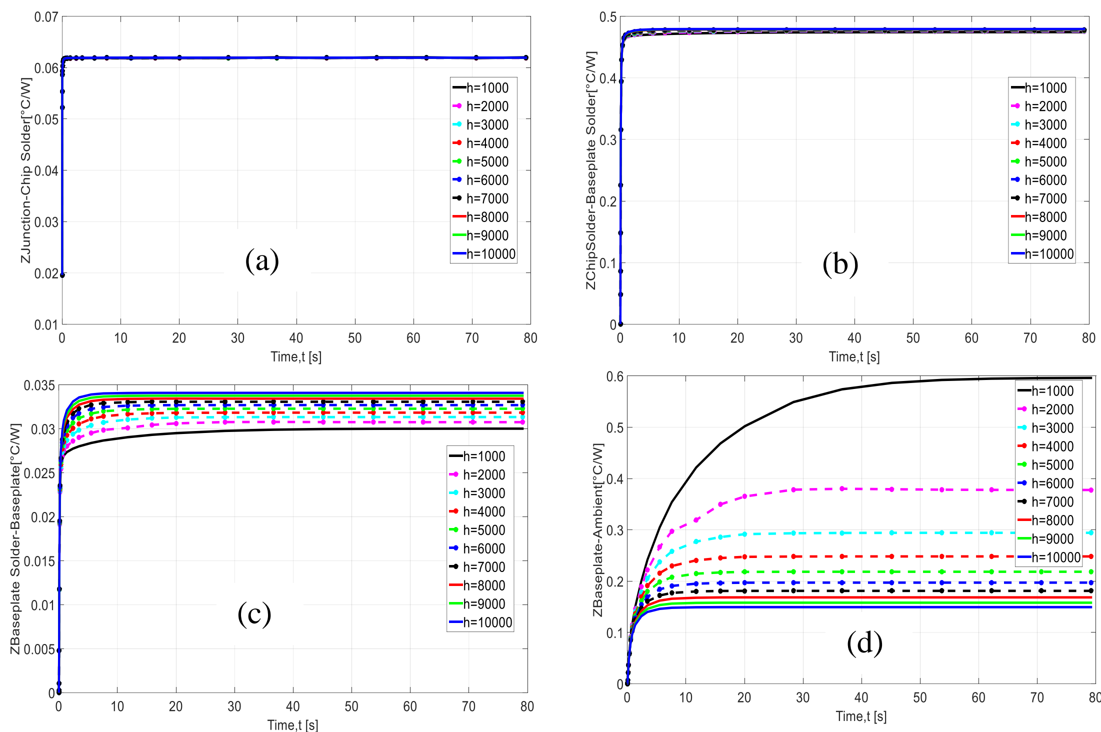


Figure 5.46 Transient thermal impedances of IGBT at interested layers for different heat transfer coefficients: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate (d) baseplate to ambient.

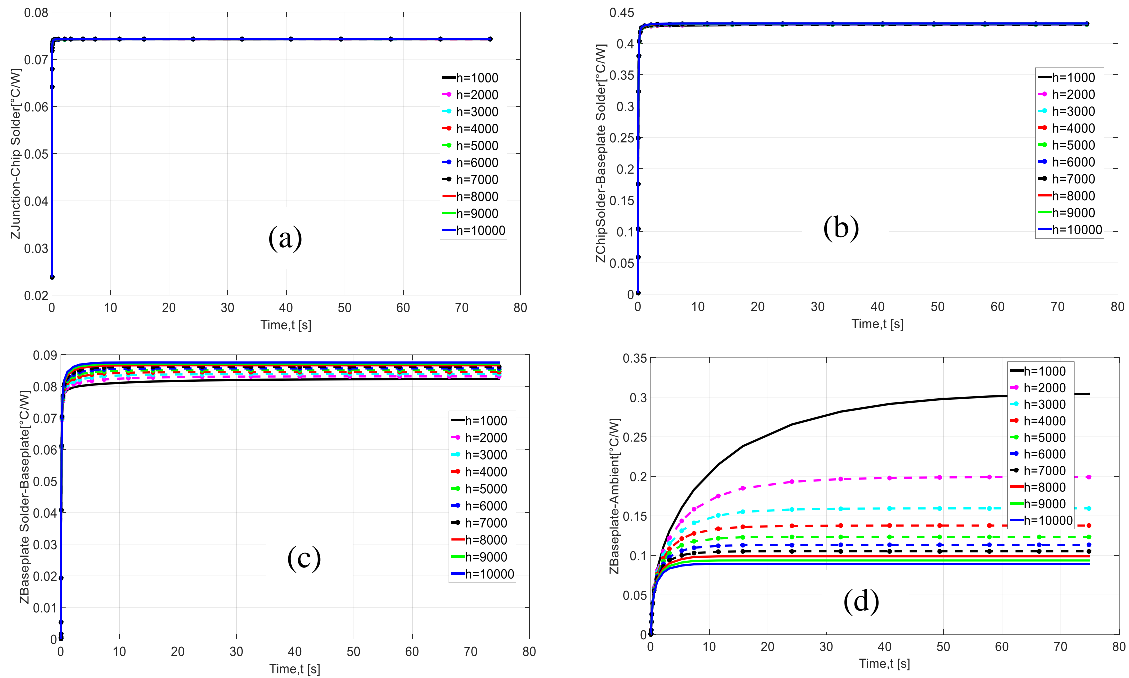
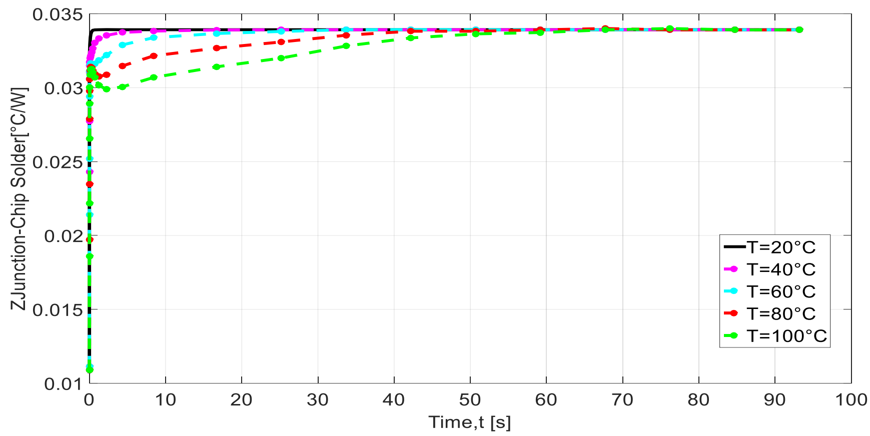


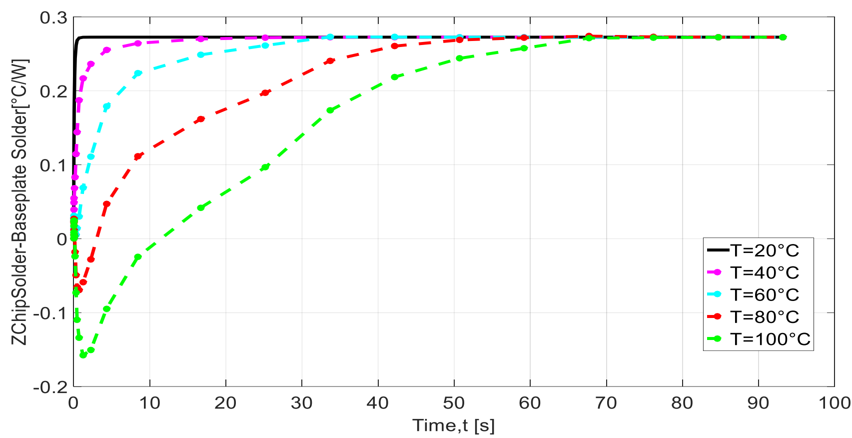
Figure 5.47 Transient thermal impedances of diode at interested layers for different heat transfer coefficients: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate (d) baseplate to ambient.

5.18.3 Study of Variation of Baseplate Temperature

To analyse the impact of power module baseplate temperature variation on the thermal impedance of IGBT module beneath the baseplate of the module, reference temperature is set to the different value of fixed temperature. In this case study, baseplate temperature is changed in the range of 20 °C to 100 °C. The results for the IGBT and the diode under the variation of baseplate temperature are shown in Figure 5.48 and Figure 5.49 respectively. As it is seen, the most affected thermal branch initiates from the chip solder to baseplate solder node. The reason is considered in this case that the heat flow is blocked by thick baseplate surface of the module and thermal capacitance contributed by thick baseplate slows heat flow from the chip to the sub-layers. This heat blocking phenomenon causes the temperature to be trapped in top layers of the power module structure.



(a)



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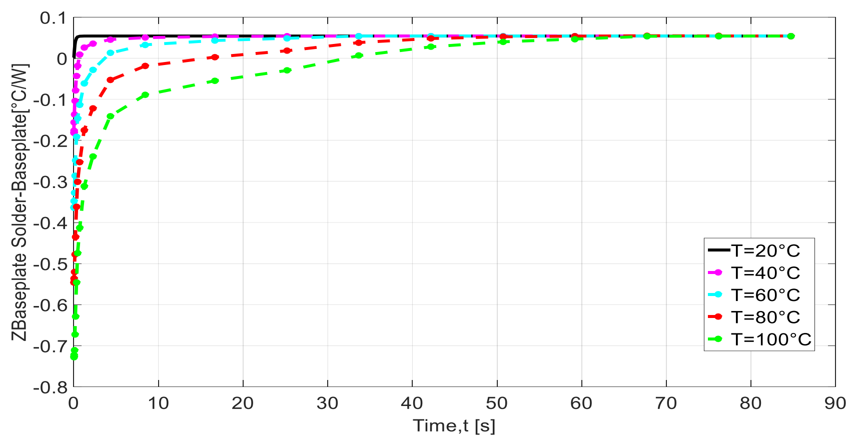
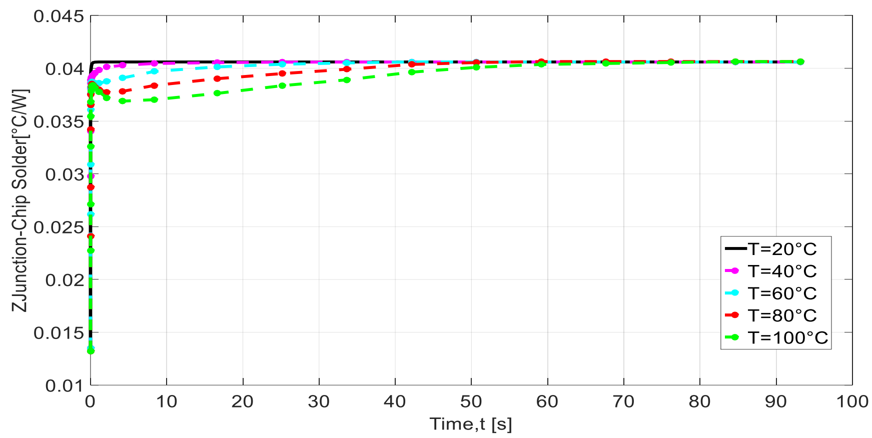
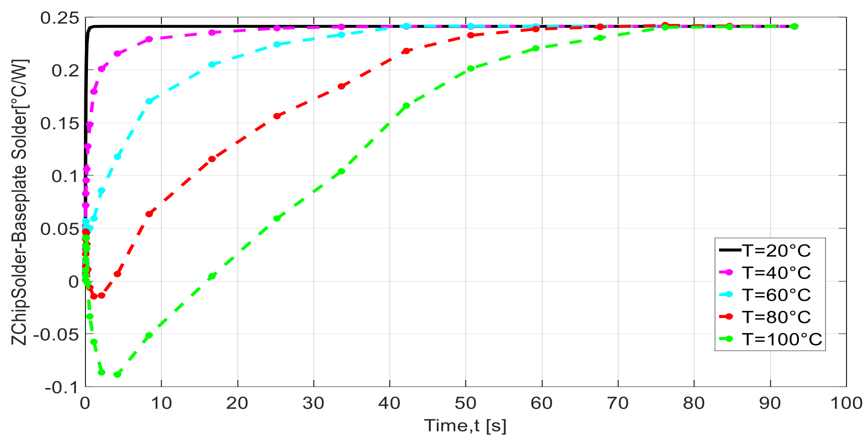


(c)

Figure 5.48 Transient thermal impedances of IGBT at interested layers for different baseplate temperature: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate.



(a)



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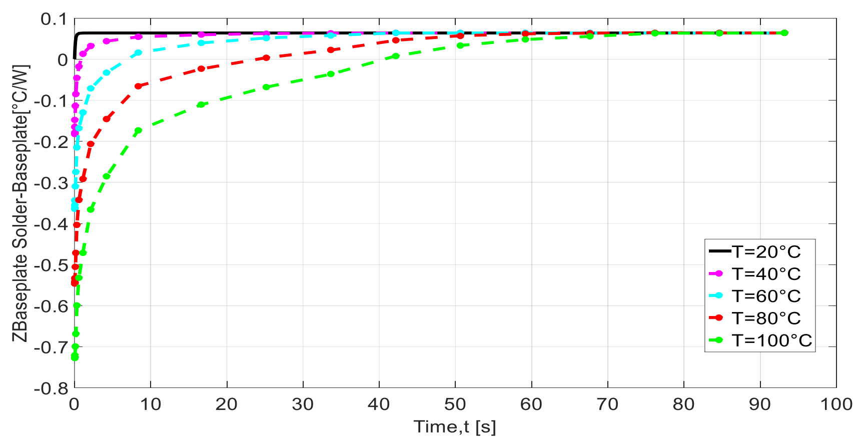


(c)

Figure 5.49 Transient thermal impedances of diode at interested layers for different baseplate temperature: (a) Junction to chip solder (b) chip solder to baseplate solder (c) baseplate solder to baseplate.

5.19 Transformation of Boundary Conditions from FEA to Lumped RC Thermal Network

Typically boundary conditions vary based on converter operating conditions. It is important to translate the varying boundary conditions. It is challenging to take this account into the compact thermal model. Moreover, it is difficult to implement in circuit simulators. This translation can be performed by exploiting transient response analysis for the varying boundary conditions in FEA as described in section 5.18 and then this can be used to develop a generic thermal model. To make the modelling simple, in the curve fitting approach to the transient responses, a 1st order RC network is used. The curve fitted expression of RC element values with respect to the different power loss profiles for both IGBT and diode are shown in Figure 5.50 and Figure 5.51 respectively.

These RC network parameters are then mathematically curve fitted to find the generic model for various power loss profiles. In the given curves, the horizontal axis presents different power loss profiles, the vertical axis presents the corresponding thermal resistance and thermal capacitance values. The least square fitting method is applied to derive accurate RC model parameters [188]. The value of R is shown in all the figures and it is maintained in the range of 0.8 to 0.9. The curve fitted RC elements for variation of heat transfer coefficient and baseplate temperatures for the IGBT and the diode are shown in Figure 5.52, Figure 5.53, Figure 5.54 and Figure 5.55 respectively. The generic thermal model for both IGBT and diode in respect to the various power loss profiles, heat transfer coefficient and baseplate temperature are shown in Figure 5.56.

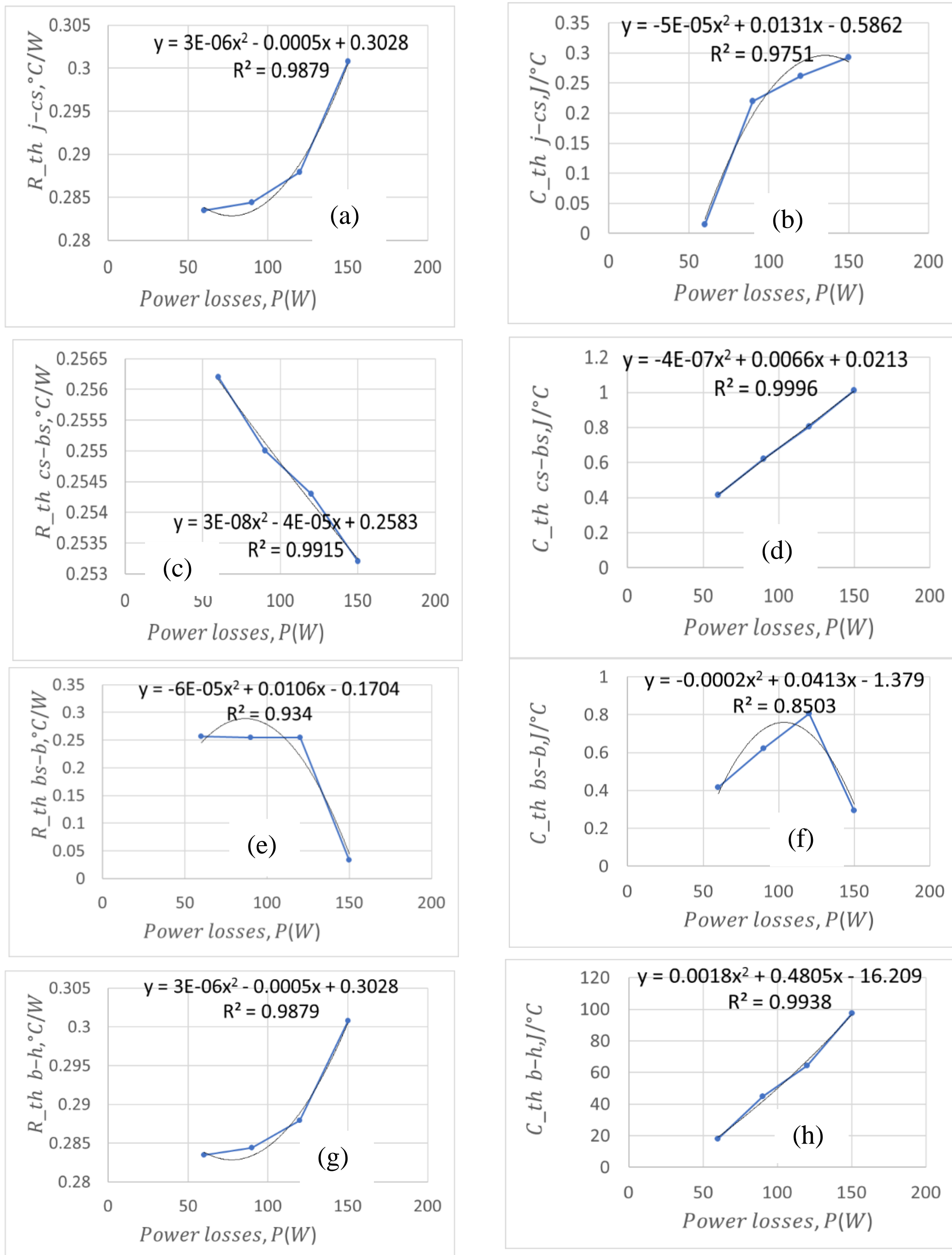


Figure 5.50 Curve-fitted transient thermal impedances of IGBT at interested layers for different power losses : (a) Junction to chip solder thermal resistance (b) Junction to chip solder thermal capacitance (c) chip solder to baseplate solder thermal resistance (d) chip solder to baseplate solder thermal capacitance (e) baseplate solder to baseplate thermal resistance (f) baseplate solder to baseplate thermal capacitance (g) baseplate to ambient thermal resistance (h) baseplate to ambient thermal capacitance.

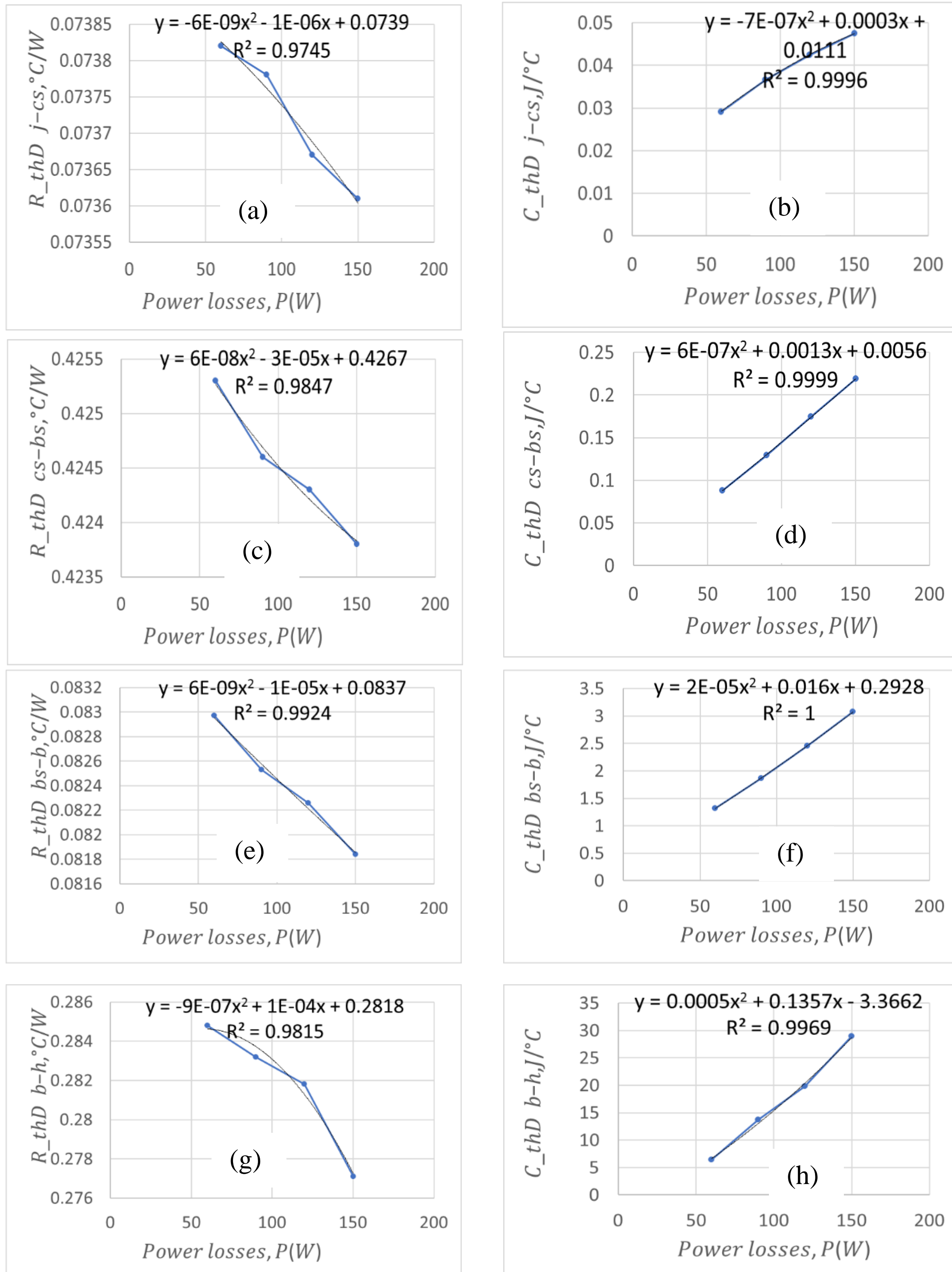


Figure 5.51 Curve-fitted transient thermal impedances of Diode at interested layers for different power losses : (a) Junction to chip solder thermal resistance (b) Junction to chip solder thermal capacitance (c) chip solder to baseplate solder thermal resistance (d) chip solder to baseplate solder thermal capacitance (e) baseplate solder to baseplate thermal resistance (f) baseplate solder to baseplate thermal capacitance (g) baseplate to ambient thermal resistance (h) baseplate to ambient thermal capacitance.

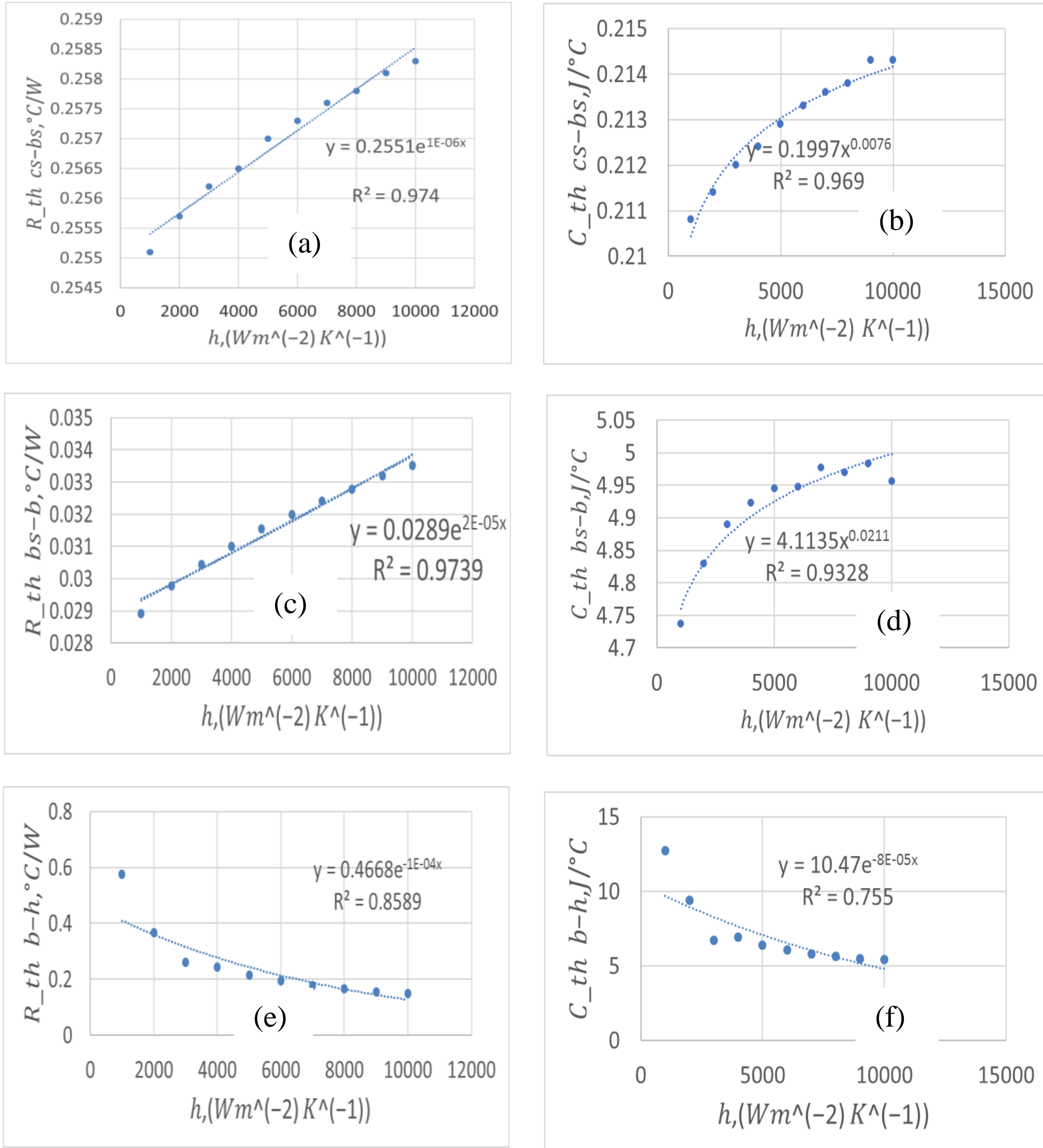


Figure 5.52 Curve-fitted transient thermal impedances of IGBT at interested layers for different heat transfer coefficients: (a) Chip solder to baseplate solder thermal resistance (b) chip solder to baseplate solder thermal capacitance (c) baseplate solder to baseplate thermal resistance (d) baseplate solder to baseplate thermal capacitance (e) baseplate to ambient thermal resistance (f) baseplate to ambient thermal capacitance.

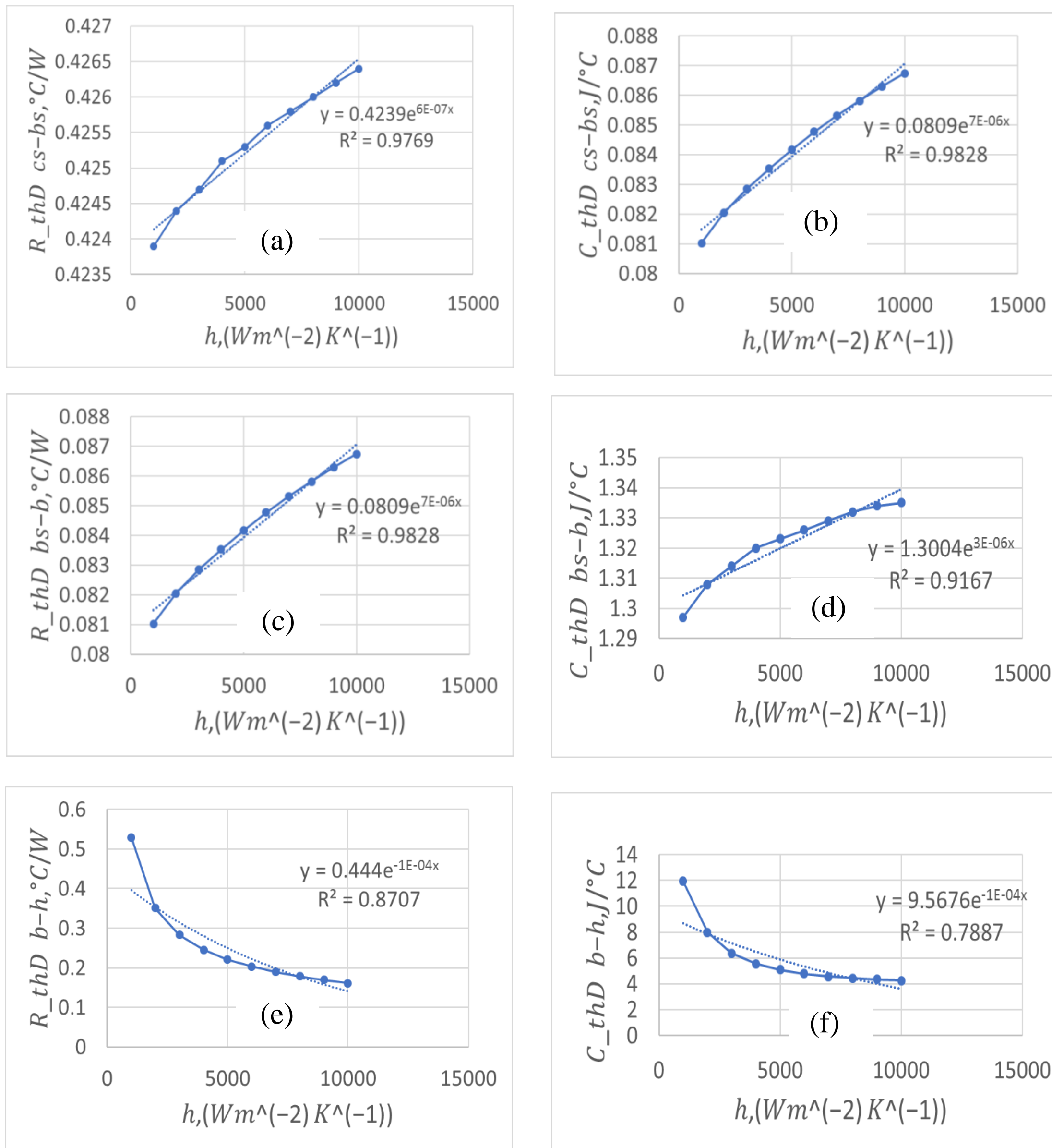


Figure 5.53 Curve-fitted transient thermal impedances of diode at interested layers for different heat transfer coefficients: (a) Chip solder to baseplate solder thermal resistance (b) chip solder to baseplate solder thermal capacitance (c) baseplate solder to baseplate thermal resistance (d) baseplate solder to baseplate thermal capacitance (e) baseplate to ambient thermal resistance (f) baseplate to ambient thermal capacitance.

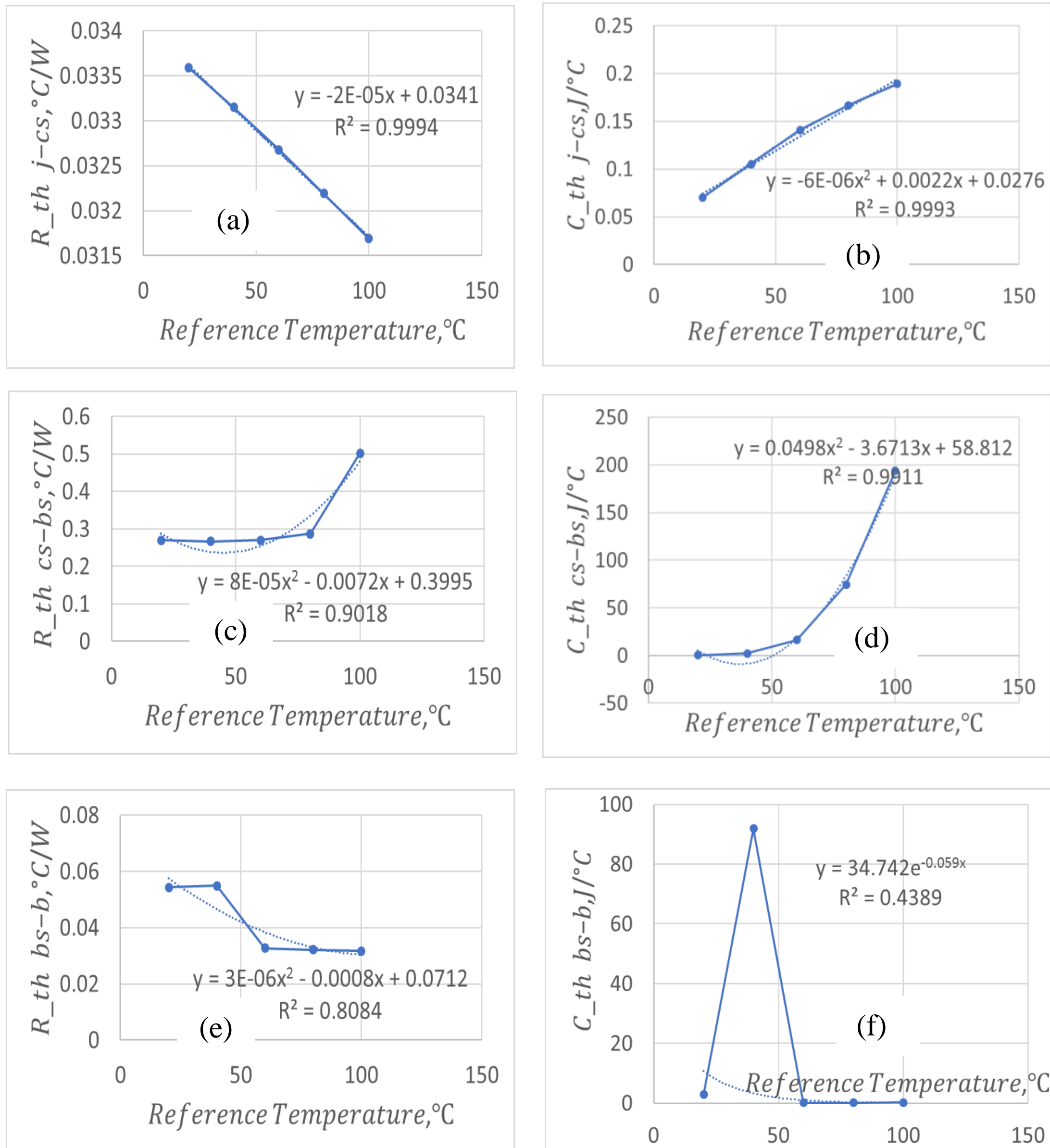


Figure 5.54 Curve-fitted transient thermal impedances of IGBT at interested layers for different baseplate temperatures: (a) Junction to chip solder thermal resistance (b) Junction to chip solder thermal capacitance (c) chip solder to baseplate solder thermal resistance (d) chip solder to baseplate solder thermal capacitance (e) baseplate solder to baseplate thermal resistance (f) baseplate solder to baseplate thermal capacitance.

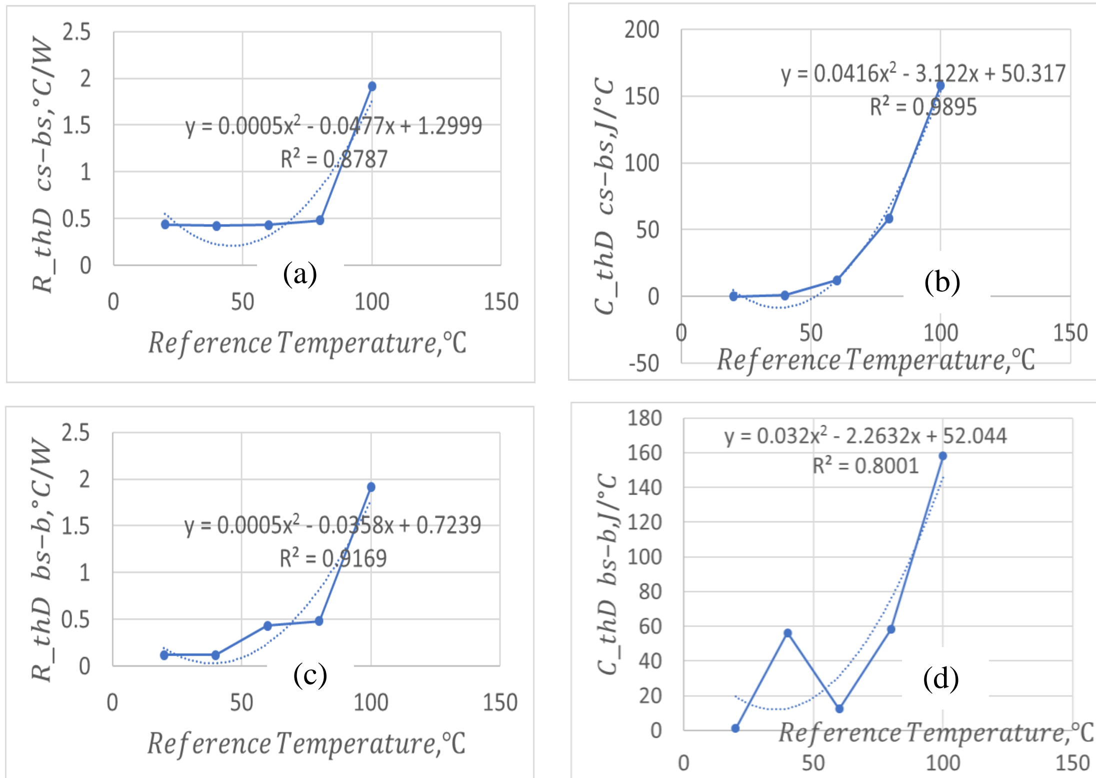
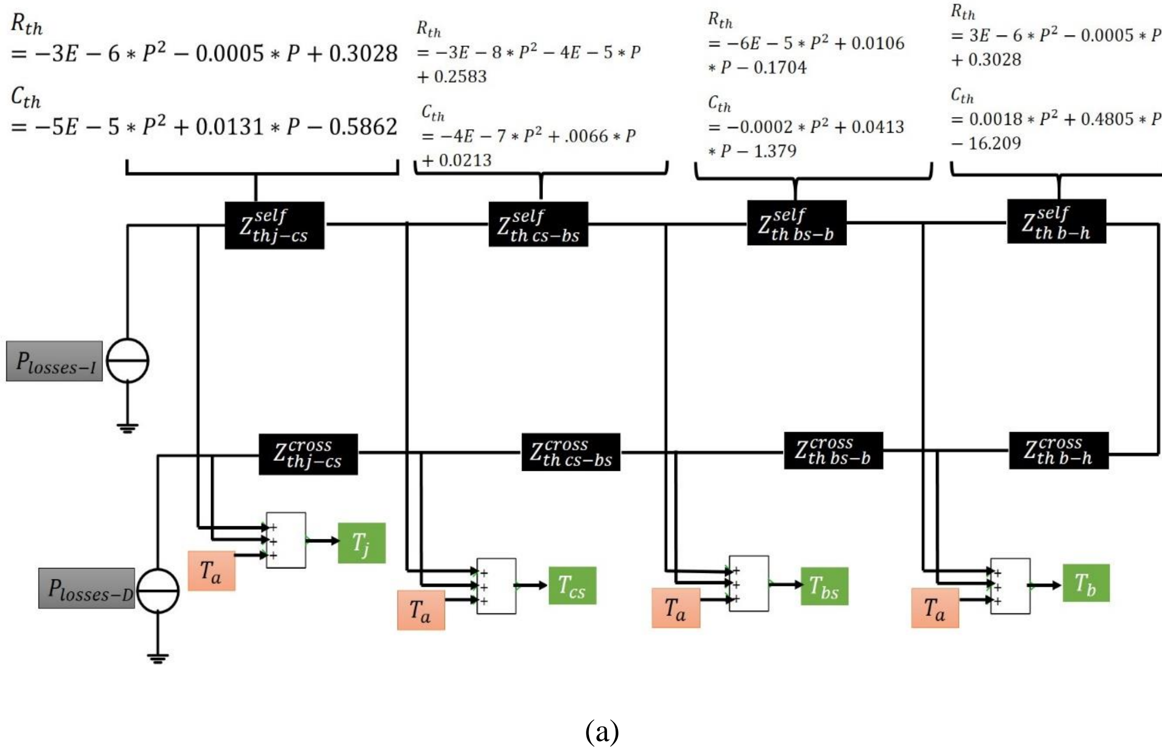


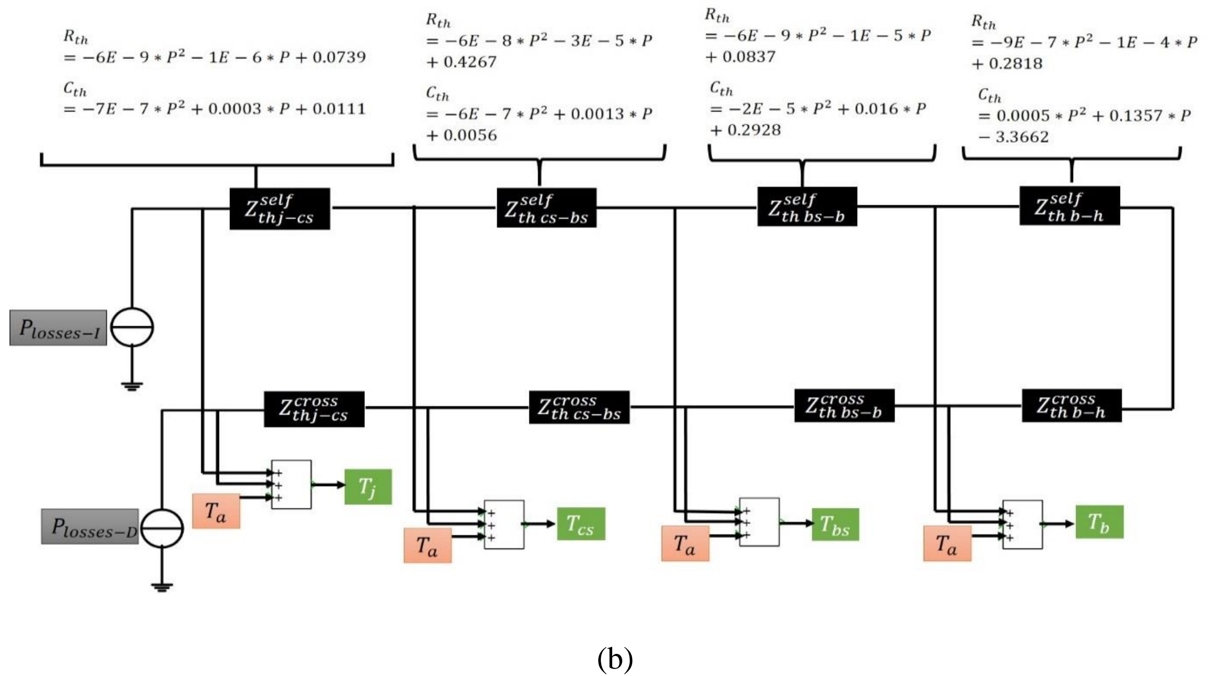
Figure 5.55 Curve-fitted transient thermal impedances of Diode at interested layers for different baseplate temperatures: (a) chip solder to baseplate solder thermal resistance (b) chip solder to baseplate solder thermal capacitance (c) baseplate solder to baseplate thermal resistance (d) baseplate solder to baseplate thermal capacitance.

Since the thermal model is influenced by the operating boundary conditions, the thermal model parameters need to be expressed as a function of operating conditions. A thermal network description is shown in Figure 5.56 where its thermal impedance branch network parameters for node to node is set as boundary condition dependent. The proposed model can take into account the variation of loading conditions and predict the temperatures acquiring the feedback from the changes in operating conditions with high accuracy and perform simulation quickly. A detailed flowchart of parameter extraction for adapting the changes of operating boundary conditions is illustrated in Figure 5.57. In this figure, block 1 describes the FEA transient step response under different boundary conditions. Block 2 represents the transformations of transient thermal impedance curves. Block 3 illustrates a first order RC network by curve fit approach in terms of determining operating boundary condition variable. Block 4 describes the adjusted RC parameters that have been achieved by curve fit. Block 7 describes the estimation of heat transfer coefficient for the operating cooling system. Block 8

to 10 illustrates the boundary conditions required to tune the RC elements. Using the converter specifications, power losses are estimated in Block 5. Finally, the thermal model estimates the temperature at the intended points of multiple locations in the component using the derived power loss profiles, reference temperature and RC thermal network parameters.



(a)



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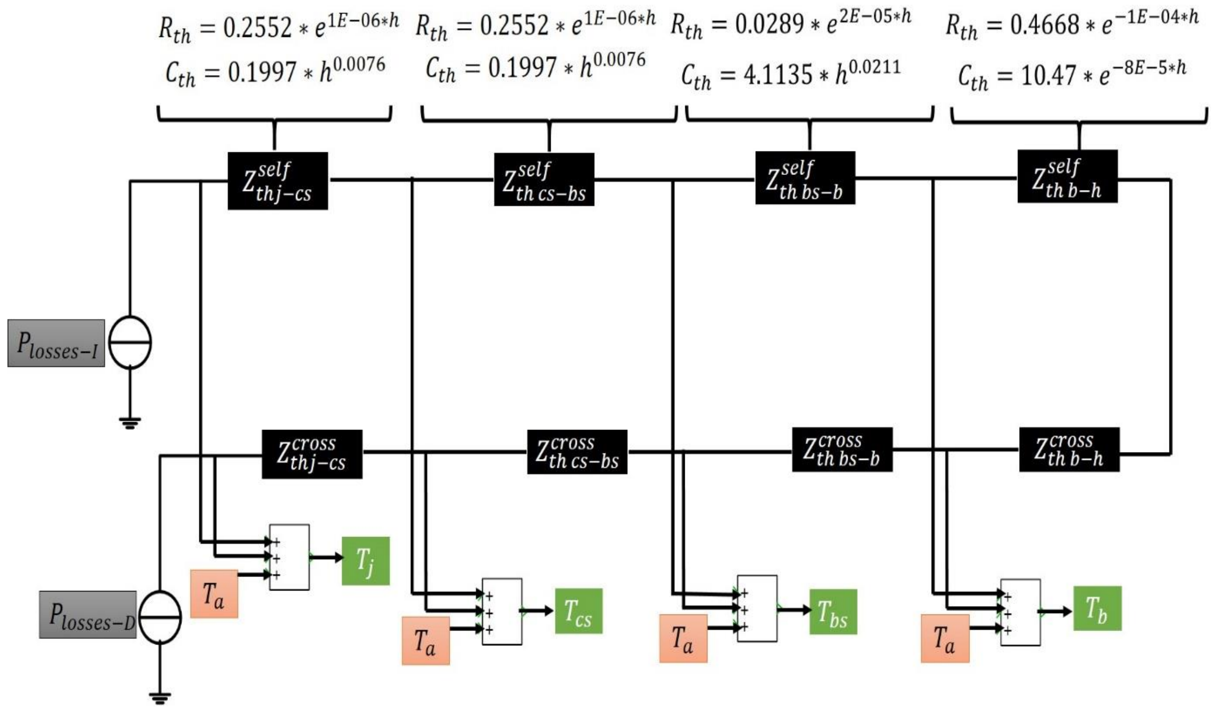

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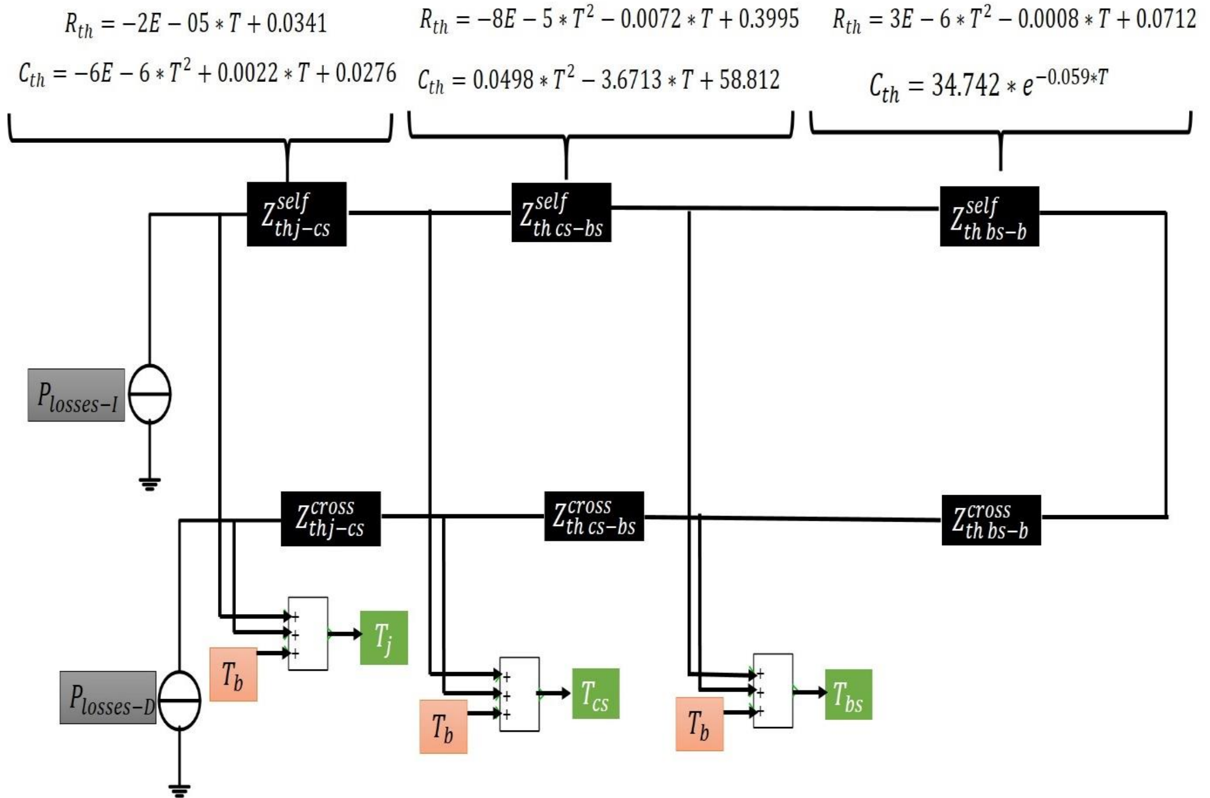

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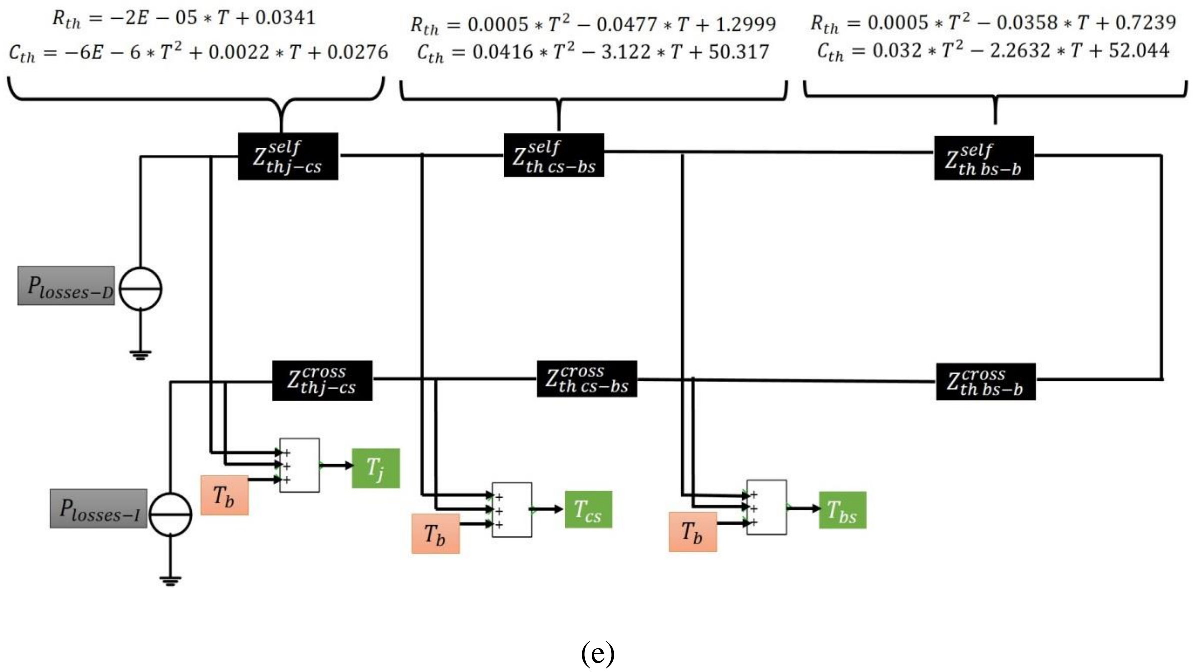


(e)

Figure 5.56 Detailed thermal model taking into account the effect of varying boundary conditions (a) IGBT-variation of power losses (b) Diode-variation of power losses (c) IGBT-variation of cooling system (d) IGBT-variation of case temperature (e) Diode-variation of case temperature.

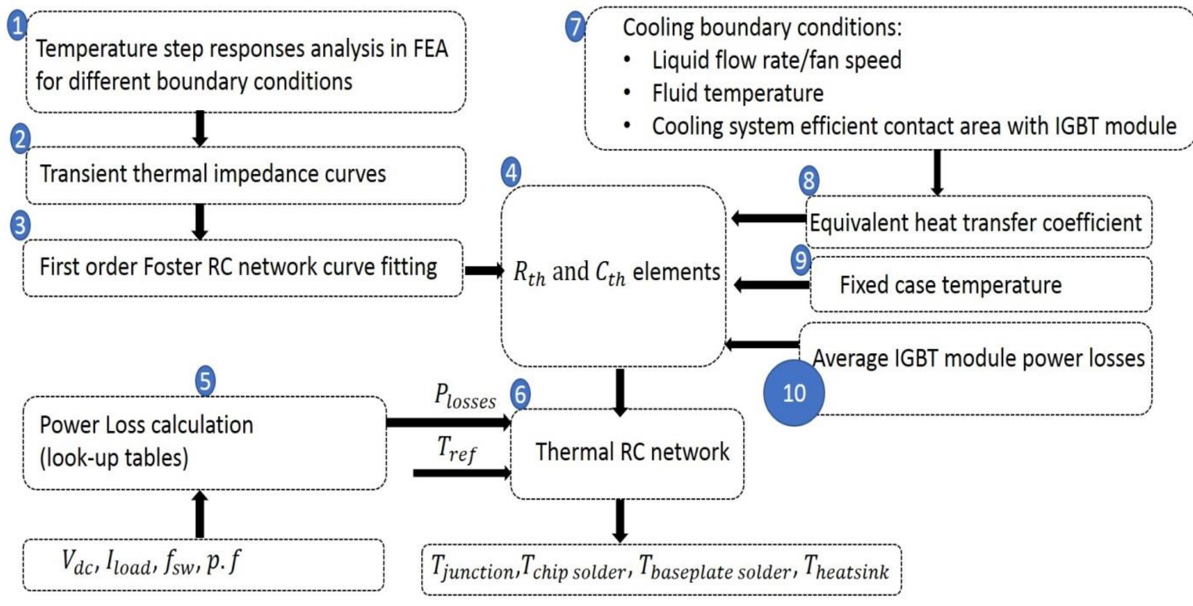


Figure 5.57 Detailed description of thermal model taking into account the effect of varying boundary condition.

5.20 Verification of Lumped RC Thermal Network

In order to validate the thermal model under varying operating conditions, the converter specifications are selected as the Table 35. Initially, the validity of a 1st order RC Foster network is compared to a 3rd order Foster network. It is seen from the Figure 5.58 that the temperature predicted by 1st order model is consistent with 3rd Foster network model. The derived model for the varying conditions is implemented for the testing boundary conditions (a) variation of power losses,$P_{loss-IGBT} = 158W$ and $P_{loss-Diode} = 30W$ (b) variation of heat transfer coefficient, $h = 3000\ Wm^{-2}K^{-1}$ (c) variation of baseplate temperature, $T_{baseplate} = 40°C$. As it is illustrated in Figure 5.58, a 1st order RC Foster network can predict the temperature with high accuracy comparing to a 3rd order RC Foster network. So, a 1st order RC Foster network can be used to verify the thermal model under varying boundary conditions loading.

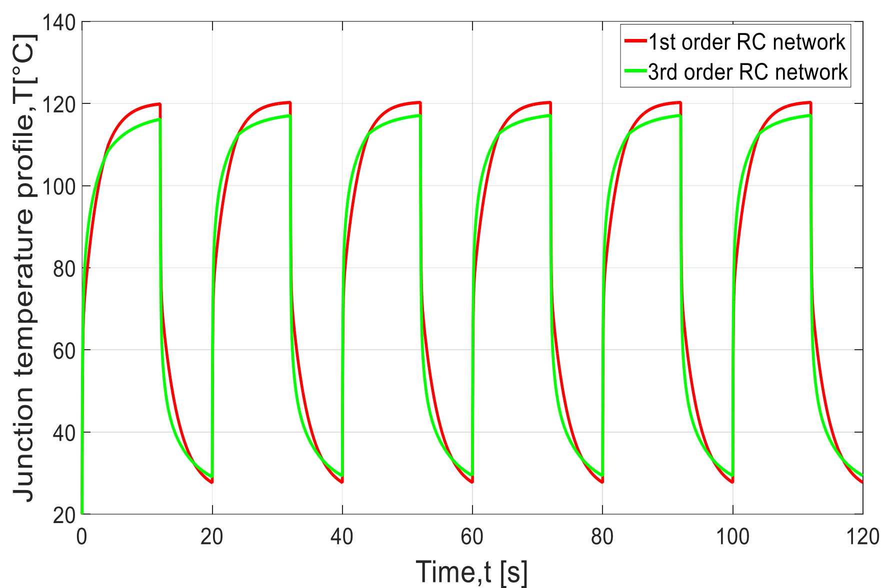
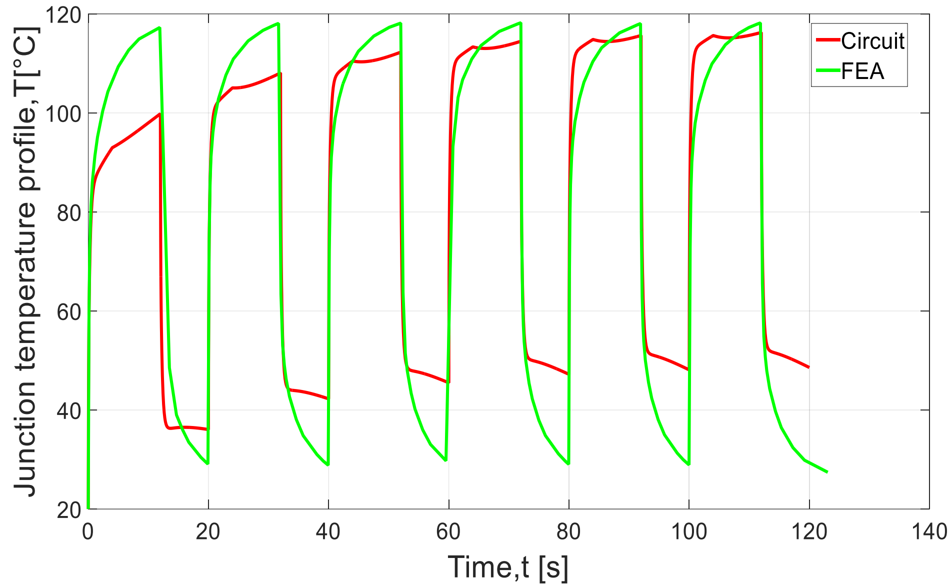


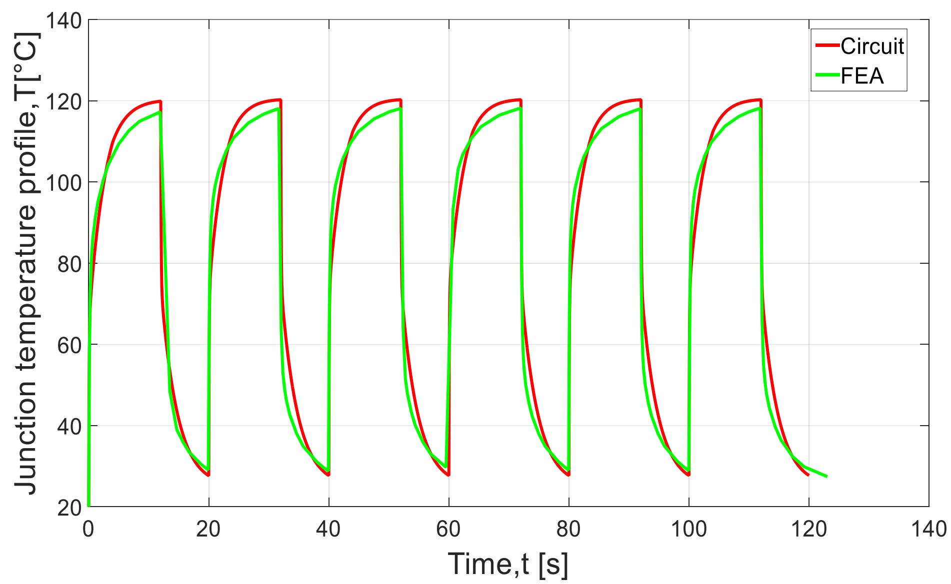
Figure 5.58 Temperature predicted by 1st order RC Foster network comparing to 3rd order RC Foster layered network

The predicted junction temperature results for IGBT chip are illustrated for the cases (a) variation of power losses,$P_{loss-IGBT} = 158W$ and $P_{loss-Diode} = 30W$ (b) variation of heat transfer coefficient, $h = 3000\ Wm^{-2}K^{-1}$ (c) variation of baseplate temperature, $T_{baseplate} = 40°C$.

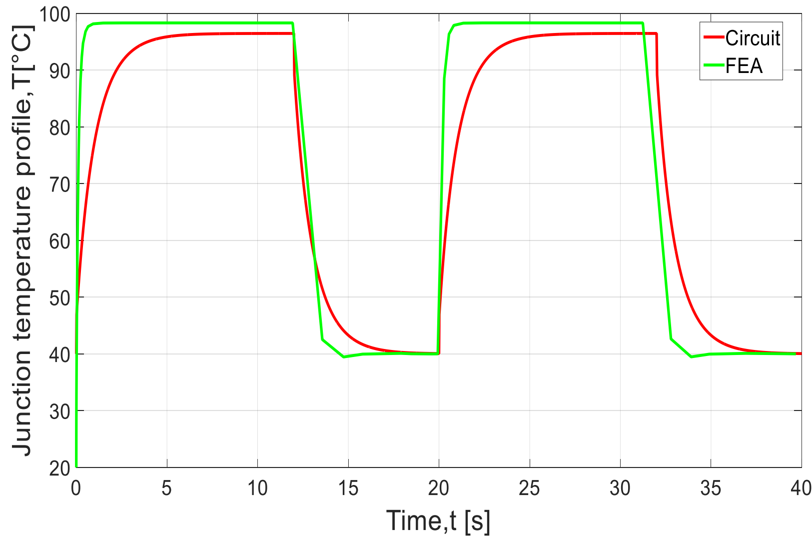
As it is shown in Figure 5.59, the result of the proposed thermal model is in good agreement with the FEA result. The errors between circuit-based compact thermal model and FEA analysis for all the tested cases are less than 1-4%.



(a)



(b)



(c)

Figure 5.59 Junction temperature of IGBT predicted by circuit and comparing to FEA model in varying boundary conditions (a) variation of power losses, $P_{loss-IGBT} = 158W$ and $P_{loss-Diode} = 30W$ (b) variation of heat transfer coefficient, $h = 3000\ Wm^{-2}K^{-1}$ (c) variation of baseplate temperature, $T_{baseplate} = 40°C$.

5.21 Conclusions

In this chapter, an electro-thermal interaction analysis of a switch that contains an IGBT and a diode in a half-bridge module of a three-phase voltage source inverter has been presented. The electro-thermal model includes the electrical model of the inverter and the loss model of both IGBT and diode and the detailed thermal model that represents the self-heating and cross-heating between the IGBT and diode. The lumped RC Foster cell parameters of the thermal model have been synthesised by transient responses of FEA analysis under different operating boundary conditions. The curve fit approach has been applied to the step responses to extract self-heating and thermal-coupling foster network parameters. On top of that, the effect of varying boundary conditions on the thermal model has been investigated. It is seen that employing large heat transfer coefficients results in the thermal blocking behaviour inside the IGBT module particularly the area between junction to case. The reason is considered less heat spreading inside the junction to case and this cause the junction to case thermal impedance high and thereby decrease heat propagation. The presented thermal model is verified by the FEA analysis. It is also accurate in contrast to the FEA model. In summary, the model is highly consistent with the FEA model and error is low compared to the FEA

analysis. The performance of proposed thermal model is fast in the context of simulation speed and it can be easily integrated and implemented in circuit simulator particularly for predicting the temperature in the critical locations of the components. Moreover, the presented thermal model predicts the temperatures in the solders where it is difficult to measure by experiments and these temperature profiles can be used for the reliability analysis of components under the long realistic loading conditions. It is worth to mention the limitations of the presented thermal model in general that the RC parameters of the model is not fixed and change with the physical structure of the components and material properties. However, the structure of the presented thermal model can be applied in all cases.

Chapter 6 Electro-thermal Analysis of Hybrid Vehicle Converter

Typically, a compact power electronic converter contains power semiconductor switching components. These are mounted on the substrate closely to each other. The proximity of the components causes the barrier to the thermal path and thereby accelerates thermal interaction. Semiconductor devices in a compact converter dissipate power at electrical loading conditions. These losses are dissipated in the form of heat. Therefore, the thermal management of the switching components in power dense converter has been an important issue to guarantee the reliable performance of the converter. This chapter investigates the evaluation of modelling performance of the proposed framework comparing with the temperature profiles obtained experimentally for the IPT-based boost converter.

6.1 Case Study on Hybrid Vehicle Converter

To evaluate the performance of the proposed modelling technique, the case study on a power electronic converter rated at 1.5 kW is carried out as an example. To model this, the information related to this converter is taken from the literature available in the form of thesis [197]. In this work, the component interaction between switches is focused. The temperature prediction of the component is analysed considering the self-heating and mutual heating coupling effects in the thermal model. The step by step modelling of the component interaction analysis is outlined below.

6.1.1 Topology and Specification of the Converter

As shown in Fig. 6.1, the full-scale power electronic converter features in applications such as battery electric vehicles, hybrid electric vehicle and hydrogen fuel-cell electric vehicle. The converter configuration is equipped with inter-phased transformer (IPT) and power electronic switch. Particularly, this topology has three attractive features. These are high current handling ability, benefit of interleaving techniques at high switching frequency and reduced size of filter components. Considering these features an interleaved topology seems potentially efficient for a power dense (12V to 48V) automotive DC-DC converter application. An IPT based dual interleaved bidirectional boost converter, as shown in Figure 6.2 is applied, which is relatively simple structure with few components. Specifications of the converter topology are listed in Table 47.

Figure 6.1 Typical powertrain configuration of a plugin hybrid electric vehicle [197].

Figure 6.2 IPT based dual interleaved bidirectional boost converter [197].

Table 47 Converter parameters for the case study [197]

Topology	Interleaved boost converter
Rated Output Power P_{rated}	1.5 kW
Input Voltage V_{in}	12V
Output Voltage V_{out}	48V
Input Current Ripple ΔI_{ripple}	10%
Output Voltage ripple ΔV_{ripple}	10%
Switching frequency f_s	40kHz
Load Resistance	1.5**Ω**
Infrared camera	FLUKE TiS 10
IRF7759L2TRPBF-FET	75V/96A

6.1.2 Structure of the Components

To model the interaction between the switches of the converter, losses in the all switches are treated as heat sources in the FEA thermal model. Each switch can be represented as a discrete chip package. Each switch is soldered to T-CLAD board by the pad. T-CLAD board consists of three layers. Layers are copper, dielectric and aluminium. The T-CLAD board is connected to the heat sink by thermal interface layer. Copper bar is used as upper heatsink due to its high thermal conductivity and it is also connected by the thermal pad. For simplicity, the can to drain layer has been avoided. Also, it is difficult to derive the inner dimension of the can to drain layer from the package geometric details. It has been assumed that most of the heat will be directed downward either bottom or upward heatsink. Less heat will be transferred through the can to drain layer. Thermal modelling of FET switch is considered from the structure that has been taken from the reference [198]. Figure 6.3 describes the FET component internal detailed geometric structure and Table 48 gives the successive materials that constitute the package structure as represented in the converter. The thermal analysis in this research focuses on four switches experiencing strong thermal coupling due to their proximity to each other and dissimilar power distributions. The dissimilar power distributions are a result of the different circuit function of each switch in the converter circuit. The power distribution of T2 and T4 exhibits the conventional converter loss. The power distribution of T1 and T3 is much different and has low power losses

compared to T2 and T4 as diode losses occurs in the T1 and T3. The interaction between the chips T1, T2, T3, and T4 are the focus of this research.

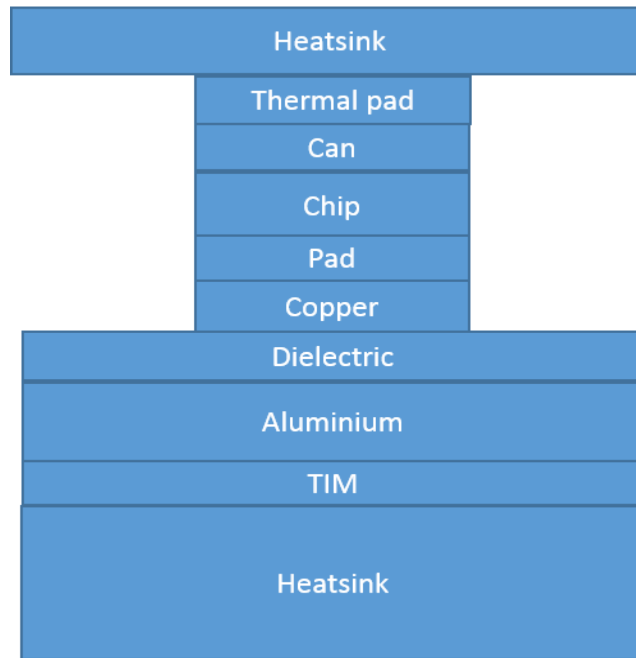


Figure 6.3 FET component internal structure [198].

Table 48 Component structural details [198].

Layers	Thickness	Dimension (L*W) in mm
Upper heatsink	1mm	35*10
Thermal pad	1mm	6.85*5.9
Can	1.5mm	6.85*5.9
Chip	0.25mm	6.85*5.9
Pad	0.1mm	4.85*3.9
Copper	70 μm	4.85*3.9
Dielectric	76 μm	9*6
Aluminium	1.02mm	9*6
TIM	50μm	150*100
Heatsink	35mm	150*100

6.1.3 Thermal Cross-coupling effects

The considered converter topology contains four switches. All the switches dissipate heat and interact with each other because all the chips share the same T-Clad board and the board is attached to the heatsink by thermal grease. So, when one switch is powered, T-CLAD board, heatsink and neighbouring switches will be heated up. This interaction can be described as thermal cross-coupling effect. The switches are labelled as T1, T2, T3 and T4 respectively.

Since the thermal coupling cannot be avoided, thermal coupling effects need to be considered carefully in the thermal model. Four switches are active in this topology. Therefore, four self-heating and four mutual –heating thermal impedances should be calculated as it shows in Figure 6.4.

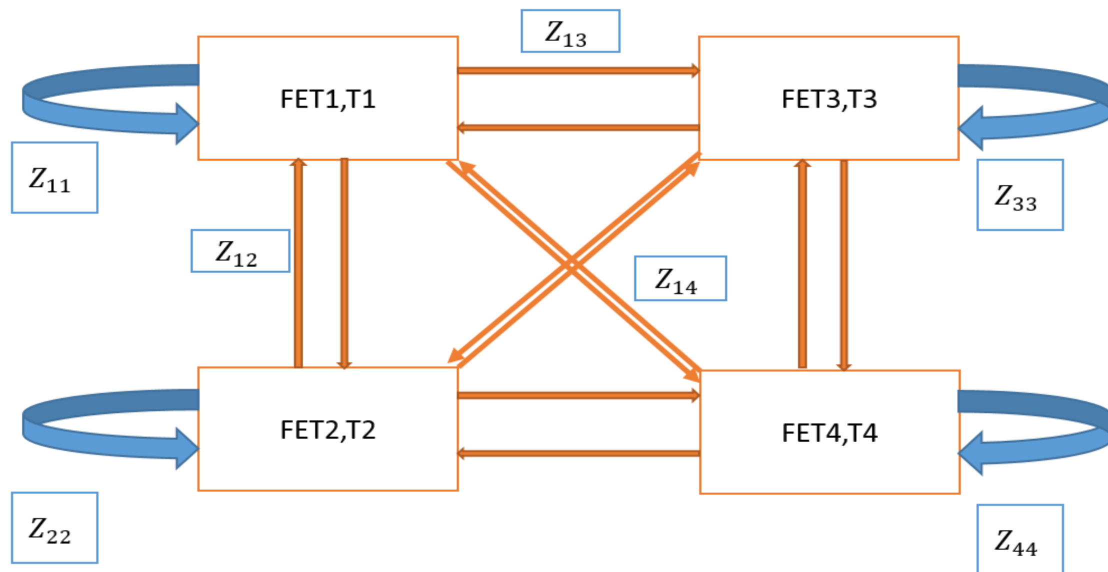


Figure 6.4 Impedance model description due to self-heating and cross-heating effect.

The temperature rise of any chips can be obtained by a linear superposition of all the heat sources in the same module using equation 5.1. To simplify the problem, a 4x4 impedance matrix is defined to describe the model [108], [191-192].

$$\begin{bmatrix} T_{jT1(t)} \\ T_{jT2}(t) \\ T_{jT3}(t) \\ T_{jT4}(t) \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} * \begin{bmatrix} P_{lossesT1} \\ P_{lossesT2} \\ P_{lossesT3} \\ P_{lossesT4} \end{bmatrix} + \begin{bmatrix} T_{ref} \\ T_{ref} \\ T_{ref} \\ T_{ref} \end{bmatrix} \quad (6.1)$$

The intended multichip power module can be modelled based on the following expression.

The losses in switches can be expressed as $P_{lossesT1}$,$P_{lossesT2}$, $P_{lossesT3}$ and $P_{lossesT4}$ respectively.

Now the key challenge is to derive the transient thermal response. To derive the transient thermal response, FEA model is created using the component's geometric dimension detailed in Table 49. Power losses of 13.7W for both switch T2 and T4 respectively are considered in this analysis. Also, power losses of 6.4 W adapted from [197] for both switch T1 and T3 respectively are applied in this analysis. These losses are applied at the top surface of each switch in the FEA thermal model. The simulation time is set to be 100 seconds so that the junction temperature reaches the steady state. Convective boundary condition is applied by using heat transfer coefficient of 52 $Wm^{-2}K^{-1}$ and the temperature of cooling air is set at 20°C.

FEA simulations are conducted four times. When switch T2 is powered, then rest switches T1, T3 and T4 are kept inactive. Figure 6.5 describes the self-heating of T2 and mutual-heating of other chips T1, T3, and T4. The temperature response due to power dissipation in T1 is referred to as self-heating effect and temperature responses at T2, T3 and T4 are known as mutual-heating effect. Similar approach is applied to obtain the temperature responses when T1, T3 and T4 are powered. Figure 6.6, Figure 6.7 and Figure 6.8 describes the self-heating of T1, T3 and T4 respectively and mutual-heating of other chips.

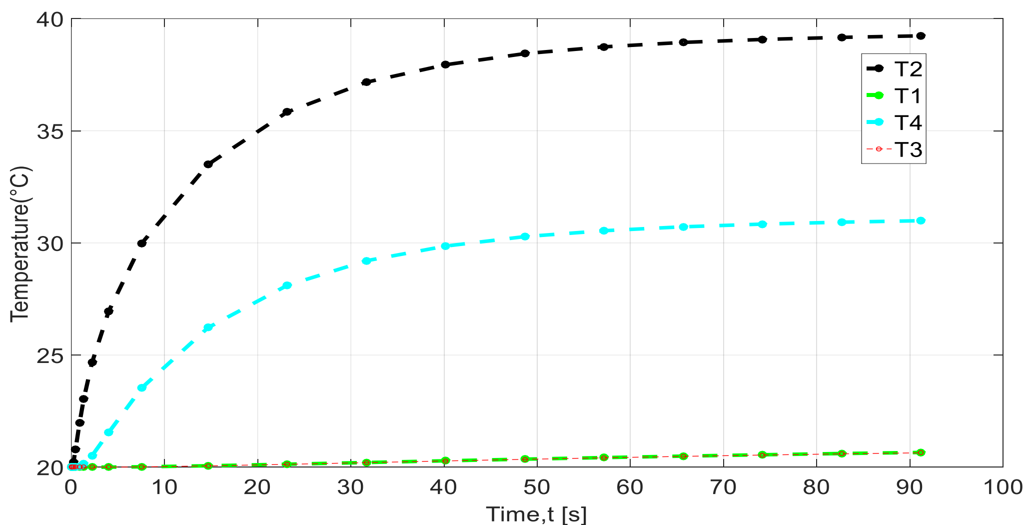


Figure 6.5 Switch's temperature responses when heat source is switch T2.

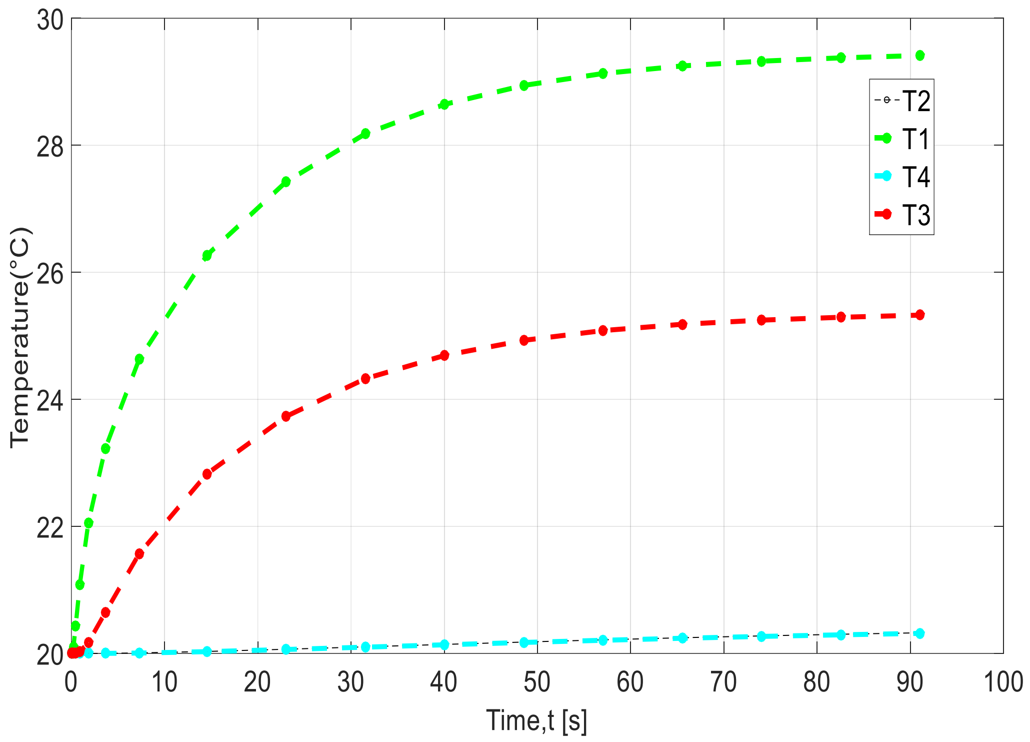


Figure 6.6 Switch’s temperature responses when heat source is switch T1.

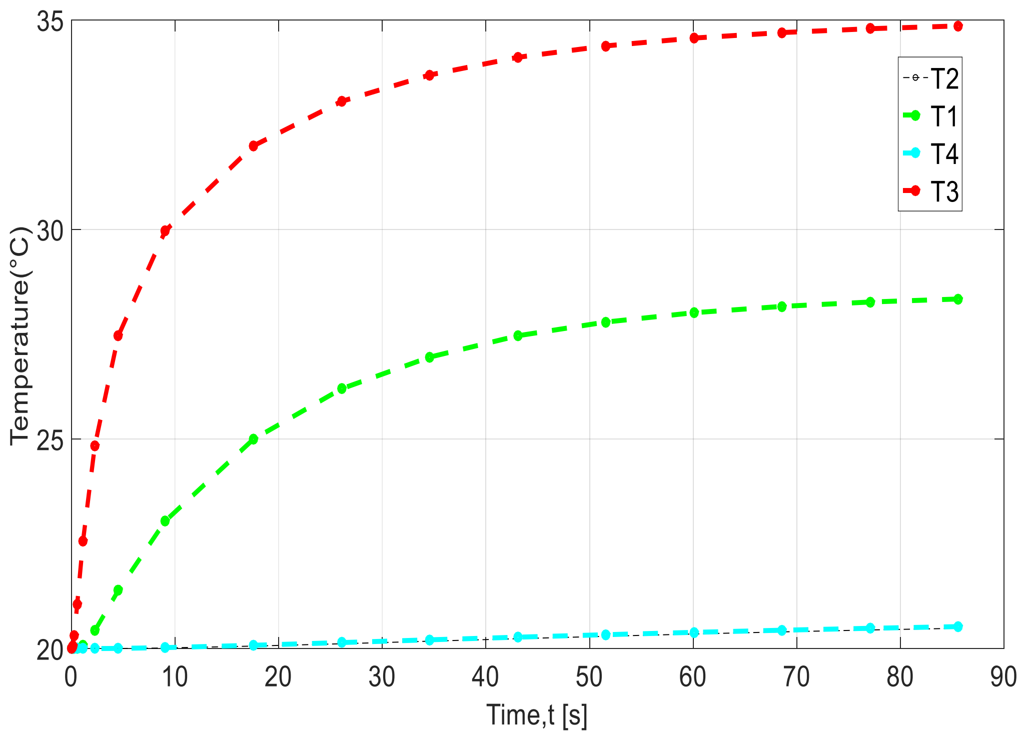


Figure 6.7 Switch’s temperature responses when heat source is switch T3.

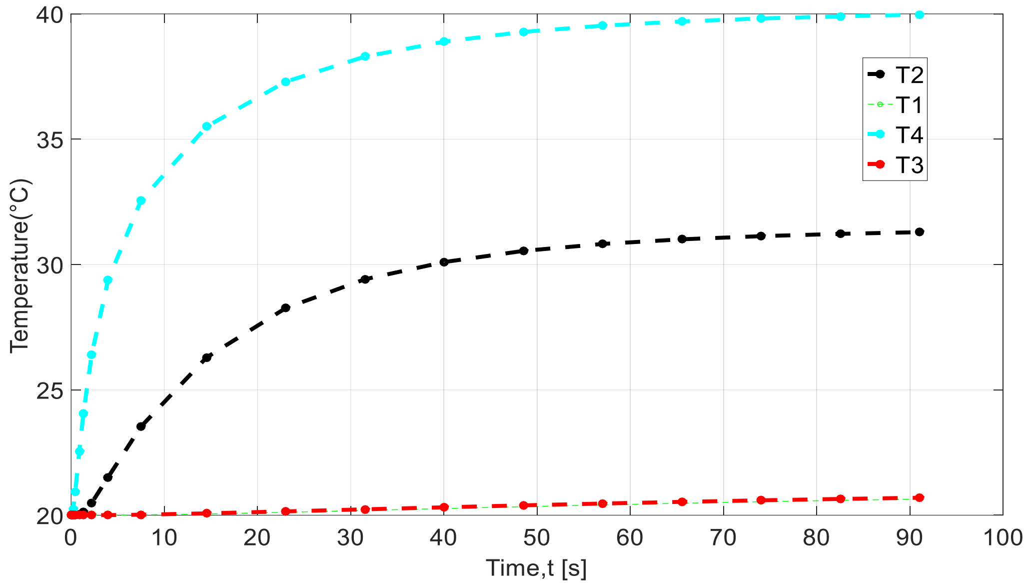


Figure 6.8 Switch's temperature responses when heat source is switch T4.

Using Equations (4.56-4.57), the self-heating and mutual-heating thermal impedance can be derived. The impedance curves for heat sources T2, T1, T3 and T4 are shown in Figure 6.9, Figure 6.10, Figure 6.11 and Figure 6.12 respectively. It can be seen from the all figures that the thermal time constant of the system increases from 0.04s to about 60s due to the large thermal inertia contributed by the fin extruded heatsink. It is also observed that the chip temperature only reaches the steady-state near at 100s. For the mutual-thermal impedances, it is clear that there is a delay in the temperature rise at the beginning because the chips only share the same T-clad board and heatsink and it takes time for the mutual heating effects to happen to unheated chips.

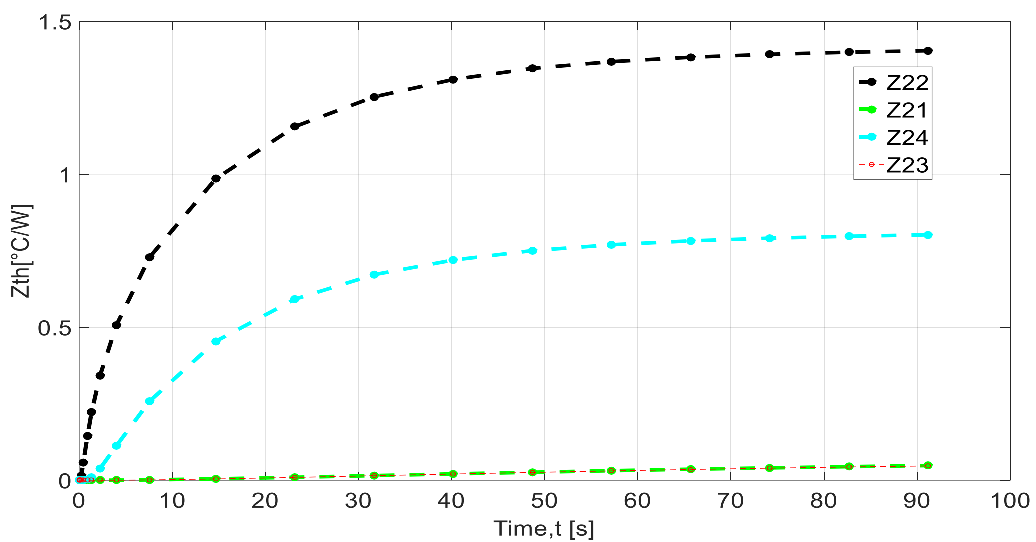


Figure 6.9 Self-heating and mutual-heating thermal impedance when heat source is switch T2.

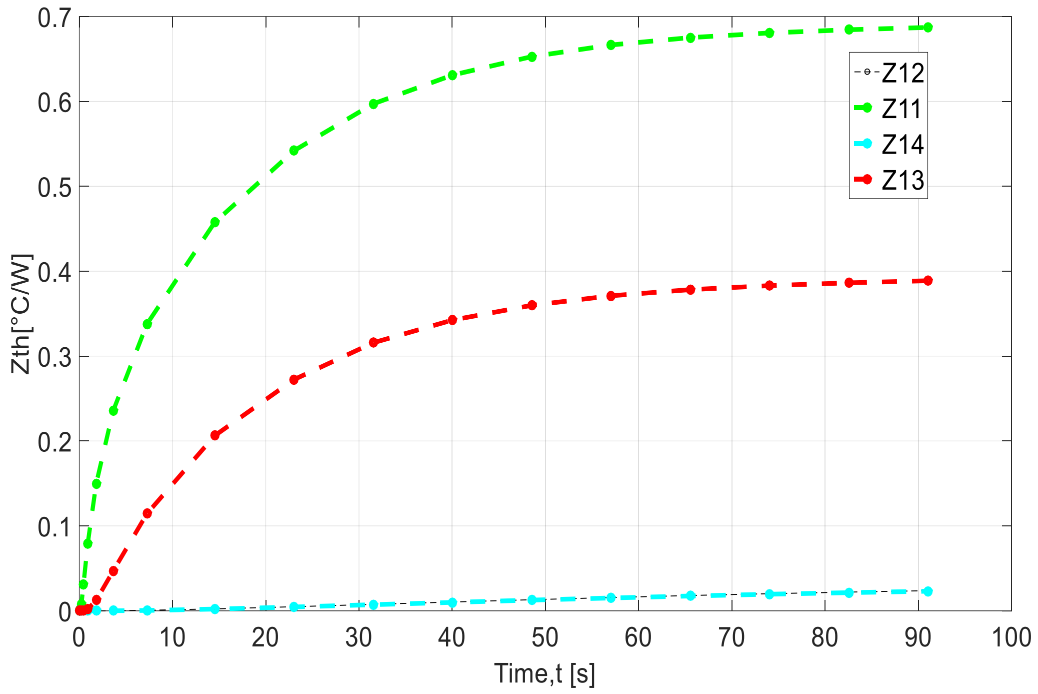


Figure 6.10 Self-heating and mutual-heating thermal impedance when heat source is switch T1.

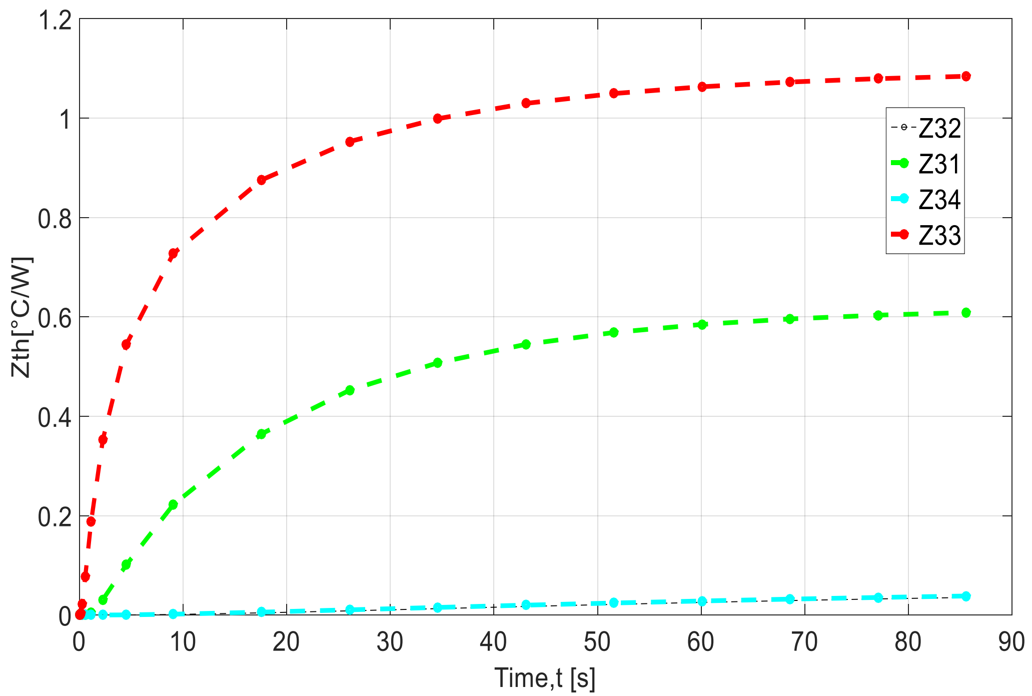


Figure 6.11 Self-heating and mutual-heating thermal impedance when heat source is switch T3.

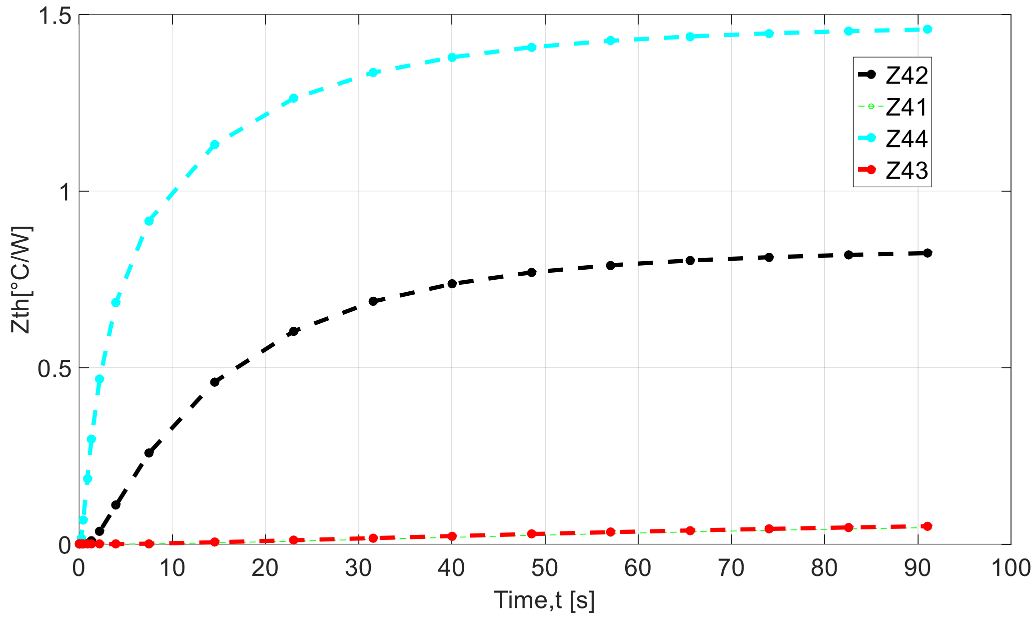


Figure 6.12 Self-heating and mutual-heating thermal impedance when heat source is switch T4.

As had been mentioned in section 4.7.5 of Chapter 4, these thermal impedance curves can be fitted into foster networks by the least square method. A third order foster network can be used to describe the self-heating thermal impedance of each thermal branch and it is enough to fit the mutual-heating thermal impedance. To demonstrate interaction analysis, only the switch T2 is considered, and temperature of switch T2 is predicted due to all heat sources active in the converter. The schematic diagrams of these foster networks are shown in Figure 6.13 and the corresponding parameters are listed in Table 49. The above described approach can be applied to estimate the temperature in switches such as T1, T3 and T4 respectively.

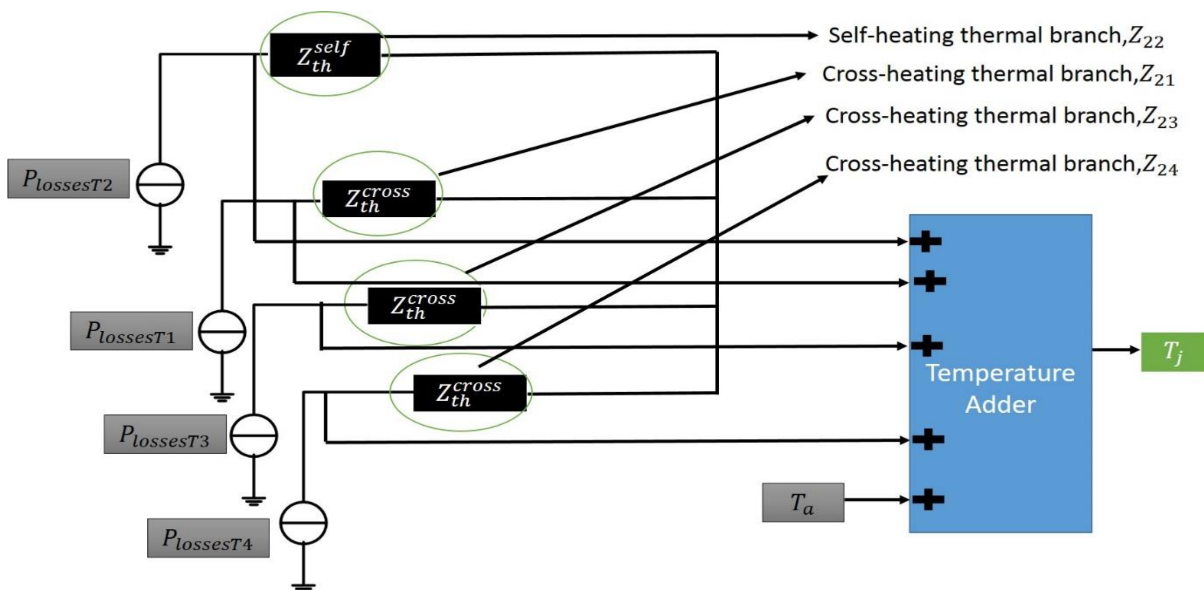


Figure 6.13 Self-heating and mutual-heating thermal impedance foster network.

Table 49 RC parameters of Foster equivalent network for T2-switch

Impedance Elements	Term number	1	2	3
Z_{21}	$R_{thi}, °C/W$	0.0215	5.4215e-19	.2497
	$C_{thi}, J/°C$	1.2179e3	20.1872	105.0409
Z_{22}	$R_{thi}, °C/W$	0.4481	0.1604	1.3231
	$C_{thi}, J/°C$	32.506	1.78e-7	.03726
Z_{23}	$R_{thi}, °C/W$	2.2419e-21	0.1666	3.7682e-22
	$C_{thi}, J/°C$	2.269e-5	1.6460e3	2.5895e-4
Z_{24}	$R_{thi}, °C/W$	8.0428e-20	6.9155e-19	0.1131
	$C_{thi}, J/°C$	4.47e-5	7.9425e-4	1.2857e3

6.1.4 Model Implementation

To demonstrate the electro-thermal interaction, the loss model is needed to be developed. Conduction losses can be estimated from circuit simulator. Multiplication of the current with corresponding voltage across the switch gives conduction losses.

The switching losses are estimated by fitting this equation into the circuit mathematical tools.

The equation of switching loss calculation is adapted from the thesis [197]. Figure 6.14 describes the loss modelling of the switch.

MOSFET conduction loss, $P_c = {I_{trms}}^2 * R_{ds}$ .... (6.2)

MOSFET switching loss, $P_{sw} = V_0 * \frac{I_0}{2} * f_{sw} * (\frac{Q_{th} - p + Q_{plt}}{i_g})$ .... (6.3)

Where gate current, $i_g = \frac{V_{gs} - V_{plt}}{Z_{drv} + R_g}$ .... (6.4)

Reverse recovery losses, $P_{rr} = f_{sw} * V_0 * I_0 * t_{rr} + f_{sw} * V_0 * Q_{rr}$ .... (6.5)

Total power Losses in MOSFET, $P_{tot} = P_c + P_{sw} + P_{rr}$ .... (6.6)

Where, I_{trms} is RMS MOSFET current, R_{ds} is MOSFET Drain to source resistance, i_g is MOSFET gate current, Q_{plt} is MOSFET gate to drain Miller plateau charge, $Q_{th} - p$ is MOSFET threshold to plateau gate charge, V_{gs} is Gate to source voltage for MOSFET, V_{plt} is MOSFET plateau voltage, Z_{drv} is Gate drive impedance, R_g is MOSFET internal gate resistance, t_{rr} is MOSFET reverse recovery time, Q_{rr} is MOSFET reverse recovery charge, P_{rr} is Loss in MOSFET due to diode reverse recovery, P_c is MOSFET conduction loss and P_{sw} is MOSFET switching loss.

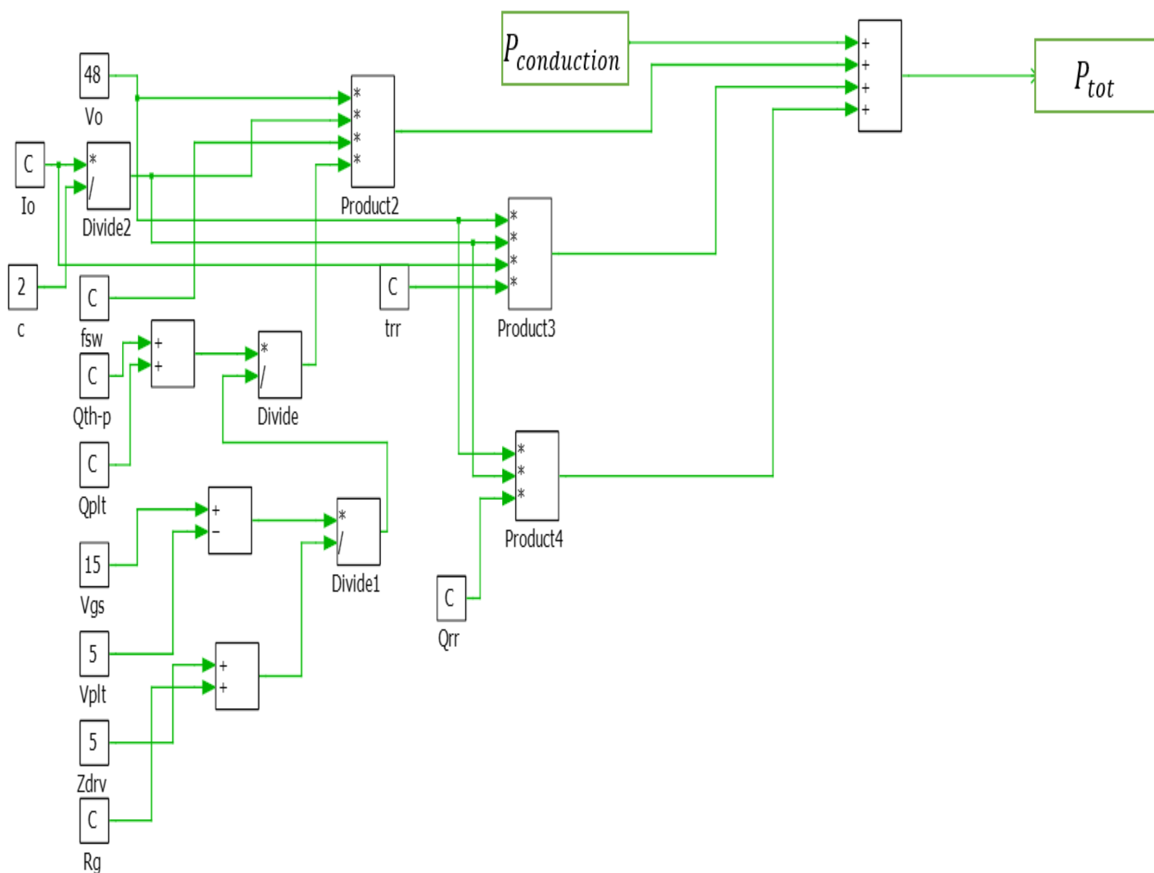


Figure 6.14 Loss modelling of switch, T2 in PLECS.

After deriving the loss model, the electrical model of the converter is coupled to the thermal network of each component and thus the temperature response of each source is accounted for and the summed junction temperature is provided by the adder. Figure 6.15 describes the coupled electro-thermal model for prediction of temperature at switch, T2.

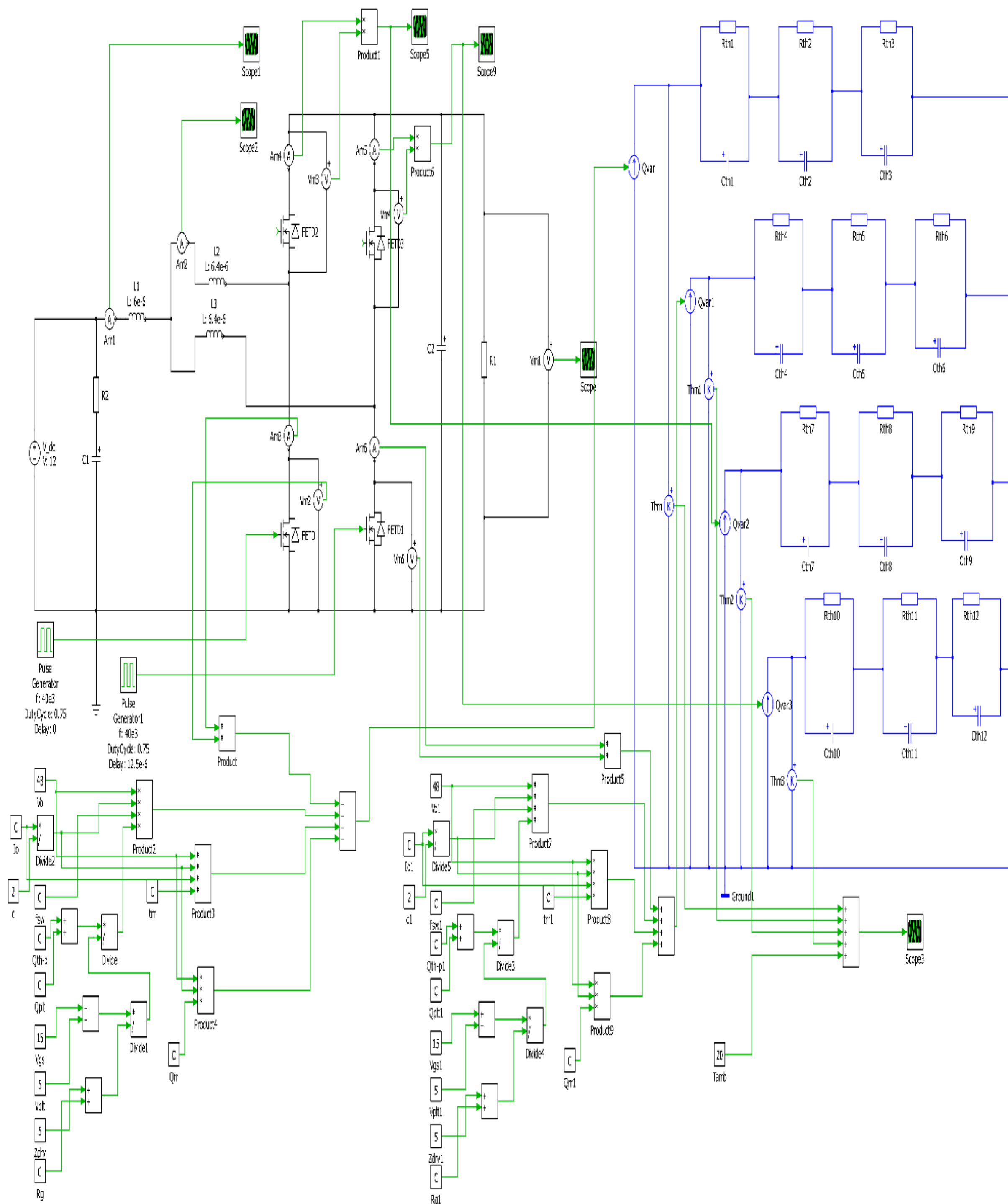


Figure 6.15 Coupled circuit model for prediction of temperature at switch, T2.

6.1.5 Circuit Approach

To demonstrate the effect of thermal coupling on the junction temperature prediction, two simulations have been performed. In the first simulation, all the switches are considered to be active. Electrical model of each switch is coupled to corresponding thermal network. In

the second simulation, only one heating source is considered to be active, while other switches are kept inactive. The temperature to be determined at the junction of the switch, T2 is estimated by solving the self-heating thermal network of itself and the cross-heating thermal network contributed by other switches. The coupled model in this analysis includes lateral thermal coupling and the derived thermal network is accounted for both self-heating and cross-heating effect. Again, the temperature predicted by non-coupled model does not include the thermal coupling of other switches. Temperature is recorded at the top point on the upper heatsink in both cases. Temperature predicted by both coupled (denoted by red) and non-coupled model (denoted by magenta) for the switch, T2 is shown in Figure 6.16. The non-coupled model differs by 6°C compared to the results of the coupled model. The difference can be explained by the contribution of thermal coupling due to the proximity of other switches to the switch, T2 and also lateral thermal coupling between downward layers of the considered structure of the components in the converter.

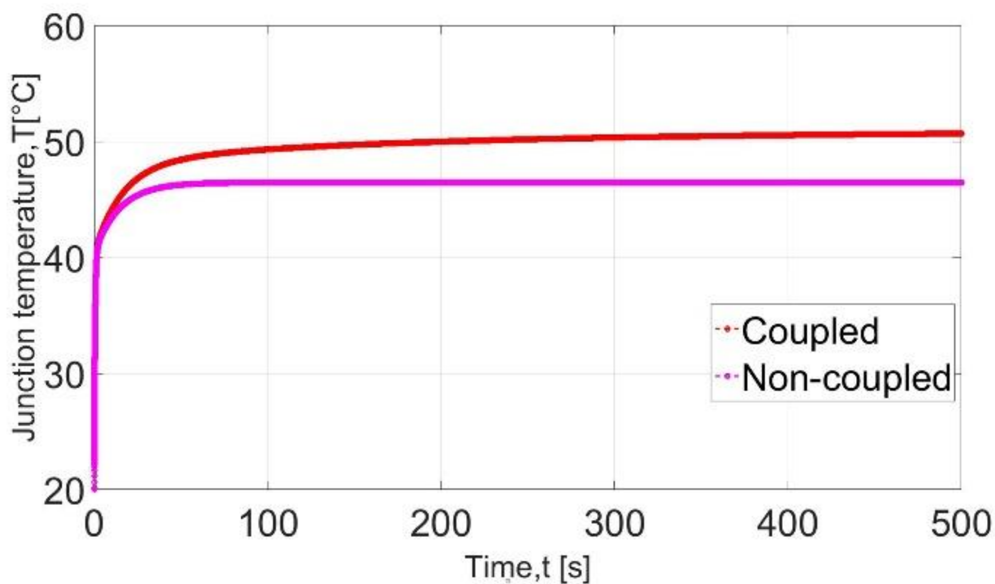


Figure 6.16 Predicted junction temperature profile of switch, T2 by coupled and non-coupled model.

6.2 Modelling Accuracy Analysis

To evaluate the modelling accuracy by the proposed method, the results of coupled circuit method is compared to the results obtained by FEA and experimental results obtained by IR thermography measurement [197]. The comparison of the temperature results predicted by the three methods is listed in Table 50. FEA model takes into account all those chips which

are considered to be active. The temperature distribution is shown in Figure 6.17. IR thermography temperature measurement is shown in Figure 6.18. It can be clearly seen that the temperature profiles agree well although a slight variation of 4.5°C is observed. The proposed circuit method differs by 1.75% and 8.3% compared to FEA method and experimental method, respectively. The FEA method differs by 6.69% compared to the experimental method. Overall, the results suggest that in general, temperature estimation error of the proposed method is less than 10% of that of the equivalent thermal circuit model. It can be clearly seen that the temperature profiles obtained by the proposed method are consistent with the estimated thermal profiles shown in Figure 6.16. The discrepancy can be explained by the fact that the can to drain layer in the FET structure is ignored. It might have an impact on temperature distribution. Also, the FET switch, T2 is surrounded by the tiny capacitors and all the losses of those capacitors can escalate the temperature by interactions. Due to ignoring all the losses of capacitor as heat sources in the thermal model inconsistencies occur with the estimated thermal profiles.

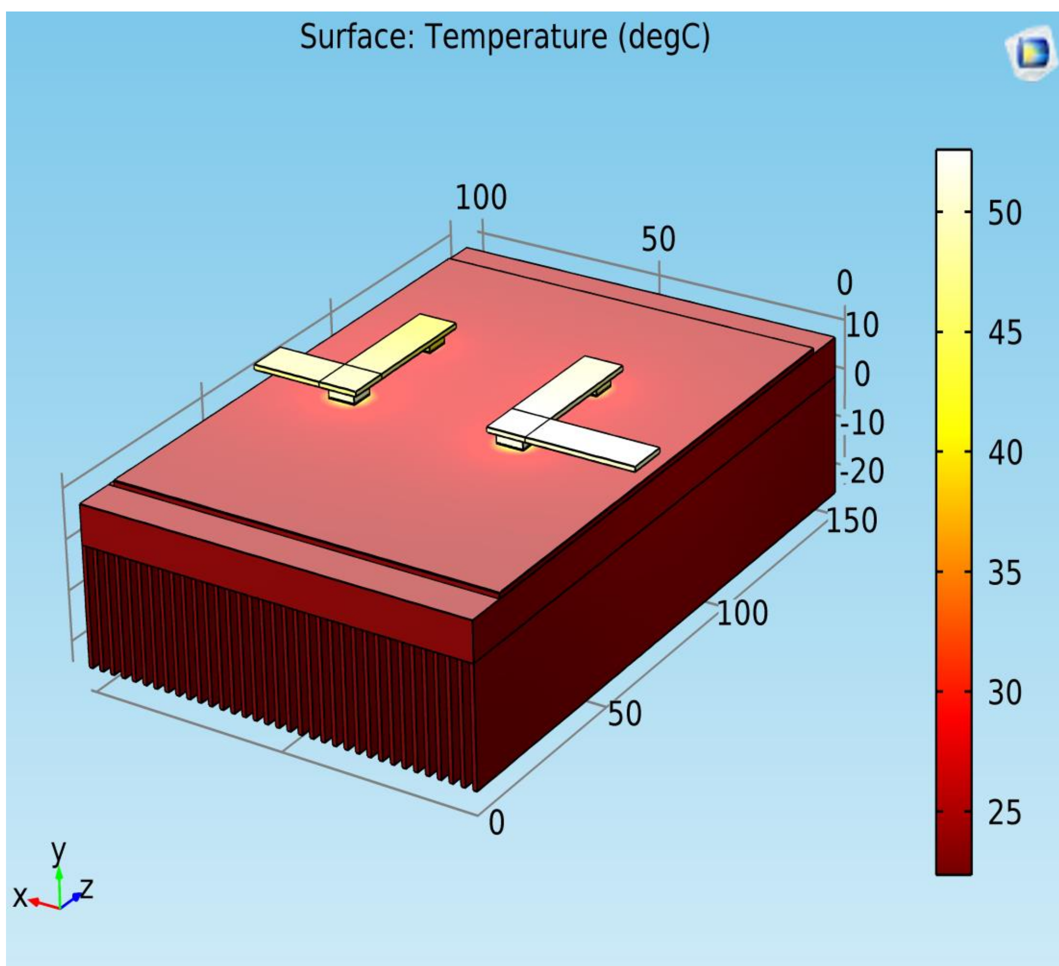
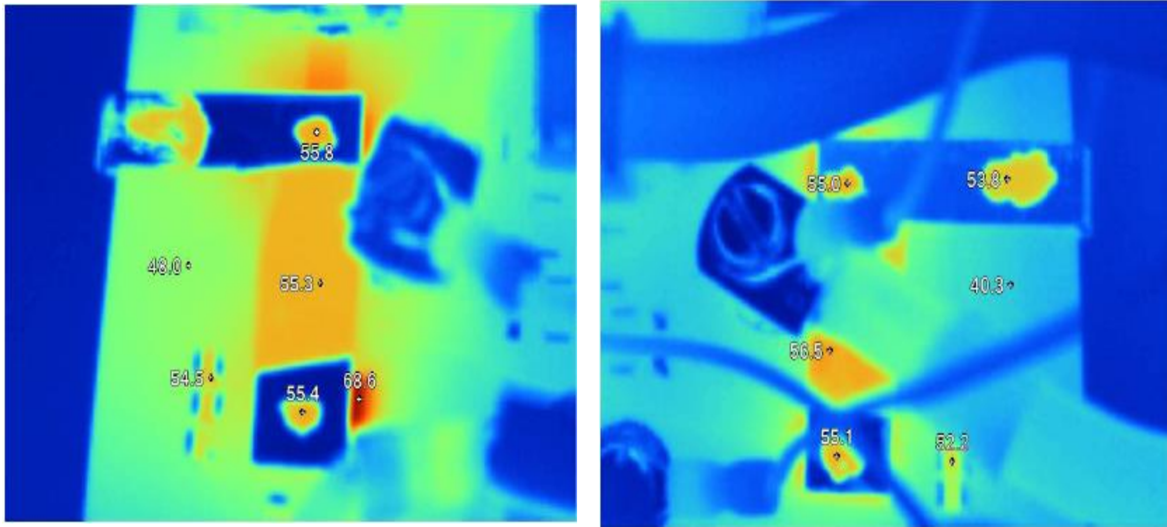


Figure 6.17 FEA modelling of IPT based dual interleaved bidirectional boost converter.



(a) (b)

Figure 6.18 Temperature of different components of the circuit (a) MOSFETs in the first phase leg and (b) MOSFETs in the second phase leg [197].

Table 50 Comparisons of temperature predicted by circuit, FEA and experimental method

Circuit, Temperature, °C	FEA Model	Thesis, Temperature, °C
50.42	51.32	55(Experimental) [197]

6.3 Modelling Magnetic Components

Modelling magnetic component is an important task as it affects the converter performance electro-thermally. With the framework described in the section 4.6.1(c) the losses can be calculated for input inductor and interphase transformer in an interleaved boost converter. The losses calculated by the framework agree well with the losses reported in this thesis. These losses are given in Table 51. These losses are then used in FEA thermal model of the magnetic component. FEA thermal model is built considering the DC inductor and IPT transformer. Winding and core losses are applied volumetrically in the winding and core section of both inductor and IPT transformer. The anisotropic thermal conductivity is applied in the model and the properties are listed in Table 52. Figure 6.19 shows the total temperature distribution. Anisotropic heat transfer is observed both in DC inductor and in interphase transformer. The temperature estimated by FEA thermal model is compared with the

measured temperature provided in this thesis and results are listed in Table 53. The results suggest that FEA predicted temperature for DC inductor agrees well with the experimental measurement whereas in the IPT transformer FEA varies slightly with the experimental results. This may happen due to simplified anisotropic assumption for foil winding. The temperature prediction of DC inductor is higher compared to the IPT transformer temperature. High losses in DC inductor raise the temperature. The temperature is high around the gap area due to the gap losses contributed by fringing fluxes. This temperature hotspot can be minimised by embedding DC inductor within potted heatsink. Figure 6.20 shows the temperature distribution when the magnetic component is kept inside the potted heatsink. This results in core temperature rise to 42.32°C and winding temperature rise to 41.8°C. The use of potted heatsink reduces the winding temperature and core temperature by 22°C and 45.08°C respectively.

Table 51 Predicted losses of the magnetic components

Components	Input Inductor			Interphase transformer	
Losses	Winding Losses	Core Losses	Gap Losses	Winding Losses	Core Losses
	5.94W	5.1W	2.3W	6.25W	2.6W

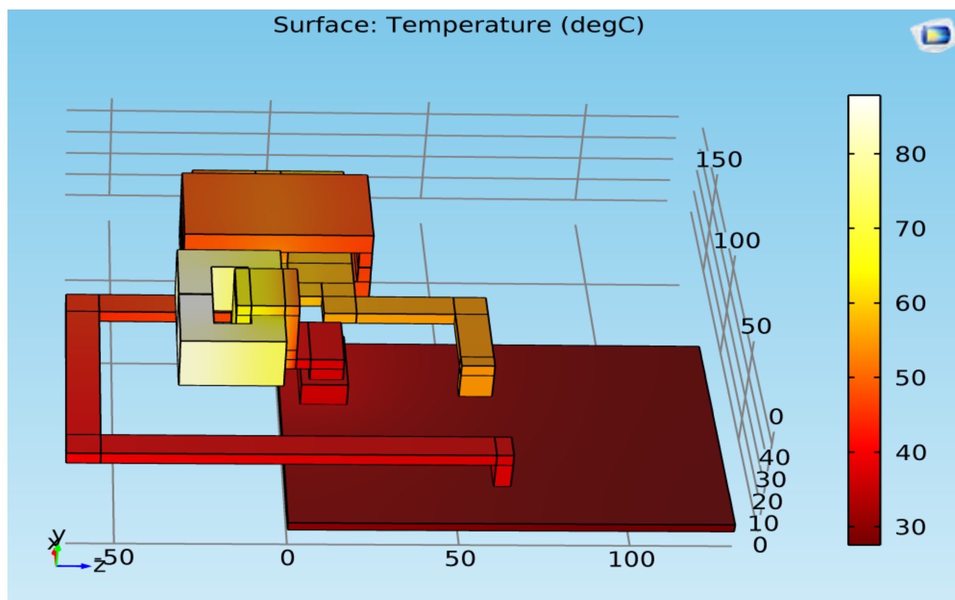


Figure 6.19 Temperature distribution of magnetic components in IPT based dual interleaved bidirectional boost converter.

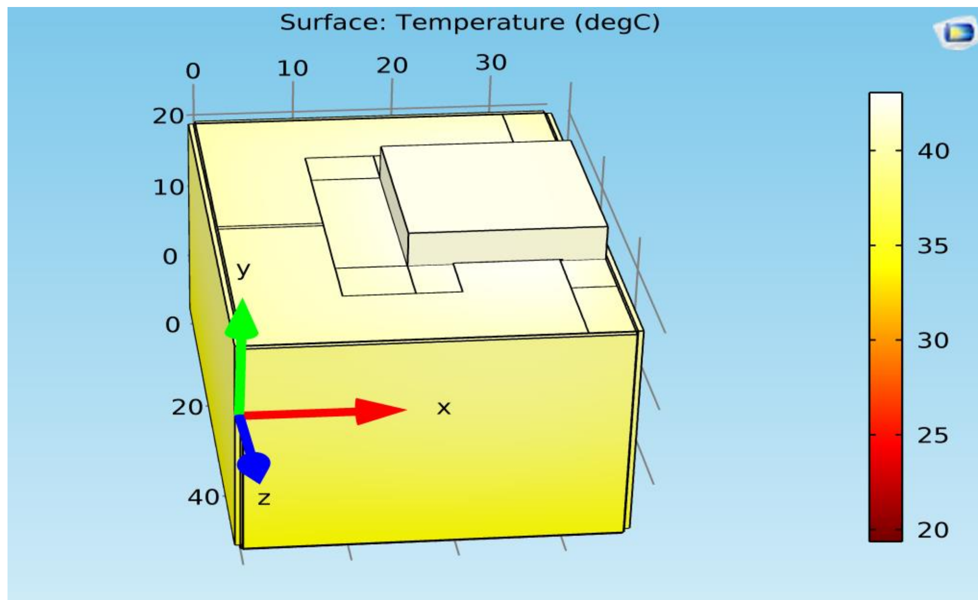


Figure 6.20 Improved thermal model of DC inductor with potted heatsink.

Table 52 Anisotropic thermal conductivity used in the model

Components	Thermal conductivity, $k, (\frac{W}{m*K})$			
	$k_{winding,xy}$	$k_{winding,z}$	$k_{core,xy}$	$k_{core,z}$
Inductor	363	4.86	7.65	9
IPT	323	2.51	4.18	4.18

Table 53 Comparisons of predicted temperature of the magnetic components

Components	DC Inductor temperature		Interphase Transformer	
Modelling Method	Winding Temperature $T_w, °C$	Core temperature $T_c, °C$	Winding Temperature $T_w, °C$	Core Temperature $T_c, °C$
Experimental, Thesis [197]	64.3	88.4	67.2	56.2
FEA	63.8	87.4	58.3	51.4

6.4 Performance Evaluation of Integrated Electric-thermal Modelling

Power electronics systems with high-power density are expected to operate at high voltages and harsh environments. Due to high power density, power electronic systems undergo thermal challenges due to complex loading in very harsh environments [147]. Moreover, the reliability of the power module is highly dependent on the device junction temperature, so accurate power loss prediction and subsequent thermal simulations are highly important for system designers [199]. Nonetheless, the electrical properties and reliability of the components of power electronics system are greatly influenced by the temperature distribution of the system level. Therefore, to evaluate the system level performance, it is highly important to have accurate electro-thermal models to predict its electro-thermal behaviour [104]. Power electronics product manufacturers continuously seek to improve their lifetime and reliability of power semiconductor devices under both thermal and power cycles. Also, it has been reported that 60% of system failures are temperature induced and the failure rate doubles in the operating environment for every 10°C temperature rise [200]. Moreover, current focus in power electronic systems design has shifted towards achieving high power density and high packaging density. Additionally, reduction of passive structure and integration of active and passive components at system-level are targeted. All these contribute to the severe size reduction of the converter at system-level. As a result dissipated power by the converter's components becomes the source of heat generation. Within the fixed volume of converter, thermal management becomes more and more critical. If left untreated, it may lead to the premature failure and thus affect the reliability of the components. Therefore, running a concurrent electro-thermal simulation at the early stages of design processes may fulfil the design requirements set by manufacturers of high-power system such as electric vehicles, aerospace, locomotives, ships and railway traction etc. [97]. Now, the evaluation of integrated electric and thermal analysis and significance of the integrated analysis will be discussed.

6.5 Analysis of Speed of the Integrated Modelling

The integrated electric-thermal analysis provides the confidence in the design and development of power electronics product. The design of the converter without concurrent electro-thermal analysis results in poor performance in the context of thermal management. One could argue that the time which is required to generate the thermal network and implementation of the same in the circuit simulator is longer that FEA analysis. It should be pointed out that for the presented thermal model, FEA simulations are performed for twice

with the dissipated power and the model can be exploited to capture long-term load profile variations without running further any FEA simulations. Prediction of temperature at the critical locations of multi-layer structured IGBT modules and component interaction analysis in the compact converter are the major contributions of the presented thermal model, which is generally a difficult one to predict accurately by the manufacturer provided datasheet or experimental measurement due to problems to integrate thermo-couples or thermal sensors to the inaccessible nodes. Therefore, the merits of fast simulation is significant when a typical converter experiences long mission profiles and fast reliability analysis is required based on temperature cycles at the junction and at the critical locations in the module. To test the speed of the proposed approach, pulsed load profiles are injected into thermal networks and simulations are run in a circuit simulator and using same load profiles FEA simulations are performed. The analysis suggests that the thermal model in PLECS is faster compared to FEA analysis in COMSOL. PLECS takes 10s to solve a 1 Hz pulsed power of duty ratio of 0.5 whereas COMSOL takes 40 minutes as shown in Figure 5.36. Table 54 summarizes the comparison of computational time.

Table 54 Comparisons of calculation time

Computer Specifications	Modelling Method	Computational time
Workstation: Intel, Core i5-2500,3.30GHz,RAM 8GB	Thermal Model in PLECS	10 seconds
	FEA Analysis in COMSOL	40 minutes

6.6 Significance of integrated analysis

The integrated approach based on electric-thermal analysis provides the accurate temperature prediction and this may help achieve an optimal design of the placement of the component making the best use of the space to transfer heat. The design of power electronics systems is an iterative process in which component selection, component dimension, thermal characteristics of the heat sink, cooling characteristics etc. are regarded as decision based variables. Because of its complexity, designing power electronics systems using experimental prototypes is extremely tiresome and expensive. Engineers use a method in building power

electronics systems which is simplistic and based on experience and costly trial and error approach. In addition, thermal performance optimisation is not considered as part of the design processes. Designs that are based on computer simulation which uses the integrated analysis can speed up the design cycle, reduce design costs and improve product reliability.

6.7 Conclusions

In this chapter, integrated electro-thermal modelling has been performed for the component interaction between four chips in an IPT based boost converter. The converter structure has been used in FEA analysis. Losses are derived analytically by using the framework. The derived losses are then used as heat sources in the FEA thermal model. Applying appropriate boundary conditions, the FEA analysis solves the temperature distribution of the converter components. The method has been verified to estimate junction temperatures in switches accurately and with very fast speed comparing to commercial FEA based thermal simulations. Using the framework, magnetic component loss profiles have also been derived and later used in FEA thermal model. The framework predicts the temperature rise in the magnetic components and provides better accuracy compared to experimental results. Also, the advantages of the integrated electric-thermal analysis are discussed. It is found that the integrated analysis can help in characterizing thermal behaviours in compact power electronic converters and can predict the temperature accurately maintaining high speed simulation. Thus, this may help achieve an optimal designing of the placement of the component making the best use of the space to transfer heat in converter system.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

In this research work, an integrated electro-thermal modelling framework which combines a circuit simulator and a FEA simulator suitable for systems level integrated power electronics design has been developed. Within this framework, electrical circuit analysis is carried out on a power electronics system and the losses in the power electronic components are predicted. The losses are then used in FEA thermal analysis and the results are used to improve compact thermal models that can be solved using a spice type circuit simulator. This methodology allows the inclusion of the thermal coupling effects among components as well as the thermal spreading effect in layered component structures. Furthermore, the methodology can be used to study the effects of non-linear phenomena such as temperature dependent material properties, geometry effects, non-linear boundary conditions and the inclusion of thermal grease layer etc. The output of the framework is a compact thermal network model which can be used to predict the thermal performance of the power electronics systems under a range of loading and boundary conditions. Compared to the FEA method, this compact model is computationally more efficient and it is very suitable for the optimization of the design. The process of generating the final compact thermal network model from FEA thermal analysis results has been automated. The electrical and thermal domain problem has been converted into single-domain electrical model which is solved using a circuit simulator. This single-domain circuit based analysis gives the benefit of reducing computational cost by eliminating the complexity of solving multi-domain problems. Thus, significant improvement on the simulation speed can be exploited in solving long-term in-service mission profile of power electronic converters. In addition, the accuracy and efficiency have also been improved significantly by using the framework. It is concluded that the proposed framework is an effective tool for the accurate estimation of temperature of power electronic components at system level. It can be also used for dealing with the optimization problems of packaging design and for carrying out reliability analysis of power electronics system. A summary of the research outcomes of this work is detailed in the following.

1. New RC compact thermal Model

FEA is a useful tool to predict temperatures of the power modules accurately for long-load cycles, but this is a time-consuming approach to solve long-term electric loading problems such as the operation of wind turbine over a time scale of years. For this type of problem, an RC network based compact model is a better alternative. In the modelling framework that has

been proposed, thermal coupling effects have been taken into account for accurate results. Besides, a generic thermal network model has been added to account for the loading and boundary conditions. It has been observed that the changes in these conditions affect the accuracy of the thermal network significantly. The thermal network performance is satisfactory for a range of load profiles and boundary conditions. The results are consistent with that of FEA simulation and it is much faster compared to FEA analysis. This shows that this compact thermal model can be used as a fast and accurate tool in different converter topologies for estimating the temperatures at critical locations in the system level components.

2. FEA thermal modelling of the converters

FEA software has been used to estimate temperatures at the critical locations of the components in the converter where measurements are challenging due to the difficulty in embedding thermo-couples and the errors that are caused by the oscillations of the thermal sensors in a test system. The predicted temperatures have been used to extract compact thermal model parameters.

3. Design Tools

The integrated design electric-thermal analysis framework consists of a few software packages. These packages are interlinked using C# and data files so that electric-thermal analysis can be concurrently performed seamlessly and can easily be used to design power electronics system. This framework allows electronics packaging designers to model easily electrical-thermal problems of converters. It only requires basic converter design parameters for estimating power losses using the PLCES package. The predicted losses are then used in FEA thermal analysis from which thermal equivalent RC parameters can be obtained. These RC network parameters take into account both self-heating and cross-heating effects which is important in ensuring accurate temperature predictions.

In this work, three conventional converter topologies have been analysed by using the developed design framework. The first one is the electro-thermal model of the dc-dc boost converter, the second one is electro-thermal interaction of the inverter components and the last one is modelling the interleaved boost converter.

7.2 Recommended future work

The design framework could be improved in the following areas.

- Linking the framework to optimisation software in order to carry out design optimisation in situ.
- Integrating a reliability analysis toolbox in the software for component and system level lifetime prediction.
- Developing an online temperature monitoring application by integrating the electro-thermal model with power electronic converter in real applications as part of a health monitoring system.
- Integrating with a thermo-mechanical modelling software to analyse the power module mechanical behaviour under electric and thermal loading to predict mechanical failures
- Applying the methodology to Wide-Band-Gap device and investigate the issues of power module packaging for high temperature applications (e.g. aircraft or automotive) and help develop new packaging techniques for reliable operation performance.

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Appendix

Appendix A. Converter Design Formula

For Step-down (Buck) Converter

Input parameters for the calculation: Input voltage (V_{in}), output voltage (V_{out}), output power (P_0) , inductor value (L) and switching frequency (f_s) .

Converter design equations are adapted from [201].

Output Current:

$$I_o = \frac{P_o}{V_o} \quad \text{(A.1)}$$

Duty cycle in continuous conduction mode:

$$D = \frac{V_o}{V_{in}} \quad \text{(A.2)}$$

Output current ripple:

$$\Delta I_o = \frac{(1-D)V_o}{L f_s} \quad \text{(A.3)}$$

The parameters needed for the loss calculation can be determined according to previously calculated values as:

$$I_{con} = I_o - \frac{\Delta I_o}{2} \quad \text{(A.4)}$$

$$I_{coff} = I_o + \frac{\Delta I_o}{2} \quad \text{(A.5)}$$

$$I_{cav} = D I_o \quad \text{(A.6)}$$

$$I_{crms}{}^2 = D I_o{}^2 = (\sqrt{D}.I_o)^2 \quad \text{(A.7)}$$

$$I_{Dav} = (1-D).I_o \quad \text{(A.8)}$$

$$I_{Drms}{}^2 = (1-D).I_o{}^2 = (\sqrt{1-D}.I_0)^2 \quad \text{(A.9)}$$

For Step-up (Boost) Converter

Input parameters for the calculation:

Input voltage (V_{in}), output voltage (V_{out}), output power (P_0), inductor value (L) and switching frequency (f_s) .

Design equations are adapted from [201].

Input Current:

$$I_{in} = \frac{P_{in}}{V_{in}} \quad \text{(A.10)}$$

Duty cycle in continuous conduction mode:

$$D = 1 - \frac{V_{in}}{V_o} \quad \text{(A.11)}$$

Input current ripple:

$$\Delta I_{in} = \frac{D.V_{in}}{Lf_s} \quad \text{(A.12)}$$

The parameters needed for the loss calculation can be determined according to previously calculated values as:

$$I_{con} = I_{in} - \frac{\Delta in}{2} \quad \text{(A.13)}$$

$$I_{coff} = I_{in} + \frac{\Delta in}{2} \quad \text{(A.14)}$$

$$I_{cav} = DI_{in} \quad \text{(A.15)}$$

$${I_{crms}}^2 = D{I_{in}}^2 = (\sqrt{D}.I_{in})^2 \quad \text{(A.16)}$$

$$I_{Dav} = (1 - D).I_{in} \quad \text{(A.17)}$$

$${I_{Drms}}^2 = (1 - D) \quad \text{(A.18)}$$

$${I_{in}}^2 = (\sqrt{1 - D}.I_{in})^2 \quad \text{(A.19)}$$

Appendix B: Formulation of Heat Transfer PDE

Typically three different modes of heat propagation such as convection, radiation or conduction can take place in a system. In solid materials, such as power electronic components, conduction is considered as a dominant mode of heat transfer and other ways such as convection and radiation are assumed negligible. In a homogenous isotropic material, the conduction is assumed to be one-dimensional.

Formulation of heat transfer PDE:

To formulate the finite element method, we begin from the general heat Fourier law equation and discretization of the problem domain. The analysis and assumptions are discussed below:

$$Q(x) = -k\nabla T(x) \quad \text{(B.1)}$$

Formulation of heat transfer PDE:

A tiny cube of volume $dv = dxdydz$ is considered (see Figure B.1), being part of three dimensional body. Under the influence of a temperature distribution $T(x)$ inside the body, there occur heat fluxes Q_i and Q_{i+di} $(i = x, y, z)$ through the six corresponding surfaces of the surface [202]. Using Taylor approximation of first order,

$$Q_{i+di} = Q_i + \frac{\partial Q_i}{\partial k} di \; (i = x, y, z) \quad \text{(B.2)}$$

We obtain the following rate net heat transfer rates into the cube (units in Watt):

Along the x-axis

$$(Q_x - Q_{x+dx})dydz = -\left(\frac{\partial Q_x}{\partial x}\right) dxdydz = -\left(\frac{\partial Q_x}{\partial x}\right) dv \quad \text{(B.3)}$$

Along the y –axis

$$\left(Q_y - Q_{y+dy}\right)dxdz = -\left(\frac{\partial Q_y}{\partial y}\right) dydxdz = -\left(\frac{\partial Q_y}{\partial y}\right) dv \quad \text{(B.4)}$$

Along the z-axis

$$(Q_z - Q_{z+dz})dxdy = -\left(\frac{\partial Q_z}{\partial z}\right) dzdxdy = -\left(\frac{\partial Q_z}{\partial x}\right) dv \quad \text{(B.5)}$$

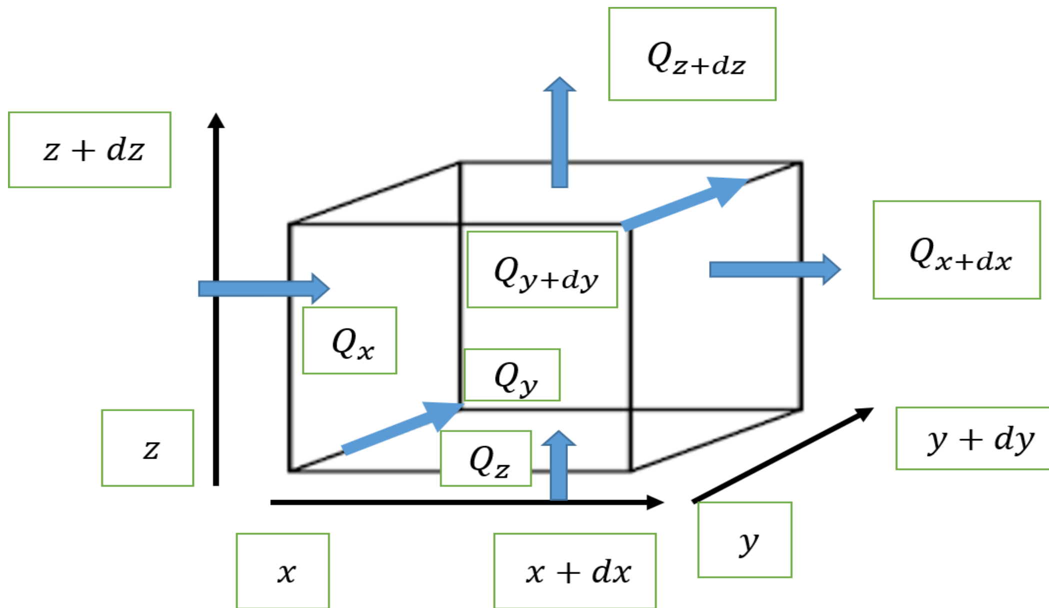

Figure B.1 Volume element $dV$and heat fluxes through its surfaces [202].

Adding up all three of them and substituting $-k\left(\frac{\partial T}{\partial i}\right)$ for Q_i (which is just the component form of equation (B.1)) yields the overall net heat entry into volume dv:

$$Q_{net} = \frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)dV + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)dV + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)dV = div(k\nabla T)dv \quad \text{(B.6)}$$

In the absence of heat sources and sinks respectively, must be equal to the storage rate of thermal energy

$$H_{st} = c_p dm\frac{\partial T}{\partial t} = \rho c_p\frac{\partial T}{\partial t}dv \quad \text{(B.7)}$$

Where

- c_p the specific heat capacity
- dm the mass of the volume dv,
- ρ the density of the material and
- $\frac{\partial T}{\partial t}$ The partial derivative of the temperature with respect to time.

This simple balance of and finally gives us Fourier's PDE

$$\rho c_p\frac{\partial T}{\partial t} = div(k\nabla T) \quad \text{(B.8)}$$

Which must be satisfied in every point $x = (x, y, z)$ for every moment t.

Boundary conditions:

The above derived PDE of heat conduction is solved with applying boundary conditions. Three types of the boundary conditions are usually applied [202].

These are as follows:

Dirichlet boundary condition (boundary condition of first type)

The temperature on the boundary of the body is represented by

$$T(x,t) = T_w(x,t) \qquad \text{(B.9)}$$

Where, T_w is a known function. In a lot of practical applications, T_w is a simply a constant.

Neumann boundary conditions (boundary condition of secondary type)

If the heat flux out of the body (perpendicular to the surface) is given, then Fourier's law helps us in determining the partial derivative of the temperature with respect to the outward normal vector$n$:

$$Q_w(\boldsymbol{x},t) = -k\frac{\partial T}{\partial n}(\boldsymbol{x},t) \approx \frac{\partial T}{\partial n}(\boldsymbol{x},t) = -\frac{Q_w(\boldsymbol{x},t)}{k} \qquad \text{(B.10)}$$

Observe that in the special case of perfect insulation($Q_w = 0$), the equation to the right becomes a homogenous Neumann boundary condition

$$\frac{\partial T}{\partial n}(\boldsymbol{x},t) = 0 \qquad \text{(B.11)}$$

Cauchy boundary condition (boundary condition of third type)

When the heat is entering in a body and this heat needs to be removed. Then convective boundary conditions are applied to model the thermal interaction between the body and a surrounding fluid temperature. To measure this, the boundary of the domain is considered as control volume in the Figure B.2 represented by a solid body. Since the thickness of the boundary is zero, no energy can be stored within [202]. This means that all the heat entering a surface increment from the interior (by conduction) has to leave outwards (by convection):

$$-k\frac{\partial T}{\partial n}(\boldsymbol{x},t) = h(T(\boldsymbol{x},t) - T_f) \qquad \text{(B.12)}$$

Sometimes, the heat transfer by radiation is taken into account as well. Engineers usually include it by simply introducing an additional transport coefficient h_{rad}:

$$-k\frac{\partial T}{\partial n}(\boldsymbol{x},t) = (h + h_{rad})(T(\boldsymbol{x},t) - T_f) \quad \text{(B.13)}$$

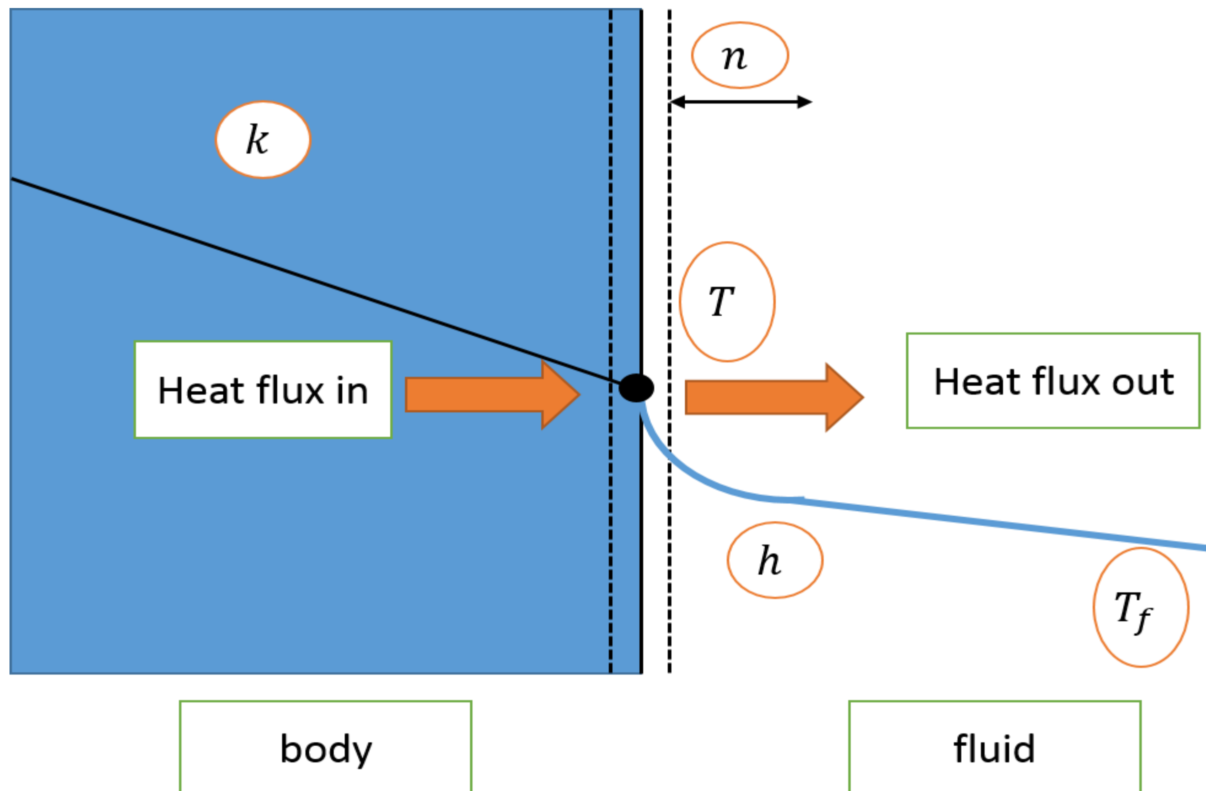

Figure B.2 Cauchy boundary condition with corresponding temperature profile.

Appendix C: RC Thermal Network Basics

Physical structure/geometry based lumped RC network

The physical structure based RC network is also known as the physical based lumped parameter networks (LPTN). The heat conduction equation can be modelled by this method as the transmission line equation.

IGBT power module is considered as a multilayer vertical structure containing several layers that are in stack by one another and in direct contact each other. Heat conduction in this

structure is assumed to be one-dimensional [203]. The thermal characteristics of silicon chip such as the conductivity) is also assumed dependent on temperature. The above two assumptions simplify heat transfer PDE equation (B.8) into:

$$k\frac{\partial^2 T}{\partial x^2} = \rho c\frac{\partial T}{\partial t} \quad \text{(C.1)}$$

Where x denotes the coordinate in the direction of heat propagation.

According to Kirchhoff's research, "Two different forms of energy behave identically when the basic differential equations which describe them have the same form and the initial and boundary conditions are identical". Therefore, the heat conduction process can be modelled by a transmission line equation [203], it can be simplified in the form of following equation representing

$$\frac{\partial^2 V}{\partial x^2} = CR\frac{\partial V}{\partial t} \quad \text{(C.2)}$$

Where, C is the capacitance per unit length and R is the resistance per unit length of the line.

So it is obvious that (C.1) and (C.2) have the same structure, and since/as transmission line can be modelled as RC network, the thermal conduction problem can be described/characterised as a similar RC network.

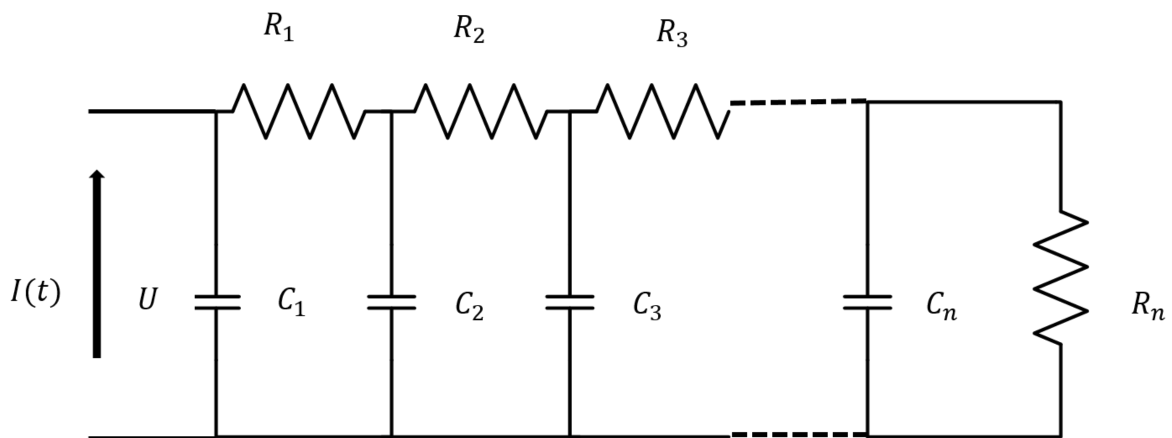

Figure C.1 Transmission line equivalent circuit diagram.

In order to derive the thermal RC network parameters value, we need to transfer equation in the following form [203]:

For modelling a power transistor such as IGBT, a transmission line equivalent circuit can be applied to solve the heat transfer problem in the form of conduction from the silicon chip to the heatsink. IGBT is considered a vertical power device, which means its inner structure can be divided/segmented to several layers as it is shown in Figure C.2 and for each layer, the thickness is much as smaller than other dimensions, so a one dimensional conduction process is always assumed in the physical based RC network method [114].

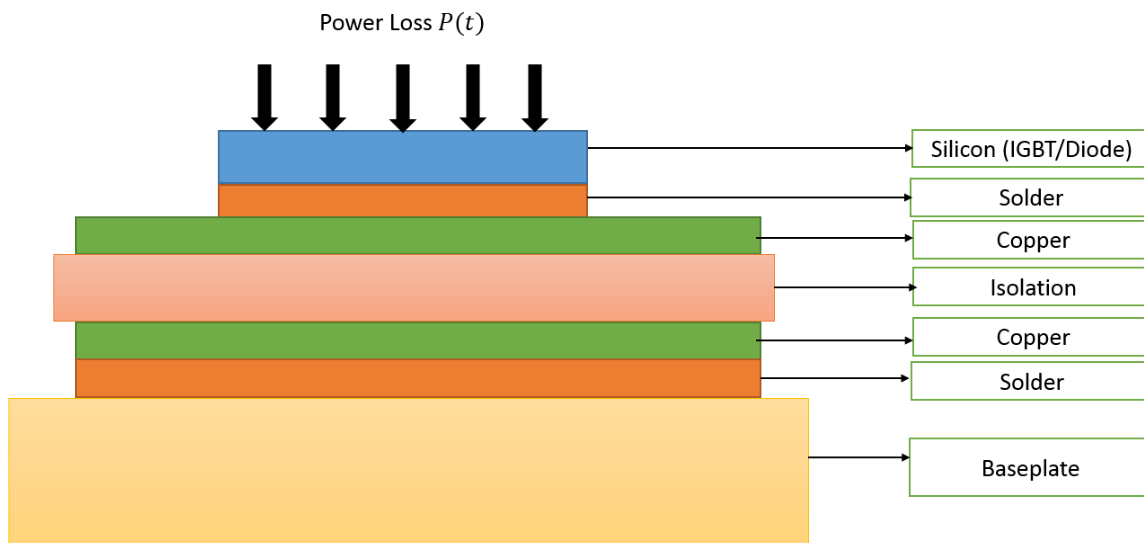

Figure C.2 Simplified physical structure of an IGBT module.

By employing the analogous physical variables of the thermal system to the transmission line equivalent circuit, the thermal RC network corresponding to the IGBT module shows in Figure C.2 can be derived as it is shown in Figure C.3 where each RC network represents the different layer of material in the IGBT module.

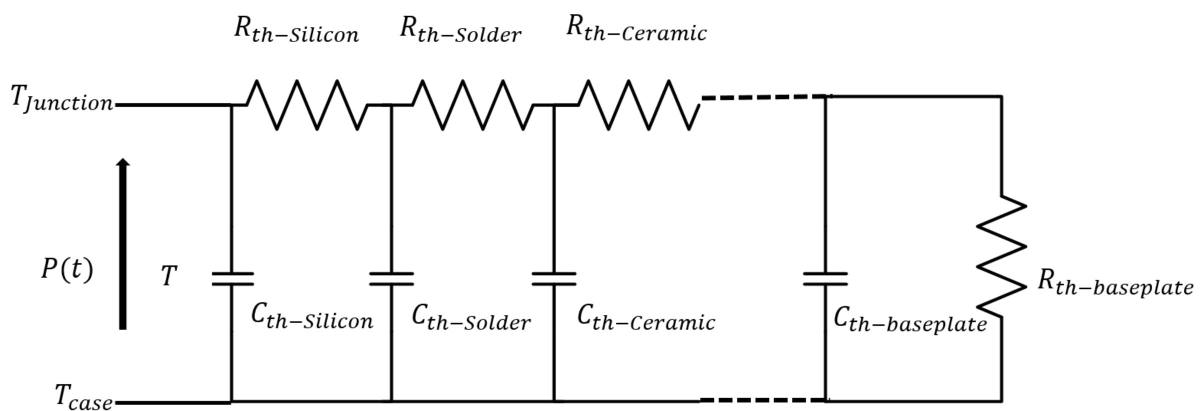

Figure C.3 Transmission line equivalent circuit diagram for thermal conduction.

As a quasi-1D heat flow is assumed in the system, the thermal resistance R_i and thermal capacitance C_i of each layer can be estimated by the following equations.

$$R_{th,i} = \frac{d_i}{\lambda_{th} A_{th,i}} \quad \text{(C.3)}$$

$$C_{th,i} = \rho c d_j A_j \quad \text{(C.4)}$$

Where A_i and d_i represent the cross sectional area and thickness of layer i as it shows in Figure C.4.

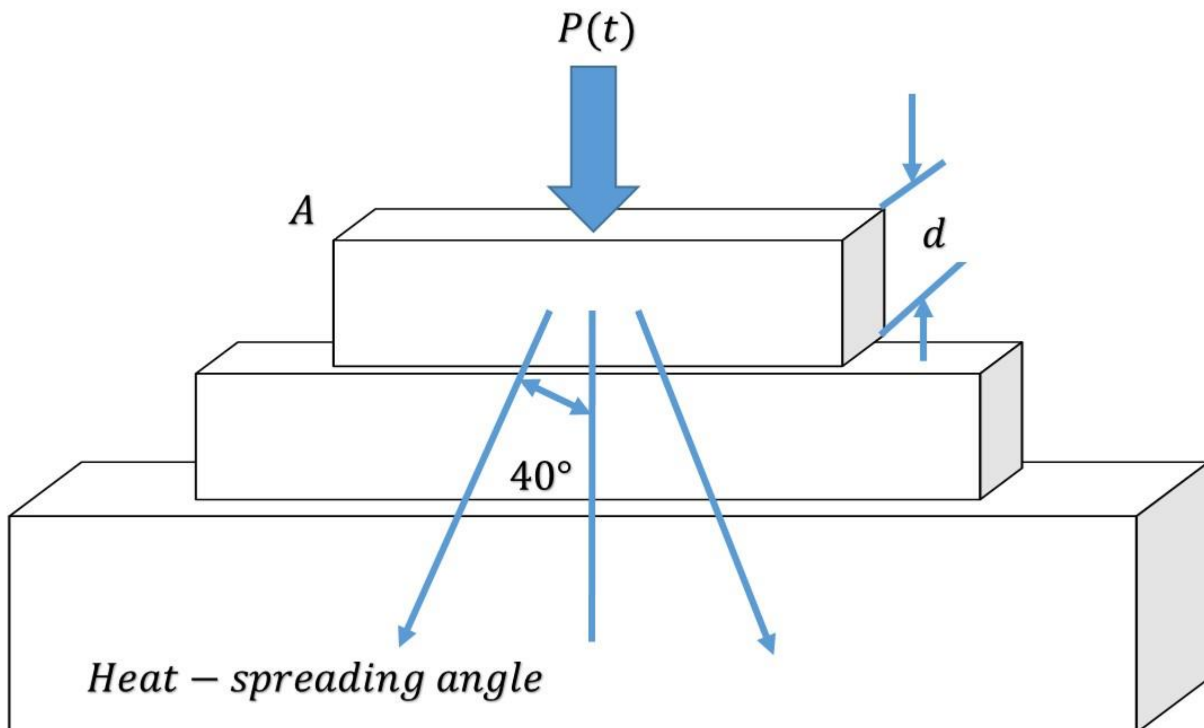

Figure C.4 Physical structure used for extracting thermal parameters.

The simplified assumption of uniform distribution of the temperature on the surface of the corresponding structure at each layer and this surface is treated as a node in the RC network circuit method. However, in practice, the cross-sectional areas of the heat conducting material in each layer behave differently, thus the heat spreading influence needs to be taken into account. Therefore, a heat spreading angle of 40° [204], some often 45° is assumed typically, but this kind of simplification still poses problems and generates errors to the system. In

particular, heat propagates through the active volume of the components, and it has a significant influence on the thermal capacitance and can be hardly accurately calculated without including the 3-D heat diffusion process. Therefore, the accuracy of using this lumped parameter type approach based on fixed angle method to predict the dynamic performance of junction temperature is a big concern. This problem has been attempted to solve by applying variable angle method. Still, the variable angle method is complicated to derive mathematically and also produces error and complexity in modelling multi-heat source problem. In addition, this approach might not provide an accurate estimation of heat convection modelling from the cold plate to the coolant because it is typically characterised by employing only a fixed/ constant heat transfer coefficient.

Representation of Foster type (RC) behavioural network

The lumped network derived using the physical structure of the components mentioned above demonstrates the capability in reducing computational load because it eliminates the nodes or meshes in the numerical simulation from millions to dozens or even less. However, numerical approaches like FEA and CFD have the features of solving complex problems including the heat and coolant flow much more accurately. Thus it is required to develop a modelling method which can capture the advantage of refined the thermal network parameter from the detailed temperature distribution.

The RC foster type network parameters extracted are used to build the thermal network and coupled to electrical network model to solve the electro-thermal interaction problems in a circuit simulator. The equivalent foster type network consists of R and C elements in this model are extracted by curve –fit approach to the transformed transient thermal impedance for IGBT power module. To build the RC parameter that will be used to build thermal network model, the first step is to derive the transient thermal response under the defined power dissipation P. The temperature rise ΔT is determined by fixing the case at a constant temperature T_{ref} and obtaining the changes of junction temperature T_j versus time t by selecting the nodes at the design interest layer of the package [205].The second step is to transform the transient thermal response into transient thermal impedance curve by using the equation.

The definition of transient thermal impedance can be expressed as:

$Z_{th}(t) = \frac{T_j(t) - T_{ref}}{P}$ .... (C.5)

To use this RC parameter for any power dissipation profile, the thermal system is assumed to be linear. The linearity of the system needs to be verified. In general, a system is said to be linear time invariant (LTI) system if the system maintains the properties of linearity and time-invariant. Clearly, the transient thermal impedance corresponds in system theory to the step response of the system with zero initial condition, and therefore it contains the full thermal description of the system [206]. To use the RC parameter from the transient step response, the prediction of transient junction temperature under any power dissipation profile can be estimated by using this following equation [207]:

$T_j(t) = T_0 + \int P(t) Z_{th}(t - \tau) d\tau$ .... (C.6)

Where, T_o is the initial temperature and $Z_{th}(t)$ is the time derivative of the thermal impedance, which corresponds to the thermal impulse response of the system.

This method simplifies the thermal problem as it uses the thermal transient behaviour of the system only and does not consider the detailed physical geometric structure and the structure material. This method solves thermal problem taking the power loss as input and producing system response temperature rise as output.

Benefits reaped from the above equation can be useful for power electronics engineer to perform thermal analysis and prediction of temperature can be estimated using the manufacturer given transient thermal impedance curve of junction to case Z_{jc} of IGBT module. The typical thermal impedance curve for Semikron- SKM 75GB123D IGBT Module is shown in Figure C.5.

The next step is obtaining equivalent thermal network parameters from the step response provided by the manufacturer provided data sheet, measured experimentally and FEA simulated transient thermal impedance curve. Typically, there are various approaches can be adopted to obtain the step response. However, the thermal network from step response expressed as Foster equivalent as shown in Figure C.6 find the wide application in representing thermal branch for the corresponding layer because it is easy to extract the coefficient of it from the measured or simulated thermal impedance curve [203].

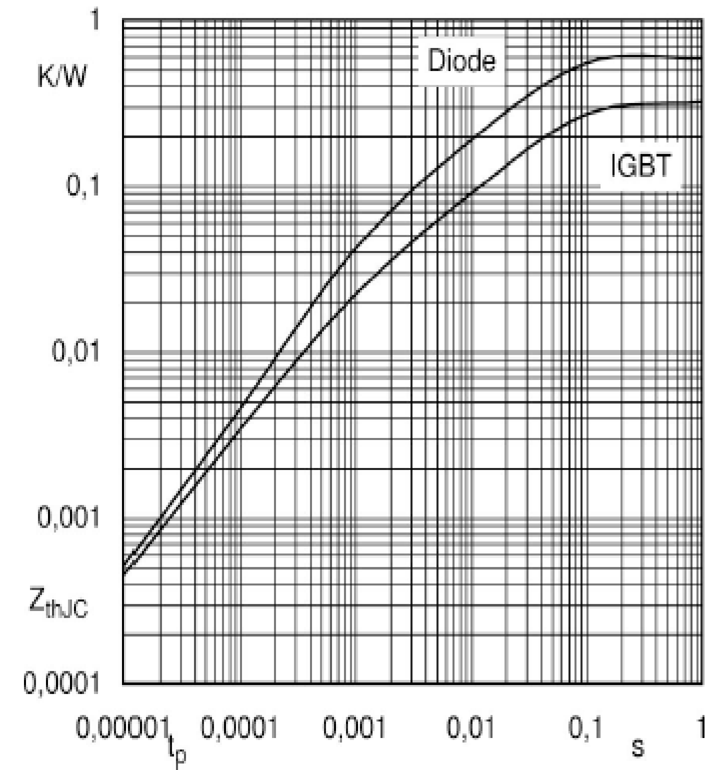

Figure C.5 Typical Transient Thermal impedance curve for Semikron- SKM 75GB123D IGBT Module [190].

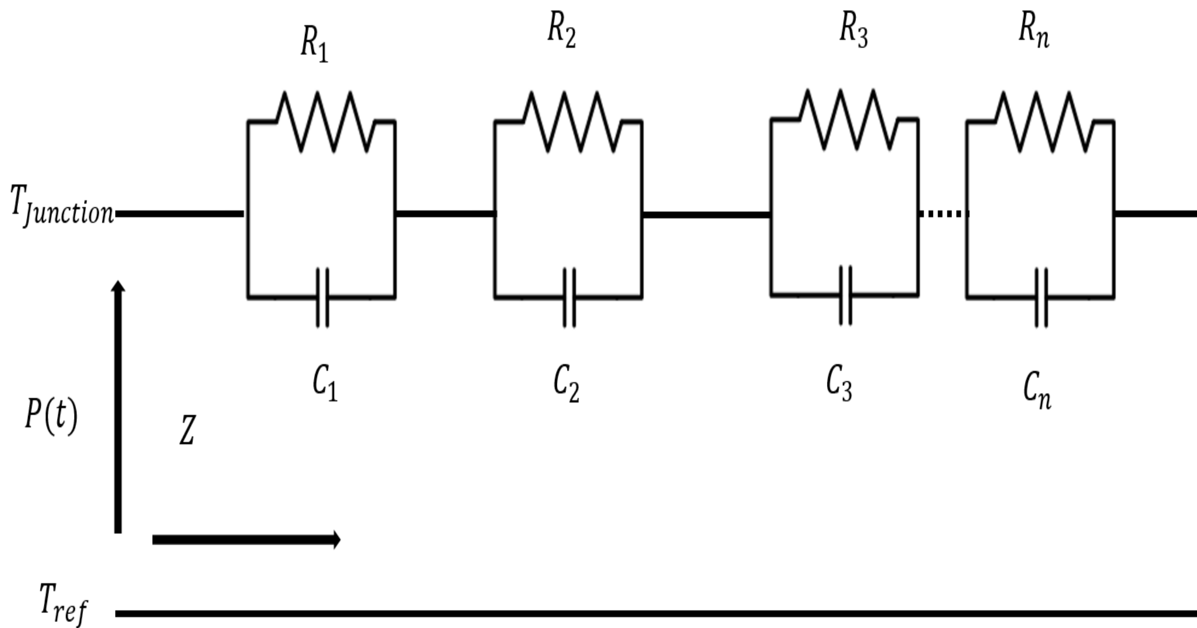

Figure C.6 Typical Foster equivalent network.

When extracting the Foster network, the transient thermal impedance curve can be represented through the fitting into a series consists of a finite number of exponential terms as given in

$$Z_{jc}(t) = \sum_{i=1}^{n} R_i * (1 - \exp(-\frac{t}{R_i C_i})\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(C.7)}$$

Where,

R_i Thermal resistance at i^{th} order

C_i Thermal Capacitance at i^{th} order

Foster network can be transformed into Cauer network by mathematical treatment adopted from [208]. Figure C.7 shows the equivalent Cauer network model where the node to node heat transfer occurs.

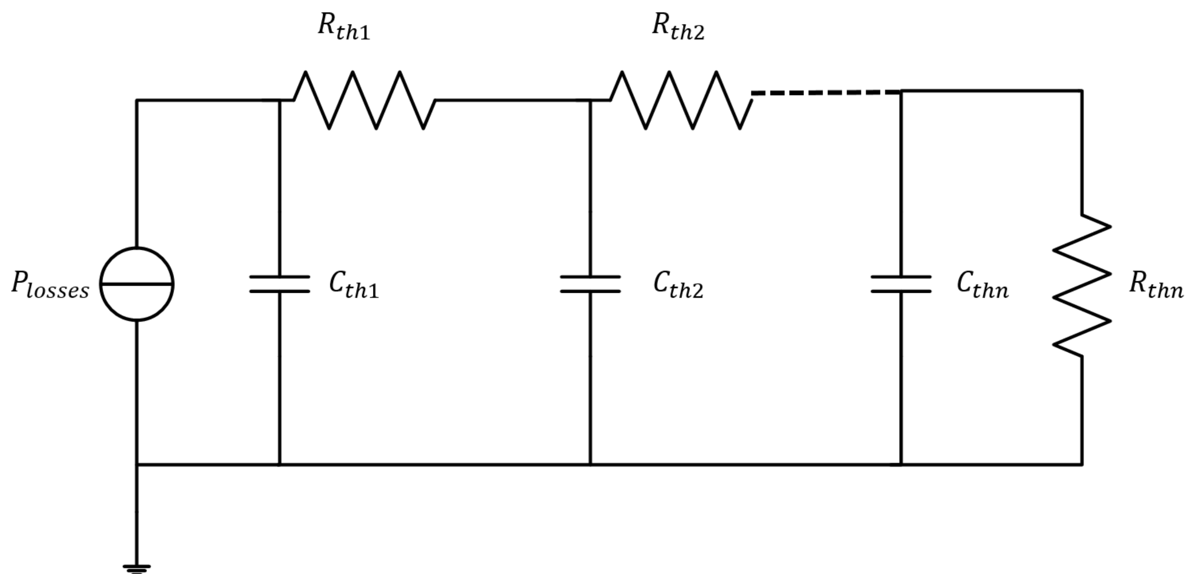

Figure C.7 Typical Cauer equivalent network.

The above mentioned foster type RC network offsets the trade-off between the computational speed and accuracy of the calculation process. The reason for wide use in dealing electro-thermal simulations by circuit simulator applications such as PLECS or SABER lies in the advantages of ease of integration with an electrical model. However, these modelling still

lacks in dealing the thermal interaction of the components and thermal dynamics of the cooling system, and this is going to be addressed later.

Firstly, this method focuses on modelling the chips individually that forms power module. For the simplification purposes, the case temperature is considered to be constant value T_{ref} as shown in [105], [208]. However, less efforts have been spent in modelling the interaction between chips in the entire system including both the power module and heatsink and the much more effort has been invested in understanding the thermal performance of the entire system [63]. Meanwhile, studying the electro-thermal performance based on the physics based RC network has been mentioned in few papers [102], the practicability/suitability of using the RC network model to model the whole system has rarely been explored.

Secondly, the most fundamental criteria of using this RC type foster network method is that that the respective system should be an LTI (Linear time invariant) system. As the transfer function of the system is time independent, the time invariant property of the system can easily be satisfied. However, the linearity of the system needs to be further tested and focused. It is generally acknowledged that the thermal model of the IGBT power module could be treated as linear. The assumptions are considered as 1) the temperature dependencies of the densities and specific thermal properties of the material can be avoided 2) Only the thermal conduction is regarded 3) The materials are assumed thermally homogenous and isotropic. However, these assumptions have seldom been verified with a high level of importance. Also, the analysis of the linearity property in the system without considering the temperature dependencies and heat spreading effects in the entire system has rarely been assessed.

In addition, if a model of the entire system is going to be established, the properties of linear time invariant system seem to be verified again because heat transfer process in the form of convection between the heat sink and the ambient could be a nonlinear issue and connecting the heatsink to the system may also generate an adverse effect on the thermal spreading within the IGBT power module.

Another disadvantage of the conventional behaviour based RC networks is that it does not take into the account thermal coupling effect from multiple heat sources [209], which may also introduce errors.

Based on the behavioural type RC network method and its drawbacks mentioned above, the thermal model used in this research will be developed. The summary of the problems that will be solved in the following part of the chapter is listed below:

1. Feasibility of applying the RC network method to build a thermal model of the converter containing IGBT and diode and for inverter interaction between IGBT and diode chips and for interleaved boost converter interaction between switching elements will be discussed.
2. The effect of non-linearity on the model behaviour i.e. temperature dependent material properties, cooling boundary condition variation, power loss variation will be evaluated and the linearity of the system will be assessed.
3. Thermal interactions will be modelled, and the effect of distance on the thermal couplings will be investigated.
4. Furthermore, a comparison will be carried out to model the coupling effect on the prediction of temperature using the manufacturer given lumped parameter and the model build from the refined RC thermal parameter from full FEA analysis. The error in results of temperature prediction by manufacturer lumped parameter will be discussed.

Appendix D: Heat Sink Design

The MOSFET and boost diode share the same heatsink, thermal resistors are modelled as in Figure D.1. Design equations are adapted from [210]. In this evaluation the maximum heatsink temperature T_s is regulated to $60°C$, so we can calculate the average junction temperature for the MOSFET and diode as follows:

$$T_{j.Diode} = T_s + P_{diode} * (R_{thcs.diode} + R_{thjcdiode}) \qquad \text{(D.1)}$$

$$T_{j.IGBT} = T_s + P_{IGBT} * (R_{thcs.IGBT} + R_{thjcIGBT}) \qquad \text{(D.2)}$$

The T_s can be regulated by choosing a heatsink that with certain airflow can reach the thermal resistance (R_{thsa}) calculated below:

$$R_{thsa} = \frac{T_s - T_a}{P_{IGBT} + P_{diode}} \qquad \text{(D.3)}$$

Where:

R_{thjc} : Thermal resistance from junction to case, this is specified in the IGBT and Diode datasheets.

R_{thcs} : Thermal resistance from case to heatsink, typically low compared to the overall thermal resistance, its value depends on the interface material, for example, thermal grease and thermal pad.

R_{thsa} :Thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets, it depends on the heatsink size and design, and is a function of the surroundings, for example, a heat sink could have difference values for different airflow conditions.

T_s: Heat sink temperature

T_c: Case temperature

T_a: Ambient temperature

P_{IGBT}: IGBT total power loss.

P_{diode}: Diode total power loss.

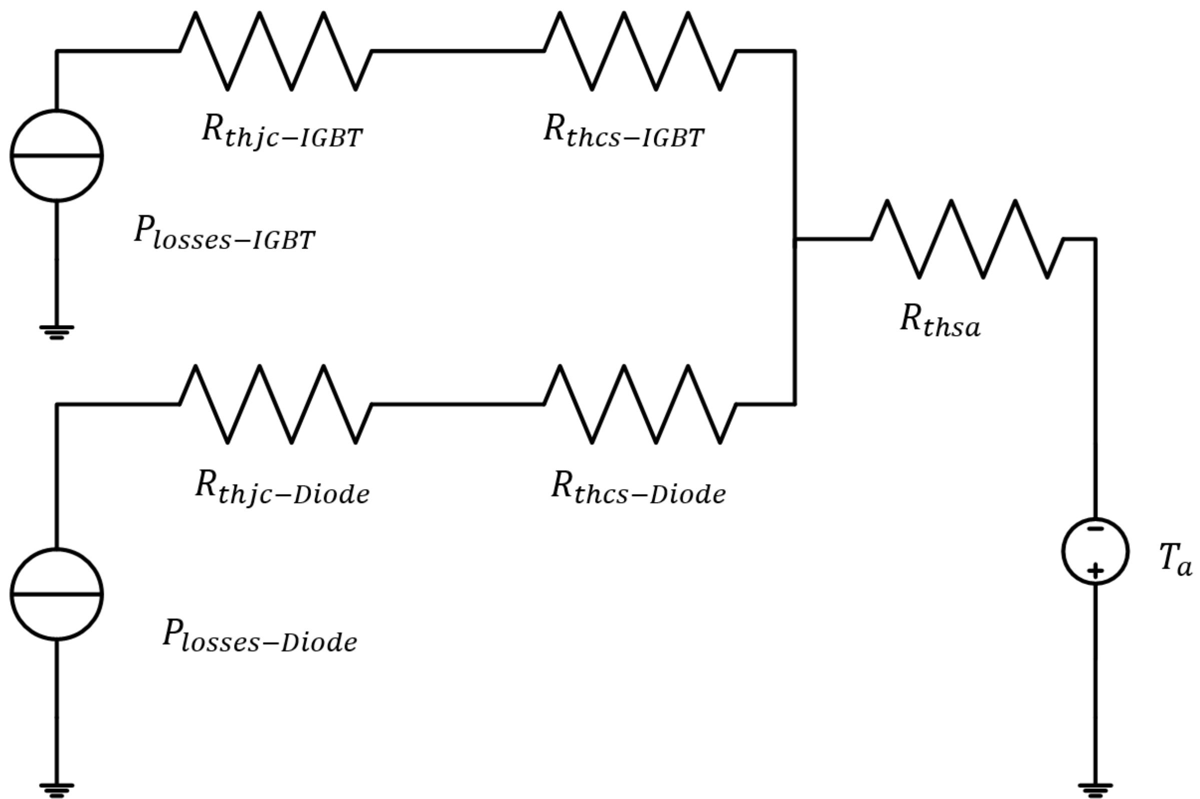

Figure D.1 Schematic of thermal network.

Appendix E: Inductor Design

The most basic relationship to configure the windings for high frequency components is the penetration depth equation. As the frequency increases, eddy currents are induced in the middle of the wire leads to an opposing current flowing. This reduces the current in the middle of the wire and more of the current flows on the surface. The simplest way to tackle/counteract this is to use Litz wires where a large number of smaller insulated wires is bundled together to form a single wire.

Equation (E.1) assumes that by the depth δ the current density have decreased to e^{-1} of the surface current density. In this area it is assumed that the current is constant and deeper it is zero. As it can be seen in the equation (E.1) the penetration depth increases with high resistivity in the wire so in a high temperature design, larger Litz wires can be used compared to a normal temperature. Larger wires increase the thermal conductivity and fill factor however some problems might happen as the component is heated up to the operation temperature. The penetration depth ranges from 0 to 100 kHz.

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad \text{(E.1)}$$

Where

δ Skin depth

ρ Resistivity at the operating temperature

μ Permeability

The windings of the inductor are affected by skin effect and proximity effect. The skin effect of the conductor increases the resistance factor of the windings. The skin effect increases with frequency, causing an inhomogeneous current distribution.

Dowel equation can be used to calculate ac resistance of the foil conductor. To take into account the effect of the core window size porosity factor has been considered in the modified Dowell equation.

Equations for estimating resistance due to skin effect and proximity effect are adapted from [211].

AC resistance of the foil winding can be written as follows:

$$R_{ac} = \frac{\rho l_w N}{\delta W}\left[x_1 + {\eta_w}^2 \frac{2}{3}(N^2 - 1)x_2\right] \quad \text{(E.2)}$$

Where

x_1 the skin effect factor

$$x_1 = \frac{\sinh(2\Delta') + \sin(2\Delta')}{\cosh(2\Delta') - \cos(2\Delta')} \quad \text{(E.3)}$$

x_2 the proximity effect factor

$$x_2 = \frac{\sinh(\Delta') - \sin(\Delta')}{\cosh(2) + \cos(\Delta')} \quad \text{(E.4)}$$

Δ Represents the penetration ratio:

$\Delta = \frac{d_w}{\delta}$ .... (E.5)

Δ' Represents the modified penetration ratio:

$\Delta' = \sqrt{\eta_w}\Delta$ .... (E.6)

η_w The porosity factor

$\eta_w = \frac{W}{h_c}$ .... (E.7)

Fr Resistance Factor

$F_R = \frac{R_{ac}}{R_{dc}}$ .... (E.8)

$R_{ac} = FrR_{dc}$ .... (E.9)

N The number of layers

δ The skin depth

l_w The mean length of one turn

W The width of foil layer

h_c The core window size

d_w The thickness of the foil

R_{ac} AC resistance

R_{dc} DC resistance

Inductor design example for Boost converter

To illustrate the preceding design toolbox, a design procedure for an inductor in the boost converter operating in CCM is given in this section. In addition, the winding loss of the

inductor over a wide range of operating conditions, when the dc load current and the dc input voltage vary, is presented here.

The inductor for PWM converters in CCM should satisfy the following conditions [174]:

1. Inductance $L > L_{MIN}$ required for CCM operation.
2. Maximum value for the peak magnitude flux density $B_{max} < B_{sat}$. Typically, for ferrite cores, $B_{sat} < 0.5T$ at room temperature and $0.3T$ at 90°C.
3. Inductor power loss $P_L < P_{Lmax}$
4. Maximum current density $J_{max} < J_{MAX}$. Typically, $J_{MAX} = 0.1 - 5A/mm^2$

The PWM dc-dc boost converter circuit is shown in Figure E.1.

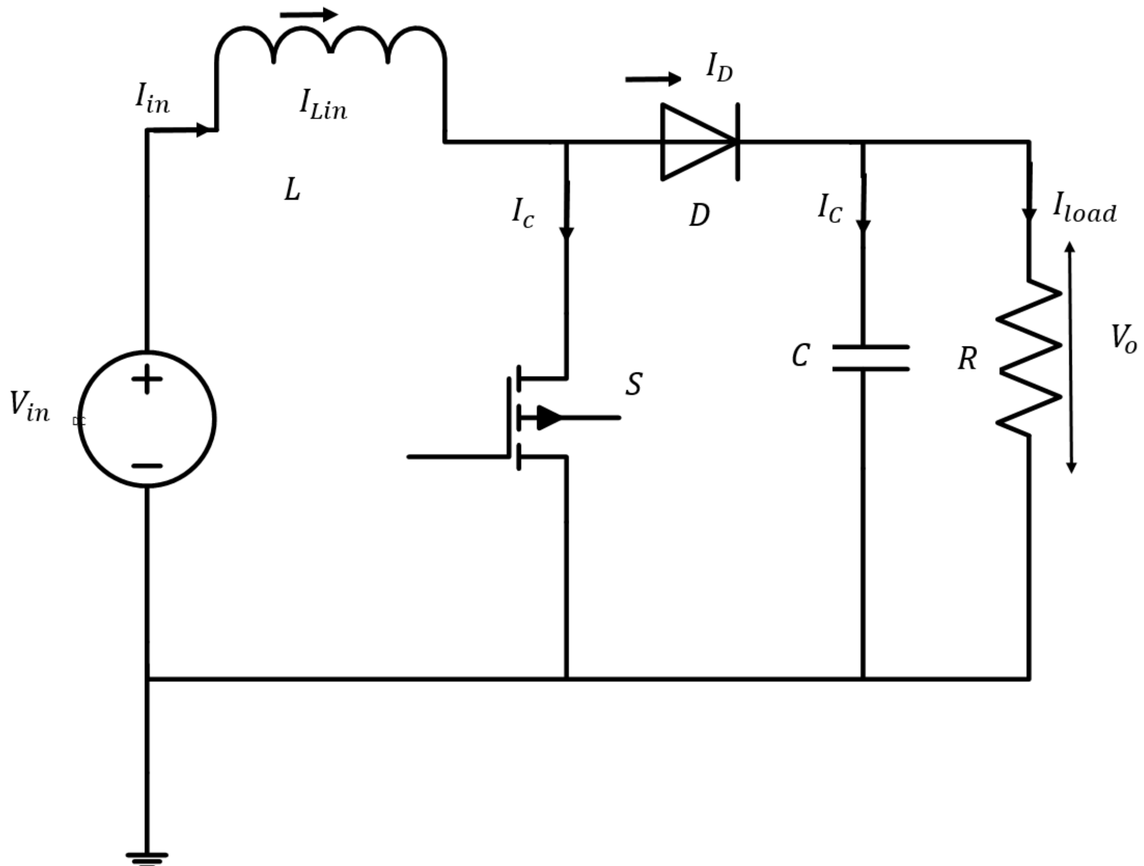

Figure E.1 PWM DC-DC boost converter circuit.

Converter Specifications

A boost PWM converter is operated in the CCM and has the following specifications: input voltage, $V_{in} = 250V$, output voltage, $V_o = 500V$, load current, $I_{load} = 10A$, ripple

voltage, $\frac{V_r}{V_o} \leq 1\%$ and switching frequency $f_{sw} = 20kHz$. The inductor required to meet the design specifications will be designed using area-product A_p method as follows:

Inductance required for CCM operation

The converter design equations relevant to the inductor design are presented here. The duty cycle of the boost converter is given by $D = 1 - \frac{V_{in}}{V_o}$.............................. (E.10)

The minimum value of duty cycle is $D = 1 - \frac{V_{in}}{V_o} = 1 - \frac{250}{500} = 0.5$.................. (E.11)

Also, the maximum value of load resistance is obtained as:

$R_{loadmax} = \frac{V_o}{I_{load}} = \frac{500}{10} = 50\Omega$.. (E.12)

The minimum value of inductance required for CCM operation is

$L = \frac{D.V_{in}}{f_s.\Delta I_{ripple}} = \frac{0.5*250}{20e3*0.3} = 1000mH$... (E.13)

For the boost converter, the dc component of inductor current is equal to the input current [174]. The maximum value of peak-to-peak inductor current ripple is

$\Delta Iripple = 30\%\ of\ I_{in} = 6.2214A$.. (E.14)

Thus, the maximum peak inductor current is

$I_{Lmax} = I_{in} + \frac{\Delta Iripple}{2} = 20.4082 + \frac{6.1224}{2} = 23.4694A$................................. (E.15)

The maximum energy stored in the inductor is

$W_m = \frac{1}{2} L I_{Lmax}{}^2 = \frac{1}{2} * 1000 * 10^{-3} * 23.4694 = .2811J$.............................. (E.16)

Core Selection

Core selection involves the selection of magnetic material, geometry and size of the core as well as the bobbin. The core material is chosen based on the operating frequency. An

amorphous Metglass AMCC core with relative permeability $\mu_{re} = 45000$ for saturation magnetic flux density $B_{sat} = 1.56T$ at room temperature and Curie temperature $T_c \geq 395°C$ is suitable for the required switching frequency of 20 kHz [174].

The inductor core is designed using the area-product method. Assume window utilisation factor $K_u = 0.4$, peak magnetic flux density, $B_{peak} = 1.2T$ and current density $J_{max} = 5A/mm^2$ .The required core area product is

$$A_P = \frac{2*W_m}{K_u*J_{max}*B_{peak}} = \frac{2*.2811}{.4*5*10^6*1.2} = mm^4 \qquad \text{(E.17)}$$

Select a core with area product A_P, cross-sectional area A_c , mean length l_m, gap length l_g. The dimensions of the selected core are given in Table E1 and core geometric structural view is shown in Figure E.2.

Table E1 Core dimension overview

Core-type	A[mm]	B[mm]	C[mm]	D[mm]	E[mm]	F[mm]	l_m [mm]	A_c [mm]	Mass[g]
AMCC-63	16	20	70	30	52	102	244	394	703
AMCC-25	13	15	56	25	41	82	194	267	379
AMCC-16B	11	13	50	25	35	72	170	226	281
AMCC-8	11	13	30	20	35	52	130	180	172
AMCC-6.3	10	11	33	20	31	53	128	164	154
AMCC-4	9	10	32.8	15	28	50.8	122	111	99

After simulating with above core only AMCC-63 meets the core product area formula.

The core utilisation window area is

$$W_a = \frac{A_P}{A_c} \qquad \text{(E.18)}$$

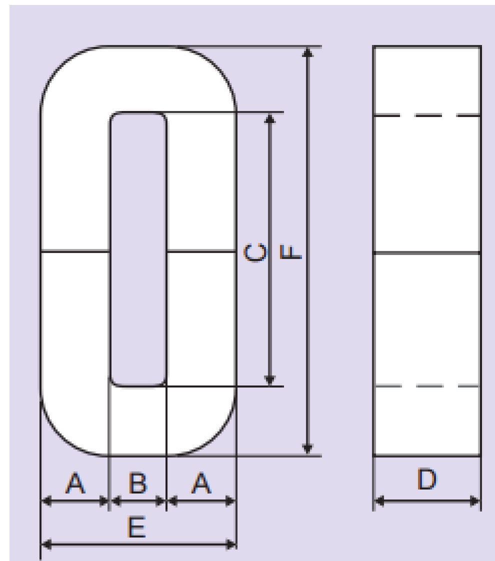

Figure E.2 Core geometric structural view.

Number of Turns

The number of turns required to obtain the specified inductance with the selected gapped core is obtained as

$$N = \sqrt{\frac{L*(l_g+\frac{l_m}{\mu_i})}{4\pi*A_e*F*10^{-7}}} = \sqrt{\frac{1000*(7.11*10^{-4}+\frac{244*10^{-3}}{1000})}{4\pi*394*10^{-6}*1.0699*10^{-7}}} = 43 \qquad \text{(E.19)}$$

The pick value of the total magnetic flux density, which consists of both dc and ac components, in the designed inductor is given by

$$B_{acpeak} = \frac{L*\Delta I_{peak}}{N*A_e} = \frac{1000*10^{-3}*3.0612}{43*394*10^{-6}} = 0.1763 < 1.2T \qquad \text{(E.20)}$$

Wire Selection

Wire selection involves the selection of material, shape, and size of the conductor as well as the thickness of insulation.

The required wire-cross-sectional area to handle the specified current density is

$A_w = \frac{I_{max}}{J_{max}} = \frac{23.4694}{5*10^6} = 4.693mm^2$ ………………………………………………… (E.21)

The required wire cross-sectional area with the required number of turns in the chosen core is

$A_{winding} = \frac{K_u W_a}{N} = \frac{0.4*16*10^{-3}*70*10^{-3}}{43} = 13mm^2$ …………………………………… (E.22)

Select a round solid copper wire with bare diameter, insulated diameter.

The bare area cross-sectional area is

The skin depth at the switching frequency $f_{sw} = 20kHz$ is

$\delta_w = \sqrt{\frac{\rho_w}{\pi \mu_0 f_{sw}}} = \sqrt{\frac{2.1124*10^{-8}}{\pi*4\pi*10^{-7}*20*10^3}}$ =.517mm……………………………………… (E.23)

Appendix F: Temperature Dependency of the Capacitor ESR

Temperature dependency of the capacitor ESR:

It can be observed in Figure F.1 that the ESR of either the film capacitor or the electrolytic capacitor has a significant change under different temperatures. Especially, the ESR of the film capacitor has experienced a significant drop along with the increase in temperature. Therefore, it can be pointed out that the hot-spot temperature calculation can lead to an error without considering temperature dependency ESR and thus produce low confidence in a thermal simulation. This can lead to inaccurate lifetime estimation. In case of using film capacitor ESR should be taken into consideration in order to achieve a reliable and accurate health monitoring of the DC-link capacitor.

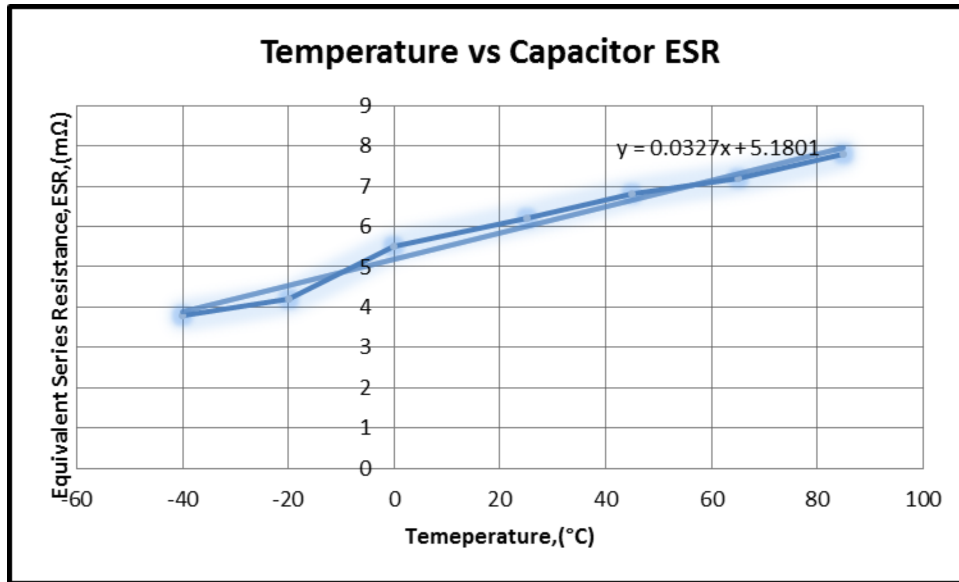

Figure F.1 Temperature dependency of the DC-link capacitor equivalent series resistor (ESR).

The relationship between temperature vs capacitor ESR has been established from the curve fitted expression:

$y = 0.0327x + 5.1801$…………………………………………………………….. (F.1)

Where,

y: Capacitor ESR

x: Temperature

The non-linear relationship of the capacitor ESR dependent to temperature has been included in the loss model coupled to an electric-thermal domain. The temperature obtained from an electro-thermal model is further feedback to the capacitor ESR loss model. Suppose, the temperature obtained from the initial assumed ESR will introduce new ESR value and thus, a new loss will be generated and applied to the thermal model. This model will iterate up to reaching the steady-state value.

Appendix G: Heatsink Modelling

The program calculates automatically the average heat transfer coefficient. Also the Nusselt number, Thermal resistance of the heat sink can be estimated .The thermal resistance of baseplate $R_{th,baseplate}$, Fin thermal resistance $R_{th,fin}$, thermal resistance to baseplate to air $R_{th,a}$, and thermal resistance fin to Air $R_{th,A}$ can be estimated. As, the thermal

resistances $R_{th,fin}$, $R_{th,A}$ and $R_{th,a}$ depend on the volume flow, the geometry and the position along the longitudinal axis of the channel, the effect of this must be taken into account in a single thermal convective resistance and these can be accurately modelled according to [182], [183], [185] .The thermal resistance has been expressed as follows:

$$R_{th,conv} = [\rho_{air} c_{air} V \left(1 - e^{\frac{-hA_{eff}}{\rho_{air} c_{air} V}}\right)]^{-1} \quad \text{(G.1)}$$

With the effective convective surface area A_{eff} and the fin efficiency η[10]

$$A_{eff} = n(2c\eta + s)L \; with \; \eta = \frac{\tanh(\sqrt{\frac{2h(t+L)}{\lambda_{hs} tL}} * c)}{\sqrt{\frac{2h(t+L)}{\lambda_{hs} tL}} * c} \quad \text{(G.2)}$$

Where:

ρ_{air}: Density of air

c_{air}: Thermal capacitance of air

V: Volume flow through the heatsink $[\frac{m^3}{s}]$

A_{eff}: Effective convective surface area

h: Average heat transfer coefficient

η: Fin efficiency

t: Fin thickness

L: Heat sink length

c: Fin height

s: Spacing between two consecutive fluid flow channel

λ_{hs}: Thermal conductivity of heatsink material

Thermal Model of Heatsink:

The easiest way of solving 3-D heat conduction problem is to represent the cooling system structure as a network of thermal resistances. Using heat-sink symmetries the thermal resistance can be expressed as shown in equation G.3 [185].

$$R_{th,S-a} = R_{th,d} + \frac{1}{n} * \frac{(R_{th,fin}+R_{th,A})*R_{th,a}}{R_{th,fin}+R_{th,A}+2R_{th,a}} = R_{th,d} + R_{th,conv} \qquad \text{(G.3)}$$

And radiation is neglected. Based on the assumption of a uniform loss distribution across the heat sink base plate area $A_{hs} = bL$, the thermal resistance $R_{th,d}$ is a function of the heat sink geometry and the heat sink material's thermal conductivity λ_{hs} , i.e.,

$$R_{th,d} = \frac{t_{base}}{A_{hs}*\lambda_{hs}} \qquad \text{(G.4)}$$

Fin thermal resistance $R_{th,fin}$, thermal resistance to baseplate to air $R_{th,a}$ and thermal resistance fin to Air$R_{th,A}$ etc. are highly dependent on the volume flow, the geometry, and the position along the longitudinal axis of the channel. According to [182] and [183] , these dependencies can be accurately modelled with the single fluid heat exchanger model that summarizes the thermal resistances $R_{th,fin}$, $R_{th,A}$ and $R_{th,a}$ in a single convective thermal resistance [185].

$$R_{th,conv} = [\rho_{air}c_{air}V\left(1 - e^{\frac{-hA_{eff}}{\rho_{air}c_{air}V}}\right)]^{-1} \qquad \text{(G.5)}$$

With the effective convective surface area A_{eff} and the fin efficiency η[10]

$$A_{eff} = n(2c\eta + s)L \; with \; \eta = \frac{\tanh(\sqrt{\frac{2h(t+L)}{\lambda_{hs}tL}}*c)}{\sqrt{\frac{2h(t+L)}{\lambda_{hs}tL}}*c} \qquad \text{(G.6)}$$

Non-dimensional Nusselt number (Nu) is a function of average ducted fluid velocity, duct geometry and the fluids Prandtl number (Pr) which represents boundary layer velocity in determining average heat transfer coefficient. Analytical model derived by Muzychka and Yovanovich [184] for the Nusselt number applicable for the extruded-fin heat sink model, which takes into account the effect of flow development at the inlet of a duct with arbitrary cross-section as follows:

$$Nu_{\sqrt{A}} = [(\frac{C_4 f(Pr)}{\sqrt{Z^*}})^m + (\left\{C_1\left(\frac{fRe_{\sqrt{A}}}{8\sqrt{\pi}\varepsilon^{\gamma}}\right)\right\}^5 + \left\{C_2 C_3\left(\frac{fRe_{\sqrt{A}}}{\sqrt{Z^*}}\right)^{\frac{1}{3}}\right\}^5)^{\frac{m}{5}}]^{\frac{1}{m}} \qquad \text{(G.7)}$$

The required coefficients C_1, C_2, C_3, C_4, γ, and functions $f(Pr)$, $fRe_{\sqrt{A}}$, Z^*, ε, and m , as provided in [184] ,are summarized below.

$$f(Pr) = \frac{0.564}{[1+\left(1.664 Pr^{\frac{1}{6}}\right)^{\frac{9}{2}}]^{\frac{2}{9}}} \qquad \text{(G.8)}$$

$$Pr = \frac{C_p \mu}{k} \qquad \text{(G.9)}$$

$$C_1 = 3.24$$

$$C_3 = 0.409$$

$$C_2 = 1.5$$

$$C_4 = 2$$

$$\gamma = -\frac{3}{10}$$

$$m = 2.27 + 1.65 Pr^{\frac{1}{3}}$$

$$Z^* = \frac{LnV_{air}}{Pr*V} \qquad \text{(G.11)}$$

$$\varepsilon = \left\{\frac{s}{c}, \text{ if } s \leq c\right.$$

$$\varepsilon = \left\{\frac{c}{s}, \text{ if } s > c\right.$$

$$fRe_{\sqrt{A}} = [\frac{11.8336*V}{Lnv_{air}} + (fRe_{\sqrt{A},fd})^2]^{\frac{1}{2}} \qquad \text{(G.12)}$$

$$fRe_{\sqrt{A},fd} = \frac{12}{\sqrt{\varepsilon}(1+\varepsilon)[1-\frac{192}{\pi^5}\varepsilon \tanh\left(\frac{\pi}{2\varepsilon}\right)]} \quad \text{(G.13)}$$

$$h = \frac{Nu_{\sqrt{A}}\lambda_{air}}{d_h} \quad \text{(G.14)}$$

with

$$d_h = \frac{2sc}{s+c} \quad \text{(G.15)}$$

$$s = \frac{b-(n+1)*t}{n} \quad \text{(G.16)}$$

Where,

d_h : Hydraulic diameter of the heat sink channel

s: Spacing between two consecutive fluid flow channels

c: Fin height

b: Heat sink width

L: Heat Sink length

n: Number of fluid flow channel

t: Fin thickness

h: Average heat transfer coefficient

γ: Shape parameter

m: Blending parameter

Z^* : Shape functions

C_1, C_3 : Coefficient for UWT boundary conditions

C_2, C_4: Coefficient for average Nusselt number

V_{air}: Velocity of air

V: Volume flow through the heatsink $\left[\frac{m^3}{s}\right]$

$fRe_{\sqrt{A}}$: Friction factor Reynolds product function

Appendix H: Average Power Loss Modelling

Since the switching time constants (few hundred microseconds) is much smaller than compared to thermal time constants (seconds), the detailed electrical stimulation of switching phenomena will require a time step much smaller than the switching time. In effect, simulation process will be delayed, and unnecessary computational burden will be experienced. To help tackle this problem, time-averaged smoothed switching power loss on each switching period is adopted in this present work [171].

For example, the average smoothing power for IGBT can be manipulated by the equation expressed as follows:

$$P_{Switching\ losses-IGBT}(t_s) = \frac{1}{t_s}\int_{t}^{t+t_s} P_{Switching\ \ losses-IGBT}(t)dt \quad \text{(H.1)}$$

Where t_s is the switching period.

The average smoothing power loss for diode is calculated with

$$P_{Switching\ losses-Diode}(t_s) = \frac{1}{t_s}\int_{t}^{t+t_s} P_{Switching\ \ losses-Diode}(t)dt \quad \text{(H.2)}$$

Where, t_s is the switching period.