Data Driven Prognostics for Failure of Power Semiconductor Packages

Mominul Ahsan, Stoyan Stoyanov and Chris Bailey

Computational Mechanics and Reliability Group, University of Greenwich, London, UK
Email: m.ahsan@greenwich.ac.uk

***Abstract**: Power chips such as Metal Oxide Field Effect Transistors (MOSFETs) are widely used and can be found in many electronics and electrical products. The ability to predict the degradation of such power electronic devices can minimise the risk of their failure during operation and support maintenance planning operations. In this study, a data driven prognostics approach using system identification and machine learning modelling technique is developed and used to predict the time-to-failure of MOSFET TO-220 packages associated with delamination failure mode of the die attachment. Run-to-failure data under thermal overstress loading conditions for power chip devices, available from the NASA Prognostics Centre data repository, is used to develop a data-driven prognostic model that can be used to predict the time-to-failure (TtF) of power MOSFETs under accelerated test loads. An increment in ON-state resistance of the MOSFET is used as precursor for device failure through die-attach degradation. Results from this research show that when monitored data from a damage indicator for a particular failure mode of an electronic package changes dynamically, data-driven modelling using engineering control techniques such as State-Space representation is capable of producing reliable, multi-step ahead predictions for the time-to-failure of the device.*

1. INTRODUCTION

Estimating state of health or predicting remaining useful life of power electronic devices is crucial to avoiding disruption in operational performance or failure of an electrical or electronic system. The metal–oxide–semiconductor field-effect transistor (MOSFET) is an example of electronic chip that is widely used in many electronic products in applications such as automotive, aerospace, energy, etc. Degradation of MOSFET package can lead to power failure and subsequently the failure of the complete electrical system. Majority of the current research efforts are focusing on new MOSFET designs for improving performance and reducing cost but research on assessing reliability of the devices in operation is less comprehensive. The capability to predict when electronic components may fail without any prior indication while in operation or under test can assist in designing strategies for failure prevention and efficient maintenance schedule. A powerful approach to achieve these objectives is to perform assessment of the device degradation state and to forecast time-to-failure (respectively remaining useful life) using data on performance monitoring parameters and suitable data-driven prognostic techniques.

Recent studies found that the sudden failure of electronic components occurred without any prior indication. It is extremely important to avoid such failure by obtaining early information and taking necessary steps based on that information. Data driven prognostics with the use of machine learning algorithms is a dominant approach to predict early time to failure information of the components. Therefore, it is important to understand the failure modes, mechanisms and effects for the prognostics of those components.

Data driven prognostic approaches such as Particle filters, Kalman filters, Gaussian process regression, Neural Network, Support Vector Machine (SVM) and other machine learning techniques are being employed for prognostics of electronic components [1,2]. It has been reported that data from accelerated aging experiments on MOSFET devices can help to understand the material degradation behaviour of the package and to develop mathematical models for predicting the device performance. Furthermore, data-driven prognostics strategies have been employed by

taking advantage of accelerated aging experimental data to predict remaining life of the devices under test. For example, Celaya *et al* [3-5] have examined run to failure MOSFET data for the prediction of remaining useful life (RUL) of the device aged under thermal overstress condition through a controlled accelerated aging experiment. ON-state resistance was used as the primary precursor of failure of the die attach in their work. Gaussian process regression algorithm, an extended Kalman filter with a particle filter, and Bayesian tracking framework are among the techniques used within developed and demonstrated data-driven and/or model-based prognostics approaches. Investigated models were able to provide good prediction results.

Zheng *et al* [6] have proposed a prognostic method with the use of relevance vector machine and a degradation model to predict the RUL of power MOSFET. Their degradation model was generated by fitting representative vectors and RUL of MOSFETs calculated by extrapolating the degradation model to a failure threshold. Updating of the degradation model is performed by using the difference between predicted and measured values. Results show that the proposed method can provide good RUL estimation accuracy. Wu *et al* [7] have discussed failure models and mechanisms of MOSFETs and developed a degradation model using track filter. The authors have estimated that over 34% of failures of electrical systems are happened due to power failure, whereas majority of these failures are occurred due to MOSFET failure. On-resistance of a MOSFET is identified as the key characteristics parameter for the degradation of the device. High temperature and temperature cycling have significant impact on the performance of power electronic devices; 55% of detected failures are attributed to those types of loads.

Dusmez *et al* [8] have proposed a data driven linear approximation model for estimating remaining useful life (RUL) of degraded power MOSFETs under thermal cycling condition. Accelerated aging test bed was used to identify the fault precursors of the device in a shorter time. The ON state resistance, in a logarithmic form and approximated by a linear function, was selected as precursor failure parameter. The empirical coefficients were estimated by the classical least squares (LS) approach, and outliers were identified and removed from the experimental data using random sample consensus (RANSAC) algorithm. A sliding window approach was used to track the nonlinearities. In addition, genetic algorithm was employed to optimise window size, threshold value, and number of samples of the data. The results show that the method could be useful for real-time failure prognosis.

Other MOSFET related investigations are also available in the literature [9-13]. However, only three research studies reported in the public domain have developed predictive models for the prognostics of MOSFETs, and limited number of machine learning techniques have been considered and used for the problem of prognostics of MOSFET failure. The aim of this study is to investigate the predictive capability of computational intelligence algorithm (state-space dynamic model) for predicting TtF of MOSFETs electronic components using data from monitored failure precursor parameters. Model prediction results are presented and performance of the model is evaluated comparing actual and predicted time-to-failure test data.

2. PROPOSED TIME TO FAILURE (TTF) PREDICTION METHODOLOGY

Accelerated aging is commonly adopted experimental technique to induce failure in an electronic component over practical timeframe and to identify required parameters for prognostics analysis. In this investigation, MOSFET accelerated aging experimental platform is used for the aging test developed by NASA AMES laboratory [4]. Degradation data sets of 42 individual MOSFET devices with various runs of them are collected. In addition, resistance is identified as a suitable precursor failure parameter, and calculated from the drain source current and gate voltage extracted through analysis of the experimental data sets. The resistance values are normalised to identify and compare presence of distinguishing degradation patterns. Smoothing of the normalised resistance is also carried out in order to understand the general trend in the data. State-space modelling is considered in this work to predict time to failure (TtF) of devices under test. Finally, the prediction performance of the developed prognostics model is evaluated.

Figure 1 shows the framework for predicting TtF of the degraded MOSFETs. It details also the sequential steps and activities related to data gathering and subsequent data-driven modelling for imbedded prognostics in test.

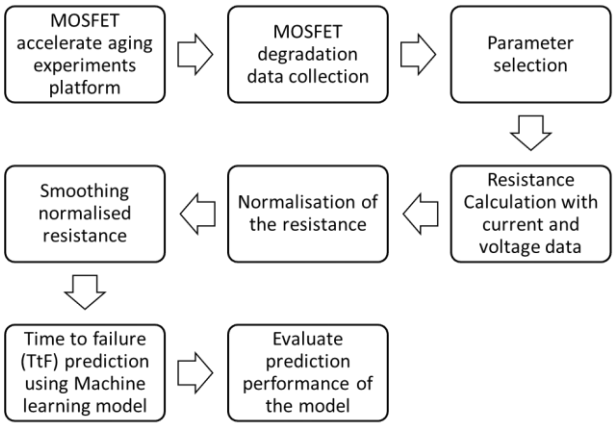

Fig. 1. Framework of time to failure (TtF) prediction for MOSFET

3. MOSFETs Degradation Experiments and Data Collection

3.1. Accelerated aging experimental set-up

MOSFETs accelerated aging experimental system was developed by AMES research center (NASA) with the help of Impact technologies to enable investigations on the degradation processes of MOSFETs packages, and for diagnosis and prognosis capability developments [4]. The main goal of the experimental work was to enable the development of prognostics algorithms for predicting TtF of MOSFETs. Power MOSFETs transistor, TO-220 package, was used for conducting the aging experiments. The accelerated aging of the device is realised by applying thermal overstress generated by indirect thermal cycling. Changes in thermal loads were induced by applied electrical power cycling under the condition that no additional heat sink was used. Under thermal cycling condition, the electronic device is subjected to quick changes in temperature, which causes cyclic expansion and contraction of the internal elements bonded together. Owing to the mismatch of thermal expansion coefficient of the bonded elements, thermal stress is generated and over the time this can lead thermo-mechanical failures in the MOSFET such as wire lift and die attach degradation. The detailed description of the accelerated aging system can be found in reference [9].

In the accelerated aging thermal oversets test, maximum and minimum temperature values are set and used to control the power ON-OFF switching of the MOSFET device. If the temperature reaches below a set minimum level, switching mode is turned ON. On the other hand, if the temperature rises above a set maximum limit, switching mode is turned OFF. When device switching takes place, a large amount of power is dissipated and this increases the temperature of the device. The parameters applied at the gate causing the device to switch rapidly during power cycling as follows: applied gate voltage with a square wave signal and an amplitude of ~15V, a frequency of 1KHz and a duty cycle of 40%. Figure 2 shows a high level schematic diagram for the accelerated aging of MOSFET. This setup uses a LabView (National Instruments) interface including data collection modules and control instruments [9]. The hardware consists of a programmable power supply as a source of 20V and 50A power. An infrared sensor and an environmental chamber are used to monitor and control the device temperature, humidity and pressure respectively.

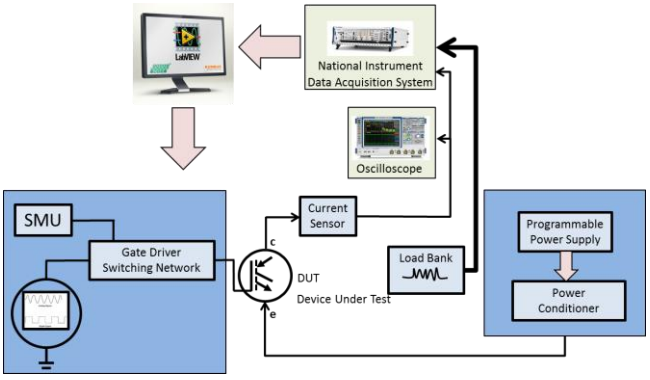

Fig. 2. Accelerated aging system for aging through thermal cycling (adapted from [4]).

3.2. MOSFET Degradation data

In this work, the experimental data for MOSFET package degradation under thermal overstress aging condition detailed in the previous section is used. The ON-state resistance, $RDS_{(ON)}$, is computed with ratio of drain to source voltage (V_{DS}) and drain current (I_D). This parameter is used as a damage indicator because $RDS_{(ON)}$ increases as die-attach degradation/ delamination starts to occur in the device. This accelerated degradation is a result of the increased junction temperature achieved by combined power cycling and externally controlled elevated temperature [3]. Figure 3 shows the normalised and smoothed resistances for a number of selected devices. It is very clear that the degradation patterns for the devices 7, 38, 32, 26 and 35 are similar even though the individual tests times range from 41 to 125 minutes.

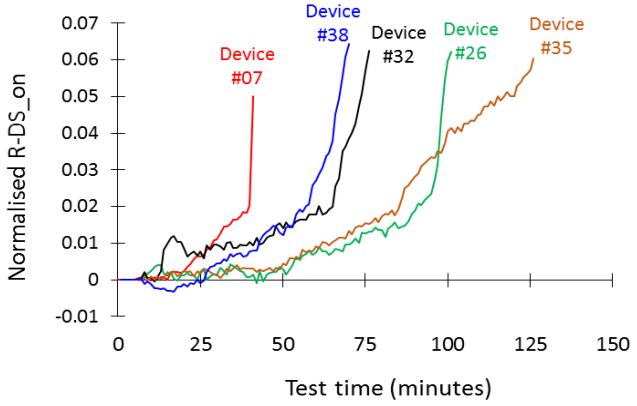

Fig. 3. Normalised ON-state resistance (R-DS_on) measurements of MOSFET power chips under accelerated degradation tests.

3.3. Data smoothing

To understand actual patterns in data, a data smoothing technique is used to remove noise from a data set. As long as a predictive model is developed by training with smoothed data, the model prediction will be more accurate and realistic compared to a model developed by training with noisy data. Therefore, data smoothing is important to improve model prediction capability [3]. Particularly, for large amount of noisy data, smoothing is essential to help predict the actual trends of the data. Data smoothing can be done in various ways.

In this case, averaging technique is used to conduct the data smoothing. The original raw measured values of the parameters in the test are gathered at high frequency. This data is first subjected to data reduction so that one parameter value per minute interval of test time is obtained. This is based on simple average of all measured values over the minute interval. Then, each parameter value is re-calculated by averaging the 10 nearest data measurements to provide the data into the desired smooth format.

Figure 4 shows a typical example of the smoothed data and actual data trends for device #8 in the dataset.

4. MOSFET Failure Prediction Results with State Space (SS) Algorithm

State space algorithm is effective for the analysis of nonlinear systems and accurately captures the dynamic behavior of a system. Further details about the algorithm can be found in references [14-16].

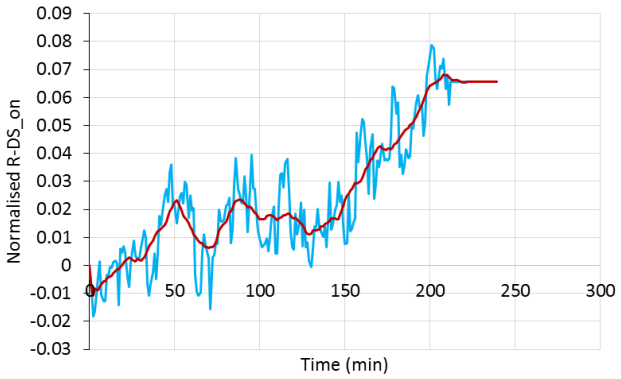

Fig. 4. Smoothing of degradation noisy data for device 8.

4.1. Multistep ahead prediction using SS model

The normalised resistance (R-DS_on) with respect to the virgin device condition is used to represent the degradation process and detect the time of failure represented with a threshold value of 0.055 (Figure 5). State space data-driven prognostic model was developed using the measured data for ON-state resistance of several MOSFETs and used to identify their performances and accuracies when used to forecast the time-to-failure of a device.

The performance of state-space model developed in the study, is evaluated for different multi-step ahead prediction. As an example, the accuracy of the model predictions for device #38 data is demonstrated. Figure 5 shows 10 steps (20 mins) and 15 steps ahead (30 mins) predictions with the actual measured data (from experiment) for the device #38.

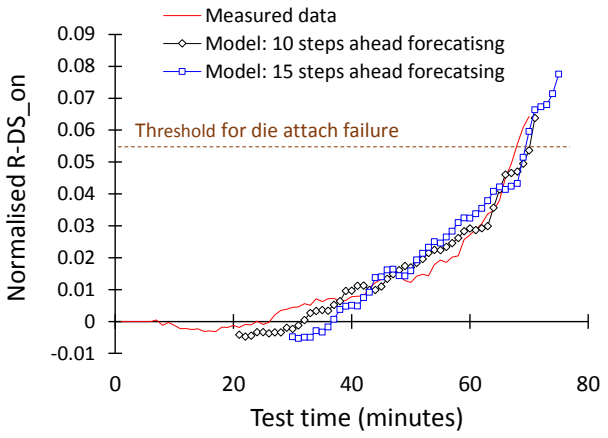

Fig. 5. ON-state resistance (R-DS_on) measured data and trajectories of the model multi-step ahead forecasts for device #38.

As expected, forecasts of remaining life over large prediction horizons become less accurate but the dynamic behaviour of the measured signal is captured well for small to medium number of forecasting steps over the sampling interval. Therefore, 10 steps ahead predictions produced more accurate results displaying a closer match to the measured data compared to the 15 steps ahead predictions. This could be explained by the fact that more data is used during trained model development for 10 steps ahead prediction and thus generated the model with better prediction capability.

4.2. Time to Failure (TtF) prediction using SS model

Time to Failure (TtF) is calculated by subtracting the time at prediction from the time when predicted resistance value is equal to or exceed the threshold resistance value (0.055). Figure 6 presents the data for TtF at different times when predictions were made. For example, at time 40 min, the time required to reach the threshold resistance value is 66 min. Therefore, the time to failure at 40 min is 26 min. For device #38, the predictions for time-to-failure are found to be robust and accurate even for the early predictions.

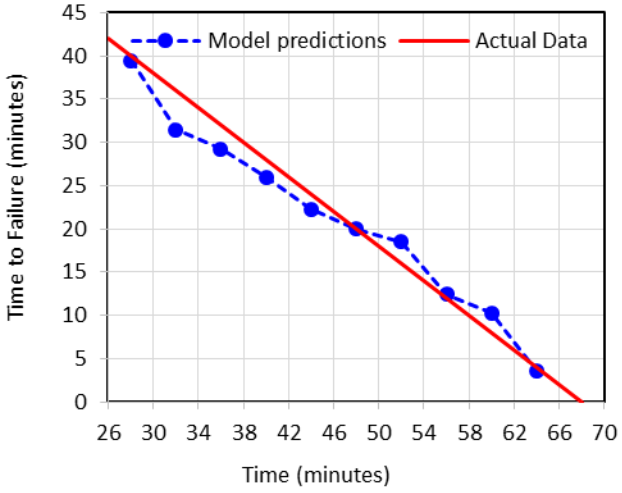

Fig. 6. Time-to-Failure prediction performance of developed state-space model for device #38.

5. DISCUSSIONS

In power electronics applications, MOSFETs play a critical role in ensuring the reliable operation of electronic system. Development of an accurate prognostic model to predict the TtF of MOSFETs is the first step towards implementation of prognostics health management capability of these electronic devices.

Measurement data from the experiments with different devices clearly show the degradation pattern follows an exponential curve. The predictive model output also follow the pattern very closely. Smoothing of the raw data will have significant influence on the prediction outcomes and model accuracies. Assessment of TtF prediction performance, as evident from Figure 6, shows that the model features very good quantitative accuracy for the devices under investigation. The values of relative accuracies presented in Table 1 also supports the performance accuracies obtained by the model. The relative accuracy values reported in Table 1 are calculated using Eq. 1:

$$RA(\%) = \left(1 - \frac{\left|TtF_{actual} - TtF_{predicted}\right|}{TtF_{actual}}\right) \times 100 \qquad (1)$$

Table 1. Prediction performance estimation by SS model.

Time at prediction	Predicted TtF (min)	Error	Relative accuracy (RA in %)
28	39.50	0.50	98.75
32	31.50	4.50	87.50
36	29.25	2.75	91.41
40	26.00	2.00	92.86
44	22.25	1.75	92.71
48	20.00	0.00	100.00
52	18.50	-2.50	84.38
56	12.40	-0.40	96.67
60	10.25	-2.25	71.88
64	3.60	0.40	90.00

A number of factors influences the predictive performance of a prognostic model. These include:

a. How representative the accelerated aging data, gathered over shorter period, is of the real life degradation data (gathered over longer time period while device is in operation).

b. The accuracy of experimental data.

c. Processing of measured data: data size reduction. normalisation and smoothing.

d. Machine learning algorithm used.

6. CONCLUSIONS

This study has investigated a computational approach for Time to Failure (TtF) predictions of MOSFET device. Data driven state-space model was developed using experimental data from accelerated aging tests of MOSFETs packages and then employed to predict the TtF of the devices under test. The failure mode of interest addressed in this work was the die attach delamination failure caused by thermal overstress. The die attach degradation affected the measured values of the ON-state resistance of the device under test and hence used as precursor for the pending failure. Results from this work have shown that state-space modelling approach can provide accurate prognostics results for the time to failure. As part of the model validation checks, good agreement between model predictions and actual test data was confirmed.

REFERENCES

[1] Salunkhe, T., Jamadar, N.I. and Kivade, S.B. "Prediction of Remaining Useful Life of mechanical components - a Review", *International Journal of Engineering Science and Innovative Technology (IJESIT)*, Vol. 3, No. 6, 2014, pp. 125-135.

[2] Ahsan, M., Stoyanov, S. and Bailey, C., "Data driven prognostics for predicting remaining useful life of IGBT", *Proc. 39th International Spring Seminar on Electronics Technology (ISSE)*, Pilsen, Czech Republic, May 2016, pp. 273-278.

[3] Celaya, J.R., Saxena, A., Saha, S. and Goebel, K.F., "Prognostics of Power MOSFETs under thermal stress accelerated aging using data-driven and model-based methodologies", *Annual Conference of the Prognostics and Health Management Society*, Montreal QC, Canada, 2011, pp. 1-10.

[4] Celaya, J.R., Patil, N., Saha, S., Wysocki, P. and Goebel, K., "Towards accelerated aging methodologies and health management of power MOSFETs (Technical Brief)", *Annual Conference of the Prognostics and Health Management Society*, San Diego, USA, 2009, pp. 1-8.

[5] Celaya, J.R., Wysocki, P., Vashchenko, V., Saha, S. and Goebel, K., "Accelerated aging system for prognostics of power semiconductor devices", *Proc. IEEE AUTOTESTCON*, Orlando, USA, 2010, pp. 1-6.

[6] Zheng, Y., Wu, L., Li, X. and Yin, C., "A relevance vector machine-based approach for remaining useful life prediction of power MOSFETs", *Proc. Prognostics and System Health Management Conference (PHM-2014 Hunan)*, Zhangiiaijie, China, 2014, pp. 642-646.

[7] Wu, Li-F., Guan, Y., Li, X.J. and Ma, J., "Anomaly Detection and Degradation Prediction of MOSFET", *Mathematical Problems in Engineering*, Vol. 2015, 2015, Article ID 573980, pp. 1-5.

[8] Dusmez, S., Heydarzadeh, M., Nourani, M. and Akin, B., "Remaining Useful Lifetime estimation for power MOSFETs under thermal stress with RANSAC outlier removal", *IEEE Transactions on Industrial Informatics*, Vol. 13, No. 3, 2017, pp. 1271-1279.

[9] Sonnenfeld, G., Goebel, K.F and Celaya, J.R., "An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors", *Proc. IEEE AUTOTESTCON*, Salt Lake City, USA, 2008, pp. 208-215.

[10] Saha, S., Celaya, J.R., Vashchenko, V., Mahiuddin, S. and Goebel, K.F., "Accelerated aging with electrical overstress and prognostics for power MOSFETs", *IEEE Energy Tech.*, Cleveland, USA, 2011, pp. 1-6.

[11] Saxena, A., Celaya, J.R., Balaban, E., Goebel, K.F., Saha, B., Saha, S. and Schwabacher, M., "Metrics for evaluating performance of prognostic techniques", *Prognostics and Health Management*, 2008, Denver, USA, pp. 1-17.

[12] Celaya, J. R., Saxena, A., Vashchenko, V., Saha, S., & Goebel, K., "Prognostics of power MOSFET", *23rd International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, San Diego, USA, 2011, pp. 160-163.

[13] Goebel, K., Saha, B. and Saxena, A., "A comparison of three data-driven techniques for prognostics", *62nd Meeting of the Society For Machinery Failure Prevention Technology (MFPT)*, Virginia, USA, April 6-8, 2008, pp. 1-13.

[14] Ljung, L., "System Identification - Theory for the User", PTR Prentice Hall, Upper Saddle River, N.J., 1999, pp 132-134.

[15] Soderstrom, T. and Stoica, P., "System Identification", Publ. Prentice Hall, 1989.

[16] Viberg, M., "Subspace-based methods for the identification of linear time-invariant systems", *Automatica*, Vol. 31, No. 12, 1995, pp. 1835-1851.