Evaluation of the Impact of the Physical dimensions and Material of the Semiconductor Chip on the Reliability of Sn3.5Ag Solder Interconnect in Power Electronic Module: A Finite Element Analysis Perspective

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Abstract

This paper primarily focuses on an evaluation study for the temperature cycling capability of tin silver solder interconnect in power electronic applications by the impact of die dimensions and die material properties. The study was investigated on finite element analysis perspective on chip/solder/substrate structure. A commercially available chip was chosen in the finite element analysis (FEA) as the nominal base die. Two thermal cycle profiles were utilised. The effect of die area, die thickness and material properties (Si and SiC) on the thermal cycling capability of the solder layer was investigated from FEA perspective. From the FEA, it was concluded that decrease in die thickness resulting in increment of thermal cycling capability of solder layer for both material (Si and SiC). Increase in die area increases the thermal cycling capability of solder. For higher ΔT thermal cycle, solder under SiC die perform better than solder under Si die in terms of thermal cycling capability. When the die thickness become smaller than a threshold value of the thermal cycle regime, solder under Si die have better thermal cycling capability than solder under SiC die. Additionally a parametric study was undertaken for a SiC chip/substrate structure under high ΔT temperature cycling profile for solder layer geometric parameter (wetting angle, titling angle and thickness). From the parametric study which utilised design of experiments (DoE), a wavelet radial basis surrogate model was generated. A sensitivity analysis was performed on surrogate model in order to identify the most influencing parameter. From the sensitivity analysis, it was concluded that wetting angle and solder layer thickness of solder layer have significant impact on the thermal cycling capability of the solder layer.

Keywords: Surrogate models, Power electronic module, Sensitivity analysis, Finite element analysis

Nomenclature

$\Delta\varepsilon_{in}$	Accumulated equivalent inelastic strain during a stabilised cycle
V_j	Volume of one jth element
V_{tot}	Summation of volumes of all the elements within the volume
N_f	Fatigue life
α_i	Coefficient of thermal expansion of material *i*
v_i	Poisson ratio of material *i*
E_i	Young's modulus of material *i*
h_i	Thickness of material *i*
ΔT	Temperature change
L	Half the length of the chip
G_i	Shear modulus of material *i*
τ	Interfacial shear stress
γ	Interfacial shear strain
D_i	Flexural rigidity of material *i*
k, κ, λ, ξ	Characteristic constants

1. Introduction

Power electronic module (PEM) devices are often exposed to rather harsh operating conditions, these devices consist of different material layers, and each material has different coefficients of thermal expansion (CTE), which induce thermo-mechanical stresses in each layers under its operating conditions. Many failure mechanisms in PEM devices were widely reported in the literature [1]. In a power electronic module, the silicon chip is attached by die attach materials usually solder materials to package substrate material. Temperature fluctuations in the power electronic module device during its service time causes gradual increase of damage in solder joints and eventually this damage accumulation passed beyond a critical value will lead to electrical

failure of the PEM device. The package substrate is typically composed of ceramic isolated by copper layers. Silicon chips are gradually replaced by silicon carbide chips which can able to withstand a temperature up to 500° C [1]. However die attach materials such as solders can't endure a temperature of above 200° C. Lead free solders such as SnAg has the melting temperature of 221° C. These lead free solders can be used as die attach material for up to 80% of the melting temperature before creep strain effects cause failure in solders [2].

One of the objectives of thermo-mechanical analysis is to generate a stress versus strain responses in solder layer and predict its reliability for a specified operating condition. An accurate reliability estimation of solder joints depends on accurate modelling of the mechanical and microstructure characteristics of the particular solder layer. The solder layer is mechanically soft and often used in high homologous temperature; hence, the plasticity and creep causes mechanical deformations in solder layer. Creep is the redistribution of stresses and strain with time in solder under a constant load at elevated temperature. Creep damage of solder joint is a process of formation and growth of voids and cavities within the solder microstructure, become significant above a homologous temperature of 0.4 [3]. Homologous temperature is defined as T/T_m, where T_m is the melting temperature. Often the solder layer in power module applications are very thin and bonded to relatively rigid materials such as copper and silicon with intermetallic layer formed at the bonding interfaces often display brittle characteristics.

Power electronic devices for switching applications based on wide band gap materials such SiC and GaN offer better performance on operating voltage, switching speed and on resistance compared to Si material [4, 5]. This is due to wide gap material's higher breakdown electric field and higher thermal conductivity. Other significant device level advantages of SiC power devices compared to Si based power devices were listed on the book by Bai et al [6]. A study by Herold et al [7] on the power cycling capability of SiC diodes and Si diode for identical testing conditions was conducted. The study concluded that reliability of standard soldered SiC diode was three to four times lower in comparison with Si diode of similar rated current and voltage category. The influence of chip dimensions and material property on the thermal cycling capability of the Sn3.5Ag solder from finite element analysis perspective has not been analysed in the past

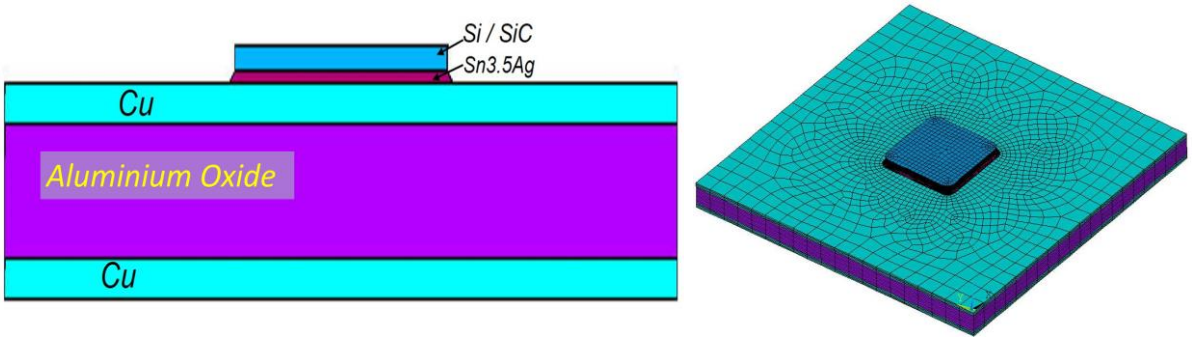
The motivation for this study arisen from the question of what is the trend to the thermal cycling lifetime capability of the solder layer

- If the chip thickness varies from a nominal base value such as ×0.333, ×0.666, and ×1.333
- If the chip area varies from a nominal base value such as ×0.125, ×0.25, ×0.5, and ×2
- What is the difference between thermal cycling capabilities of solder layer under die if the die material properties change (Si instead of SiC)?

That motivated to conduct passive thermal cycling of structure for chips with various materials (Si and SiC) and dimensions in order to investigate the thermal cycling capability of solder influenced by thermally induced stresses. Additionally how the wetting angle, layer thickness, and tilting angle influences the thermal performance of the solder layer was also investigated by utilising a surrogate modelling approach combined with sensitivity analysis.

2. Finite Element Analysis of Solder Interconnect in Power Module

In order to evaluate the impact of die thickness, area and material properties on the thermal cycling capabilities of Sn3.5Ag, a CREE manufactured Schotkky diode chip (CPW5-1200-2050B) [8] was chosen as a base chip. The length, width and thickness of the base die are respectively 4.9 mm, 4.9 mm, and 380 µm. The standard substrate thickness of the structure are extracted from Lutz et al [9]. Thickness of copper aluminium oxide, and solder are respectively 0.3mm, 1mm, and 0.1mm. The wetting angle of the solder was chosen as 33° based on national institute of standard (NIST) report [10].



The length and width of the substrate for all the simulation were chosen as 20.4mm. The elastic and thermal material properties of the materials used in this model were extracted from public domain [11] and the

temperature depended solder material properties are from Kim's thesis [12]. The material properties used in the numerical modelling are listed in Table 1. Top and bottom metallisation on the chip was ignored in the finite element modelling since they contribute very little in terms of stresses and inclusion of the metallisation in the finite element analysis will increase the complexity of the modelling and the solution process. To simulate the thermo mechanical loading condition on a soldered structure in Ansys FEA software [13] we generated the three dimensional finite element model as shown in Figure 1.

The Anand's viscoplastic model used in this study, was originally developed for high-temperature metal forming processes such as rolling, but it has been demonstrated for use in predicting the life of solder joints in electronic packaging. The Anand viscoplastic material properties of the solder layer were extracted from Wang's article [14 and 15] and they are listed in Table 2. The parts in the model associated with critical regions of interest have finer mesh in order to ensure accurate FEA results. In this study, FEA simulation in Ansys is a passive thermo mechanical analysis using the element SOLID185.

Table 1: Elastic and thermal material properties used in the FEA

Properties	Copper (Cu)	Aluminium Oxide (Al_2O_3)	Silicon (Si)	Silicon Carbide (SiC)	Solder (Sn3.5Ag)
Density (kg/cm^3)	8900	3985	2300	3210	7360
Coefficient of Thermal Expansion ($10^{-6}/K$)	16.9	5.8	3	4.3	21.
Young's Modulus (GPa)	117	380	162	501	$52708-61.74*T-0.0587*T^2$
Poisson Ratio	0.31	0.23	0.3	0.14	0.4

Table 2: Anand viscoplastic parameters of Sn3.5Ag

Anand Parameters	Sn3.5Ag
A (sec-1)	2.23 (10^4)
Q/R (° k)	8900
ξ	6
m	0.182
$\hat{s}$	73.81
n	0.018
h_0 (MPa)	3321.15
a	1.82
s_0 (MPa)	39.09

JEDEC standard [16] for temperature cycling is specifically for the solder interconnection testing on thermal chambers. Many studies on eutectic solder have shown that the dwell time beyond certain limit has a minimal effect on the Mean Time to Failure (MTTF). Additional dwell time will not produce additional damage beyond a limit or boundary. The faster ramp rate does impose more damage on solder joint than a slow ramp rate. According to Fan et al [17], it was concluded that the ramp time and dwell time have conflicting effects on solder joint reliability and the finite element results were also shown that the majority of damage occurs during the ramp period.

As stated by Zhai et al [18], the dwell time at high temperature is predicted to have a negligible contribution to the total inelastic strain energy density. Hence in this analysis ramp time and dwell time were taken as 3 and 15 minutes respectively based on the study by [18]. Maximum and minimum temperature sets are taken as [-25°C, 50°C], [-25°C, 150°C] for two ΔT regime. The structural boundary condition is as the three point freedom restraining boundary condition was imposed on the model.

Figure 2 is the FEA output for plastic strain on the thin layer (10 μm) of solder. In order to evalaute the MTTF of the solder layer, tradionally a predictive fatigue life model was utlised. The predictive fatigue life time models can be categorised based on stress, plastic strain, plastic and creep strain, energy, and damage accumulation [19]. For lead free solder with creep properties, we utlised inelastic strain based life prediction model. Previous studies have found that the low-cycle fatigue behaviour of solder alloys can be modelled by using the Coffin–Manson law [20].The Coffin-Manson fatigue life model one of the widely used model with the following equation was used in this study

$$\Delta\varepsilon_{in}\left(N_f\right)^k = C \tag{1}$$

where, k is fatigue ductility exponent and C is the fatigue ductility coefficient. To calculate the accumulated inelastic strain we used the volume weighted average (VWA) method which is widely reported in the literature.

$$\Delta\varepsilon_{in} = \frac{\sum_j \Delta\varepsilon_{in}^j V_j}{V_{total}} \tag{2}$$

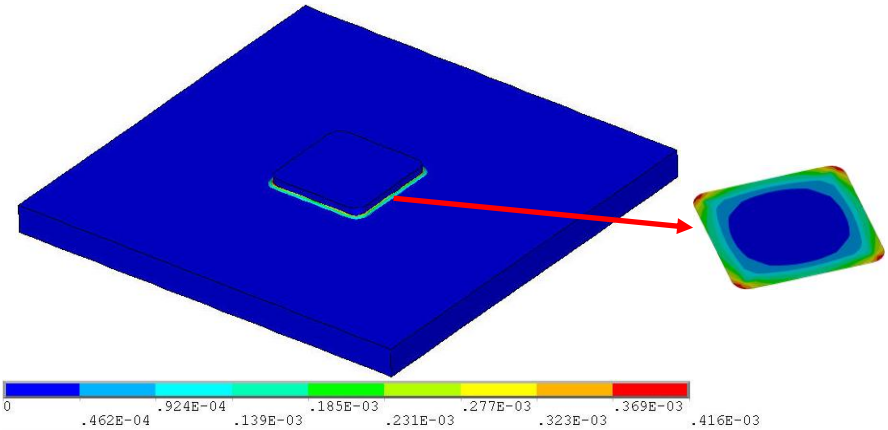


Figure 2: Accumulated plastic strain distribution in fourth cycle, on thin layer (10 microns thickness layer on the chip side) of solder

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where $\Delta\varepsilon_{in}^j$ is the accumulated inelastic strain of element j. The various values were proposed for C and k for equation (1) in literature based on the different type of solder on the model. In the article by Andersson et al [20] for Sn3.5Ag solder, the values of C and k as 3.921 and 0.6978 were assigned. In the study by Takahashi et al [21], for SnAg solder the Coffin Manson fatigue model parameters, C and k used as respectively 0.4 and 0.5. In this study, in order to predict the number of cycles to failure of the solder layer, the value of Coffin Manson parameters of C and k extracted from Andersson et al [20].

Accumulated inelastic strain was used in the Coffin-Manson based relation (1) to predict the cycles to failure. In the input from FEA simulation in ANSYS [13] during the temperature cycling test includes of the accumulated plastic strain (ANSYS command script output parameters for accumulated plastic strain is NL, EPEQ). A volume averaging technique described in equation (2) was then employed to calculate the accumulated inelastic strain for 10 micron thick layer of solder close to chip.

3. Finite Element Analysis Results.

Accumulated plastic strain of fourth cycle were evaluated for all the models and number of cycles to failure (N_f) of each models were evaluated as in the Figures 3 and 4. To assert the consistency in all the model simulations, substrate dimensions, solder layer thickness and wetting angle were kept constant.

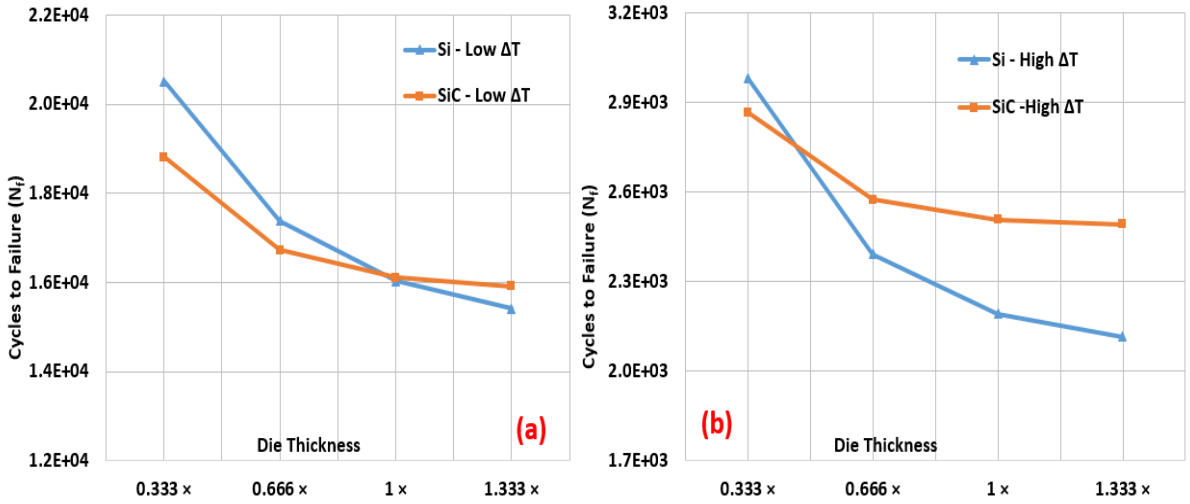

Figure 3: Cycles to failure of solder layer versus die thickness increment from original value (380 μm) for (a) low ΔT cycle and (b) high ΔT cycle

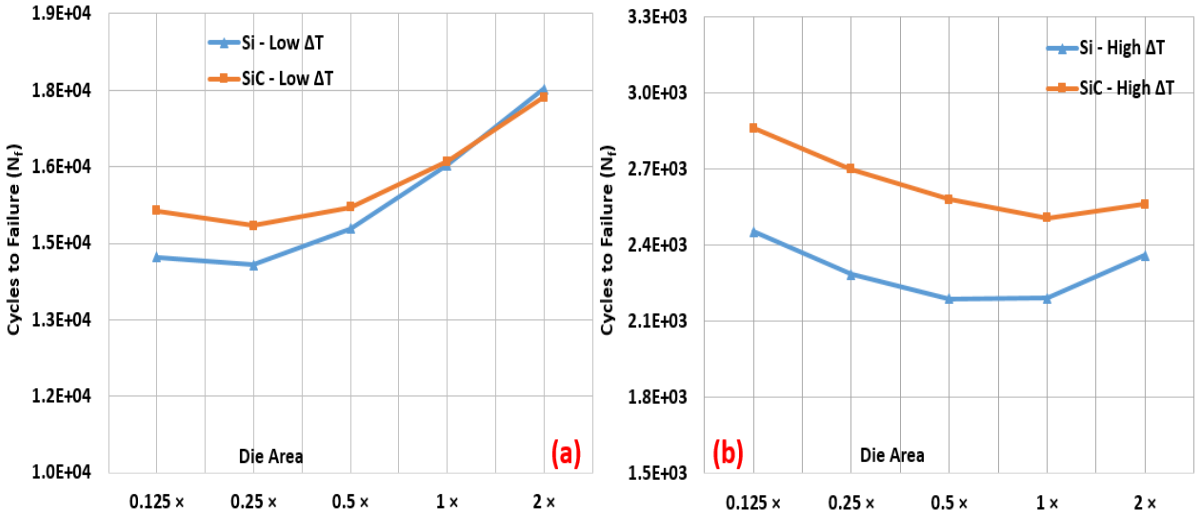

Figure 4: Cycles to failure of solder layer versus die area increment from original value (4.9 mm × 4.9 mm) for (a) low ΔT cycle and (b) high ΔT cycle

Based on the FE modelling results as in Figures 3 and 4 it can be concluded that,

- Decrease in die thickness by a factor from the nominal value resulting in increment of thermal cycling capability of solder layer for both material (Si and SiC) dies. But the solder layer thermal cycling capability (N_f) plot against die thickness by Si die is much more steeper than N_f plot versus die thickness by SiC die. This phenomena was observed for both ΔT cycles thermal loading. Eventually when the die thickness is below a small threshold value for particular ΔT cycle thermal loading, the solder layer under Si die has higher N_f than the N_f value of solder layer under SiC die for identical physical dimension.
- Increment in die area gradually increase the solder layer thermal cycling capability for both materials in low ΔT cycle thermal loading. In high ΔT cycle loading, solder layer thermal cycling capability plot against die area behaving like upward concave shape for both materials. Although N_f value of solder layer under SiC die has higher value than N_f value of solder under Si die, as area increases, the difference between N_f value of solder layer under Si die and N_f value of solder layer under SiC die narrows down and eventually after the die area value exceeds a particular threshold value, N_f value of solder Si die will become higher than the N_f value of solder layer under SiC die.
- Increase in ΔT of the thermal cycle increases the difference between the N_f value of solder under Si die and N_f value of solder under SiC die. For higher ΔT thermal cycle, solder under SiC die perform better than solder under Si die

Is the results (Figure 3 and 4) justifiable? Theoretically the governing equations represent the thermo-mechanical behaviour of the structure involving of, thermal expansion and subsequent mechanical deformation and hence stresses on the structure. The analytical assessment of the results was infeasible due to the nonlinear FE analysis. Simple straightforward approach was analytically evaluating local mismatch shear strain since shear strain caused by thermal expansion is more dominant than other stresses. Many theoretical models have been proposed for evaluating local mismatch shear stresses [22]. We utilised two of the theoretical models proposed by Suhir [23] and Jiang [24] for comparing the trends.

3.1. Analytical Evaluation of Average Shear Strain

The location dependent local interfacial shear stresses (τ) resulting from the local expansion mismatch between a tri-layer material structure as in the Figure 5 is defined as in Equation (3) [22, 23]

$$\tau_{Shear}^{Sukir}(x) = \frac{k(\alpha_{copper} - \alpha_{chip})\Delta T}{\lambda\, Cosh(kL)}\, Sinh(kx) \tag{3}$$

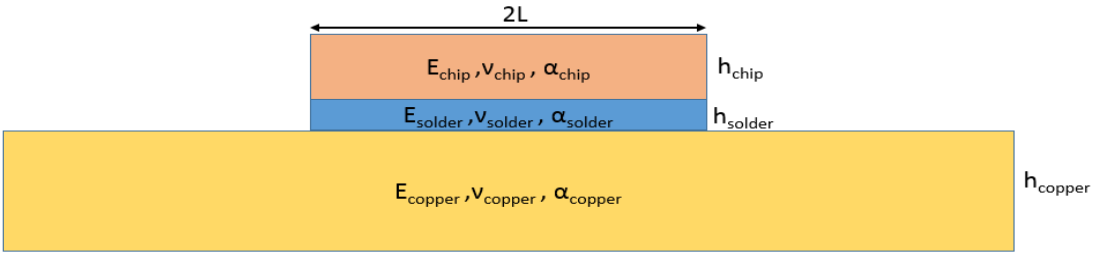

Figure 5: Tri-layer material schematic and properties

Where $k = \sqrt{\lambda / \kappa}$

$$\lambda = \left(\frac{(1-\upsilon_{chip})}{E_{chip} h_{chip}} + \frac{(1-\upsilon_{copper})}{E_{copper} h_{copper}} + \frac{(h_{chip} + h_{copper})^2}{4(D_{chip} + D_{copper})} \right) \tag{4}$$

$$D_{chip} = E_{chip} h_{chip}^3 / 12(1-\upsilon_{chip}^2) \tag{5}$$

$$\kappa = \left(\frac{2h_{chip}(1+\upsilon_{chip})}{3E_{chip}} + \frac{2h_{copper}(1+\upsilon_{copper})}{3E_{copper}} + \frac{4h_{solder}(1+\upsilon_{solder})}{3E_{solder}} \right) \tag{6}$$

Hence location dependent shear strain is defined along the interface as

$$\gamma_{shear}^{Sukir}(x) = \frac{\tau_{shear}^{Sukir}}{G_{solder}} = \frac{2(1-\upsilon_{solder})\tau_{shear}(x)}{E_{solder}} \tag{7}$$

Average shear strain on chip solder interface is evaluated by integrating the location dependent shear strain (Equation (7) along the interface as

$$\gamma_{Average\ shear}^{Sukir} = \frac{\int_0^L \gamma_{shear}^{Sukir}(x)dx}{L} = \frac{2(1-\upsilon_{solder})(\alpha_{copper} - \alpha_{chip})\Delta T}{E_{solder}\lambda L}\left[1 - \frac{1}{Cosh(kL)}\right] \tag{8}$$

Similarly, another analytical model developed by Jiang et al [34] for location dependent shear strain is defined as

$$\tau_{Shear}^{Jiang}(x) = \frac{G_{solder}\left(\left(1+\upsilon_{copper}\right)\alpha_{copper} - \left(1+\upsilon_{chip}\right)\alpha_{chip}\right)\Delta T}{\zeta . h_{solder}} e^{\zeta(x-L)} \tag{9}$$

Where $\zeta = 2\sqrt{\dfrac{G_{solder}\left(\dfrac{\left(1-\upsilon_{chip}\right)}{E_{chip}h_{chip}} + \dfrac{\left(1-\upsilon_{copper}\right)}{E_{copper}h_{copper}}\right)}{h_{solder}}}$

Average shear strain from Jiang model (equation (9)) is defined as

$$\gamma_{Average\ shear}^{Jiang} = \frac{\left(\left(1+\upsilon_{copper}\right)\alpha_{copper} - \left(1+\upsilon_{chip}\right)\alpha_{chip}\right)\Delta T}{4G_{solder}\left(\dfrac{\left(1-\upsilon_{chip}\right)}{E_{chip}h_{chip}} + \dfrac{\left(1-\upsilon_{copper}\right)}{E_{copper}h_{copper}}\right)L}\left[1 - \frac{1}{e^{\zeta L}}\right] \tag{10}$$

Since $\gamma_{Averageshear}^{Sukir} \propto \left(\alpha_{copper} - \alpha_{Chip}\right)$, and $\gamma_{Averageshear}^{Jiang} \propto \left(\left(1+\upsilon_{copper}\right)\alpha_{copper} - \left(1+\upsilon_{chip}\right)\alpha_{chip}\right)$, hence Si chip introduces higher local interfacial shear stress in comparison with SiC chip for identical chip physical dimensions because of the, CTE of Si is lower than the CTE of SiC. Similarly $\gamma_{Averageshear}^{Sukir}, \gamma_{Averageshear}^{Jiang} \propto \frac{1}{L}$ implies that, if the length of the chip increases then the average shear strain decreases and consequently higher thermal cycling capability. Additionally $\gamma_{Averageshear}^{Sukir} \propto \frac{1}{\lambda}$ and λ depend on h_{chip}, implies that, if the chip thickness increase, then the average shear strain increases in a nonlinear format and hence decrease in thermal cycling capability of solder. These trends agree well with the trends of finite element results (Figures 3 and 4).

4. Parametric Study for Sensitivity Analysis

Does the solder geometry have any significant influence on the thermal cycling capability of solder? Hence we decided to undertake a parametric study to identify the effect of geometrical parameters on the overall performance of the solder layer for one particular chip model. A finite element analysis parametric study has been undertaken in order to analyse the influence of the geometrical parameters of solder layer, effect on solder layer temperature cycling capability. Three geometric design parameters of the solder layer were identified such as wetting angle, tilting angle and solder layer thickness as in the Figure 6. A medium size SiC die (CPM2-1200-0025B) was chosen for the parametric study. The length, width and thickness of the die are respectively 6.44 mm, 4.04mm and 180 μm. The range of wetting angle was chosen as {33° ± 20%}. Similarly solder layer thickness range was chosen as {0.1 mm ± 20%}. Due to manufacturing uncertainties, die tilting can occur. Previous study indicated that tilting angle has some influence on the reliability of the solder. Hence, in this study, we included tilting angle as one of the geometrical parameter. The tilting angle for the particular model is θ,

$$\theta = Sin^{-1}\left(\frac{\text{Solder Thickness Difference between Left and Right}}{\text{Chip Length}}\right)$$

Hence maximum tilting angle was chosen as 0.5° in order to avoid the meshing difficulties in sharp pointed corners. The sharp corners are the sources of numerical singularities and consequently FEA predicts inaccurate results at these locations even with very fine mesh. The range of tilting angle was between 0° and 0.5°

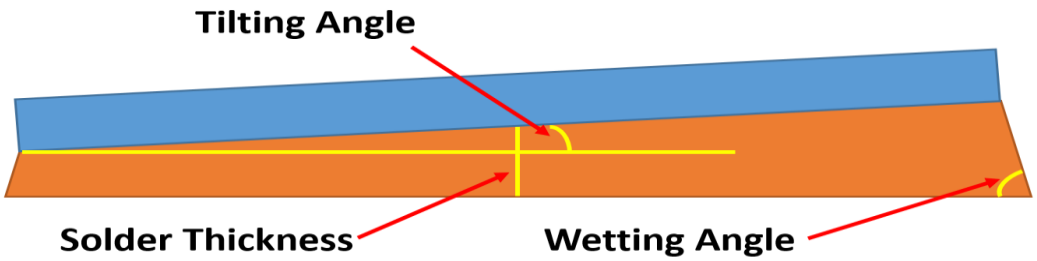

Figure 6: Schematic of wetting angle, tilting angle and solder thickness of the solder layer

4.1. Design of Experiments

Three basic principles of design of experiment (DoE) are randomization, replication and blocking [25]. Randomisation is the allocation DoE points by random. The replication is the process of repeating of each factor combination. Blocking is a process of removing the effects of irrelevant variation and improves the efficiency of experimental design. Three design variables and their design space range are in the Table 3. The second column of the Table 3 specifies the value of the nominal (or initial) design of the solder layer structure while third column of the table provides details on some possible design variations of the model assembly parameters that are selected for this study. The fourth column of the table is the normalised design parameter variations.

Table 3: Design parameters of the model

Solder Model Design Variables	Nominal Values	Un-scaled limits	Scaled Limits/dimensionless
Solder Layer Thickness(mm)	0.1	0.08 to 0.12	-1 to 1
Wetting Angle (°)	33	39.6 to 26.4	-1 to 1
Tilting Angle (°)	0.25	0 to 0.5	-1 to 1

Table 4: DoE points and predicted solder layer accumulated plastic strain from FEA

DoE Points No	Wetting Angle (°)		Tilting Angle (°)		Solder Layer Thickness (mm)		Number of Cycles to Failure
	Actual	Scaled	Actual	Scaled	Actual	Scaled	
1	26.4	-1	0	-1	0.08	-1	2562.8
2	39.6	1	0	-1	0.08	-1	2659.3
3	26.4	-1	0.5	1	0.08	-1	2446.6
4	39.6	1	0.5	1	0.08	-1	2619.3
5	26.4	-1	0	-1	0.12	1	2696.0
6	39.6	1	0	-1	0.12	1	2789.6
7	26.4	-1	0.5	1	0.12	1	2658.0
8	39.6	1	0.5	1	0.12	1	2795.4
9	33	0	0.25	0	0.10	0	2692.0
10	33.82	0.12	0.389	0.55	0.12	0.93	2742.1
11	38.76	0.87	0.130	-0.48	0.10	-0.13	2737.5
12	28.03	-0.75	0.057	-0.77	0.10	0.08	2658.1
13	30.69	-0.35	0.358	0.43	0.09	-0.63	2629.9

By altering the value of these design variables within the selected range, various design modification of the solder model can be generated. A set of values for the specified design variables that specify a particular design is referred as a design point. Thirteen DoE sampling points include of eight full factorial/Taguchi design points, one central point, and four Latin hypercube points Table 3 lists the key design parameters of interest for specific characteristic performances. Increasing more DoE points increases the accuracy but it also increases the effort and computational cost in FEA model simulation. Hence we limited design samples to 13. The first step in the surrogate modelling approach was to obtain performance characteristic data through DoE by evaluation of limited number of design FEA simulations. From the design point of view, any design modification of the solder model is restricted to changing the Solder layer thickness (h_{Solder}), wetting angle (θ_W), and the tilting angle (θ_T).

The DoE points are listed in Table 4. The table also shows the dimensionless scaled values of design variables over the range -1 to 1 used in the following generation of the surrogate models. The last column list the finite element analysis predictions for thermal cycling capability values of solder. The thermal cycling capability values were derived from the equation (1) by utilising the accumulated average plastic strain of 10 µm thick solder layer.

4.2 Wavelet Radial Basis Function (WRBF) Surrogate Model

There are many surrogate models exists in the literature such as radial basis function (RBF), Kriging, Neural network, and so on. Kriging surrogate model can estimate the error bound of a prediction, but estimating Kriging basis function coefficients requires an optimisation task which is a drawback. Wavelet is a localised function. A wavelet RBF (WRBF) neural network surrogate model with *n* neurons has been used to interpolate the multidimensional *n* sample data with zero error [26]. Additionally, WRBF is relatively easy to implement in contrast to other more complex surrogate models such as Kriging. Hence we employed WRBF in this study. The interpolation is a method of predicting the new data points by forming of weighted average of the values at known surrounding points. The WRBF surrogate model is defined as follows

$$\varepsilon(X) = a_0 + a_1 h_{Solder} + a_2 \theta_W + a_3 \theta_T + \sum_{i=1}^{13} \frac{b_i}{|\psi(0)|} \psi\left(A\|X - X_i\|\right) \tag{11}$$

where Ψ is the wavelet function, A is the constant value chosen as 3. The vector X_i consists of three component, $X_i = \{(h_{Solder})_i, (\theta_W)_i, (\theta_T)_i\}$. Wavelet functions are widely applied in many fields because of their unique mathematical properties. The definition and the properties of the wavelet function are described by Charles [27]. Many wavelet functions are defined in the literature, in this study we utilised one of the widely known wavelets namely the Ricker wavelets or Mexican hat wavelet for its symmetric property. Definition of Mexican hat wavelet is as follows.

$$\psi(X) = \frac{2}{\sqrt{3}\pi^{1/4}}\left(1 - X^2\right)e^{-X^2/2} \tag{12}$$

The coefficients of the surrogate model (Equation (11)) for number of cycles to failure (N_f) are detailed in Table 5

Table 5: Coefficients for WRBF surrogate models

Solder Layer model DoE scaled value			Wavelet RBF Coefficients
$(\theta_W)_i$	$(\theta_T)_i$	$(h_{Solder})_i$	b_i
-1	-1	-1	9.02
1	-1	-1	-15.7
-1	1	-1	-58.42
1	1	-1	-5.17
-1	-1	1	-7.68
1	-1	1	-34.55
-1	1	1	0.83
1	1	1	5.81
0	0	0	-37.13
0.12	0.55	0.93	15.43
0.87	-0.48	-0.13	35.83
-0.75	-0.77	0.08	18.91
-0.35	0.43	-0.63	72.82

The other coefficient values such as a_0, a_1, a_2, a_3 in equation (11) are respectively 2670.11, 64.78, -23.91, and 79.88.

4.3. Sensitivity Analysis

Sensitivity analysis (SA) is a process of identifying the design (independent) variables that most contribute to the variability of the performance (dependent) variable. SA attempts to determine the change in the performance variable that results from modest change in the design variable values. Various SA approaches has been proposed in the literature [28]. Simplest approach to SA is often implemented using sampling the design space of one variable and keeping the other design variables at nominal values. This process was also named as local

sensitivity analysis. Local SA evaluates changes in the performance function with respect to the variations in a single design variable. The design parameter are typically changed one at a time and the effect on this individual design variable perturbation on the performance variable is calculated. That's for design each parameter, generate multiple values at the design space. Evaluate the surrogate model at each combination of parameter values to plot the performance function for samples to analyse the trend. In this study a uniform sampling was performed on each design space. The in-house software ROMARA [29] was utilised in this study. The objective of SA was to analyse the most influencing variables of the cycles to failure of solder layer (surrogate model (equation (11)) within the three design variables such as solder layer thickness, wetting angle and tilting angle. The variance in cycles to failure plots for each design variables when other design variables are at nominal value are in Figures 8 and 9. The x-axis units in Figures 8 and 9 are in normalised range [-1, 1].

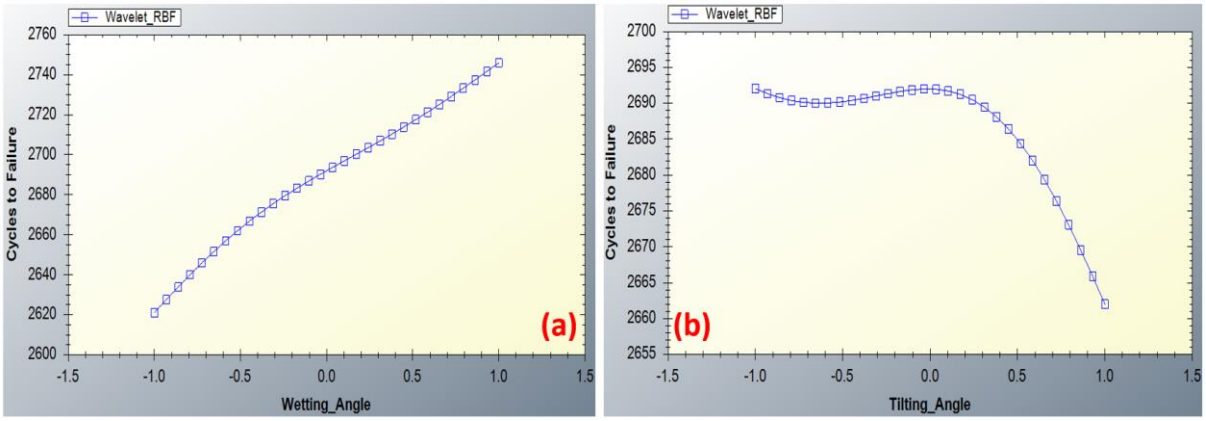

Fig 8: Cycles to failure plot versus (a) wetting angle of solder layer and (b) tilting angle of solder layer when other variables are at their nominal values.

The percentage variance in cycles to failure is less than 5% for all three variables. Nevertheless, wetting angle of solder layer has significant influence in the solder layer temperature cycling capabilities. Increment in wetting angle results in increment in cycles to failure. Second influencing factor is solder layer thickness, increase in solder layer thickness will increase the thermal cycling capability of the solder layer, but increase in tilting angle decreases the cycling capability of the solder layer. One of the interesting factor is the tilting angle, increment of tilting angle increases the thermal cycling capability of the solder layer initially and then the cycling capability decreases.

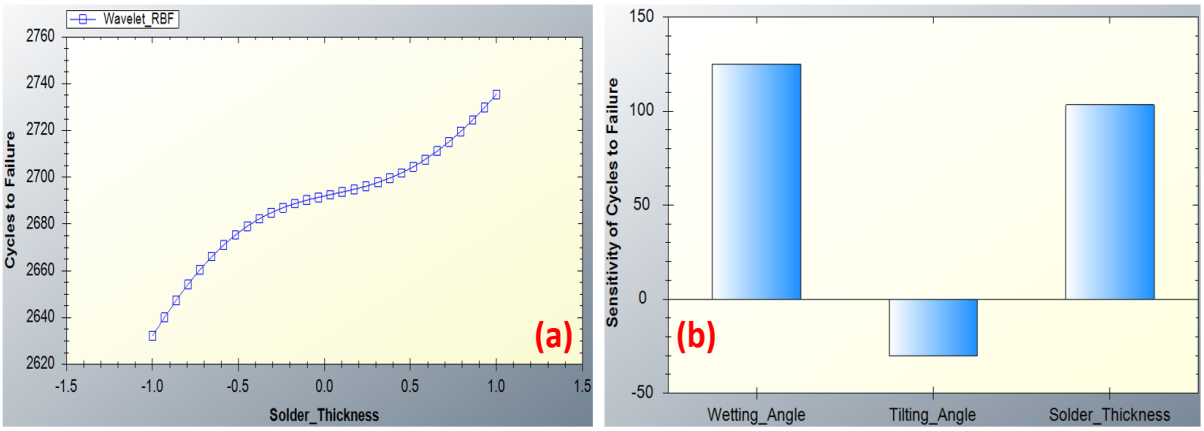

Fig 9: (a) Cycles to failure plot versus layer thickness of solder layer when other variables are at their nominal values (b) sensitivity plot of cycles to failure of solder layer for each design variables

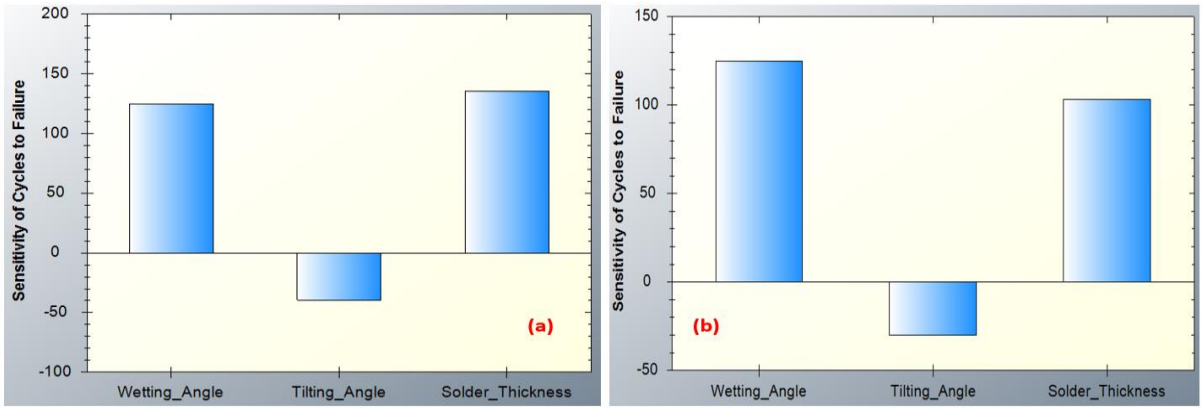

Fig 10: (a) Sensitivity plot of cycles to failure of solder layer for each design variables in Kriging surrogate model, (b) Sensitivity plot of cycles to failure of solder layer for each design variables in WRBF surrogate model,

Naturally one of the question arises, do these observations (Figure 9(b)) depend on the surrogate model chosen? Hence we utilised another surrogate model namely Kriging model [30] in order to observe similar trend. Sensitivity plot of Kriging model for the data in Table 4 as in Figure 10 (a). From Figure 10 we can conclude that wetting angle and solder thickness have positive correlation on cycles to failure and tilting angle has negative correlation on cycles to failure for both surrogate models, but Kriging surrogate model generated slightly higher sensitivity value of solder thickness than wetting angle sensitivity value

4.4 Sobol's Sensitivity Analysis

Sobol's SA is a decomposing process of the performance variable variance into summation of variances of the design variables. It is another sensitivity analysis approach widely cited in the literature [31]. It estimate the influence of each design variable and their interactions to the performance variable variance. It can handle nonlinear and non-monotonic performance variable [32]. A *p* dimensional function can be defined as

$Y= f(X) = f(X_1, X_2 \ldots X_p)$

Where Y is the model performance variable and X $(X_1, X_2 \ldots X_p)$ is the design variable set, Sobol's decomposition of the performance variable is defined as

$$f\left(X_1, X_2, \cdots, X_p\right) = f_0 + \sum_{i=1}^{p} f_i\left(X_i\right) + \sum_{i=1}^{p}\sum_{j=1}^{p} f\left(X_i, X_j\right) + \cdots \tag{13}$$

Where f_{ij} is partial derivative of f with respect to X_i and X_j. f_0 is the f value for design variables are at their nominal values. If the design variables are independent, then total variance can be defined as

$$V(Y) = \int_{\Omega_P} f^2(X)dx - f_0^2 \tag{14}$$

Where Ω_p represents the p dimensional domain. The first order variance is defined as

$$V_i = \int_{\Omega_i} f_i^2\left(X_i\right)dX_i \tag{15}$$

First order Sobol index (FOSI) is defined as

$$S_I = \frac{V_i}{V} \tag{16}$$

The FOSI is a measure of each design variable variance contribution to performance variable variance. In other word FOSI is the variance of the conditional expectation of the performance variable for given design variable, normalised by the total variance [33]. In this study FOSI were evaluated to the surrogate model (equation (11)) representing the solder layer cycles to failure for each design variables (solder thickness, wetting angle, and tilting angle) by utilising an open source MatLab code namely Global Sensitivity Analysis Tool (GSAT) [34] and the Sobol's first order sensitivity index of each design variables are on the Table 6

Table 6: Sobol's index of the solder layer design variables

Variable	First order Sobol's index
Wetting Angle	0.461
Tilting Angle	0.045
Solder Thickness	0.455

It is clear from the Table 6 that wetting angle has higher influence on the solder layer cycling capability since Sobol's index value of solder thickness is maximum. Next influencing factor is solder layer thickness. Tilting angle play little part on the cycling capability of the solder layer. This trend agrees well with local sensitivity analysis in Figure 9(b).

5. Conclusions

This paper has discussed a finite element analysis of solder layer interconnect structure in power electronic module assembly. The objective of the finite element modelling was to analyse the impact of die material properties and dimensions on the effect of the viscoplastic strain distribution of Sn3.5Ag solder layer interconnect and the subsequent estimation of thermal cycling capability (cycles to failure) of the solder layer. Two thermal cycling profiles were utilised in finite element analysis tool. A commercially available SiC Schottkky diode die was used as the nominal base die. Anand viscoplastic model was also utilised for the solder creep strain estimation. Average accumulated viscoplastic strain on thin layer with 10 microns thickness of solder layer was estimated by volume averaging technique and this accumulated strain value was utilised to estimate the number of cycles to failure of the solder layer under the applied thermal load.

Based on thermal cycling capability data from FEA, it was concluded that,

- For the both material (Si and SiC) dies, there was a negative correlation between die thickness and the solder layer thermal cycling capability (Lifetime*)*. This trend was also observed in both ΔT temperature cycling profiles. Hence thinner die results in higher lifetime of solder. Generally solder under SiC perform better in terms of lifetime in comparison with solder under Si die, but the die thickness exceeds a threshold value, solder under Si die has higher lifetime in comparison with the lifetime value of solder under Si die.
- There was a positive correlation between the die area and thermal cycling capability of solder if the die area exceeds a threshold value. This trend was observed for both materials (Si and SiC). Although the lifetime value of solder under SiC die is higher than the lifetime value of solder under Si die but the gap between lifetimes is narrowing as area increases.
- For higher ΔT thermal cycle, solder under SiC die perform better than solder under Si die in terms of lifetime.

Additionally a parametric study which includes of computational analysis framework integrated with surrogate modelling and sensitivity analysis was undertaken. In order to analyse the most influencing design variable of the solder layer geometry, the parametric analysis has been undertaken for a medium size SiC chip under high temperature cycling profile. Three design variables such as solder layer thickness, wetting angle, and tilting angle were used in the parametric analysis. Fast design evaluation surrogate model based on results from thermal-mechanical finite element analysis and Design of Experiments methods was developed using Wavelet radial basis functions. The surrogate modelling approach uses prediction data of thermal cycling capability of the solder layer. These surrogate models was utilised to predict the fatigue damage in solder layer in power electronic modules as a die attach material. From the parametric analysis, it was concluded that

- Wetting angle and solder layer thickness influence positively and these influences were significant in the thermal cycling capability of solder layer.
- Tilting angle have negative impact on the thermal cycling capability of the solder layer. This impact is very small, this could be due to small range of tilting angle range in this study.

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