Adiabatic DC-AC Power Converter with 99% Efficiency

[Interleaved, Folding, Interpolating, Dual-path Adiabatic Autotransformer Power Converter]

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Abstract

This paper describes a novel approach to building a high efficiency and dimensionally compact power converter / inverter. A prototype was built for the Google / IEEE Little Box competition. The converter takes a 400-450 V DC input and creates a single-phase 230V AC output. It is capable of supplying 2kW continuously to a load. The design is based on a multi-winding DC-DC active transformer operating at around 500 kHz. The AC output sinewave is synthesized by switching between the DC tap levels produced by the active transformer. The transformer MOSFETs operate under ZVS and have an adiabatic gate driver. Early tests on the prototype demonstrate a high fidelity sinewave output and very high efficiency (better than 99%).

1. Introduction

Google and the IEEE organized a competition called the “Little Box Challenge”: They offered a million dollar prize to whoever could build the world’s smallest 2kW inverter. The converter described here was a finalist in that competition [1]. It is under half the cubic-volume of the final prize winner [2]. It is an ambitious and innovative design, which is centered on two adiabatically switched high frequency transformers in a multi-level configuration, followed by a low frequency AC waveform synthesis stage. This is similar to the multi-level converters found in large-scale high voltage drives and MMC HVDC systems [3]. By adiabatically switching the main transformer stack, and thus avoiding switching losses, the efficiency can be very high [4] [5]. The low losses result in little need for heatsinking, so the converter may be physically very compact.

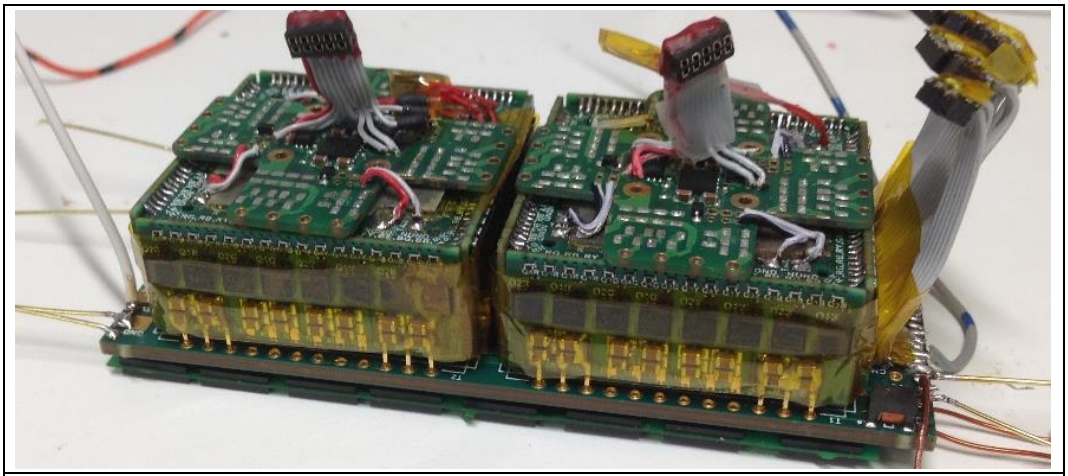

Fig. 1 The core of the system: Showing the DC-DC Active Transformers, the MUX base-board and the smoothing capacitor bank PCB (underside).

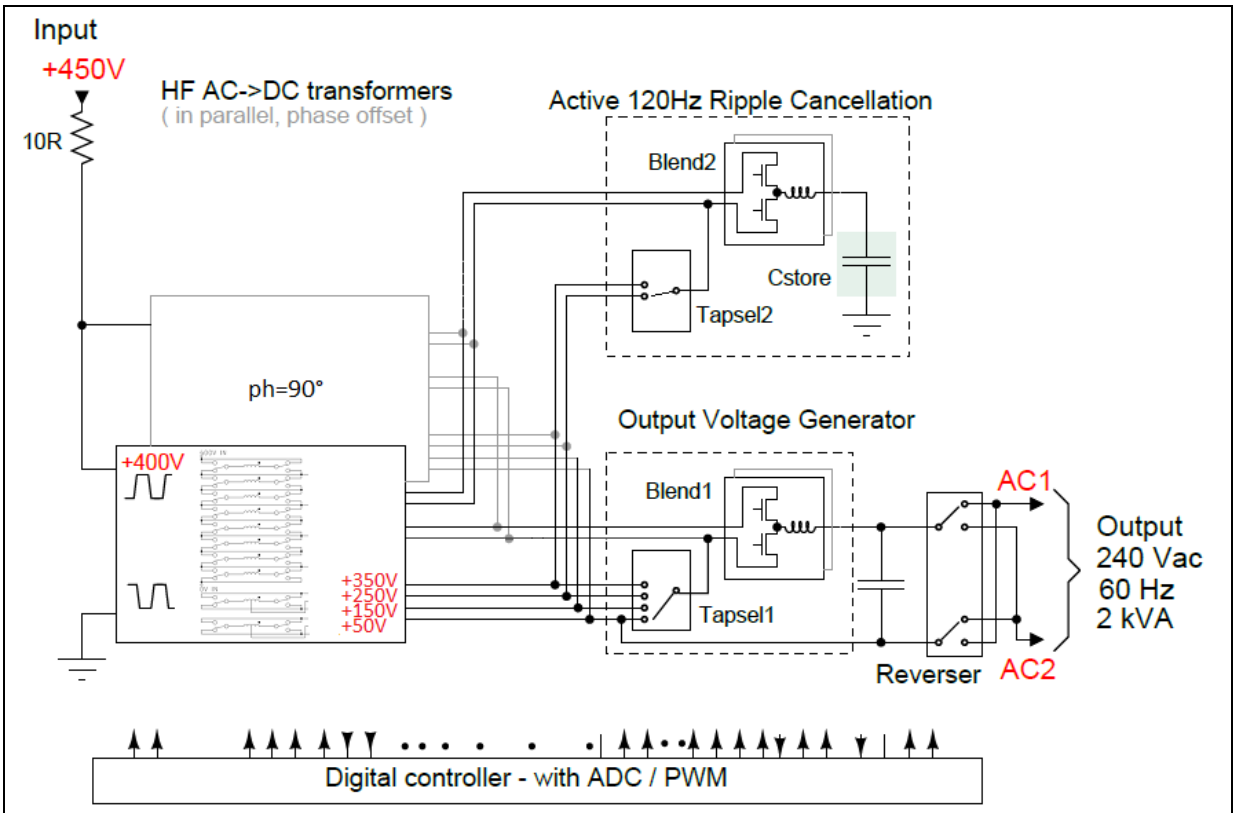

Fig. 2 Overall architecture showing the main current paths and ripple cancellation circuit.

The converter architecture comprises the following sub-systems:

1. Two adiabatically switched transformers that generate a series of DC voltage levels.
2. A digitally controlled binary-tree tap-selector that creates a repeating half-sine waveform by switching between these DC voltage levels in a series of small steps.
3. A pulse-width-modulated (PWM) blender circuit to smooth between these steps.
4. A reverser circuit to flip every-other positive-half-sine, making it an AC output.
5. An active ripple cancellation circuit, that uses an auxiliary output phase internal to the converter to deeply charge and discharge an energy storage capacitor, such that the input DC current remains constant with varying AC output current.

There is a digital control circuit that coordinates the operation and timing of these various sub-systems. It also monitors the performance of the converter. A PC software GUI application was created to configure and optimise various control parameters.

2. System Design

2.1 DC-DC Active Transformer

Our approach uses two identical auto-transformers driven 90° out of phase with each other (*see Fig. 1 and Fig. 2*). Both transformers contribute to the power conversion, with sufficient on-time overlap to ensure that at least one of the transformers provides a continuous conduction path from input to output at any given time. Each transformer is composed of a number of windings that are electrically isolated from one another, but magnetically coupled. The transformers are configured with 8 main windings and two isolated centre-tapped auxiliary windings. The former make up the main transformer voltage stack, whilst the latter provide floating supplies for finer adjustment of the output voltage and storage capacitance (*see Fig.3*).

Low voltage MOSFETs are used for the main power switching, as each winding is switched at a far lower voltage than the input or output voltage, bringing further advantages of size reduction and lower on-state resistance.

Alternating excitation voltages are applied to the transformers windings at high frequency by MOSFETs in a stacked H-bridge arrangement. A magnetisation current flows one way and then the other, as this switching is performed. Each winding is switched in perfect synchronisation with every other winding. This maintains a constant voltage between neighbouring turns, which significantly reduces capacitive charging currents. The relative voltage across each winding (end-to-end) is strongly related to every other winding by magnetic coupling.

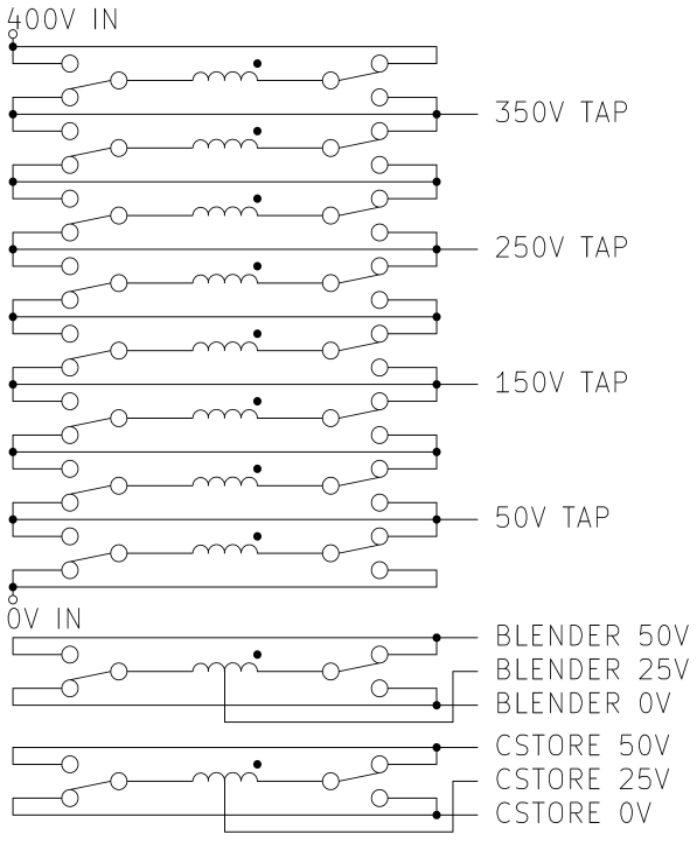

Fig. 3 The Active dc-dc transformer.

The polarity switching of the transformer windings is performed adiabatically. That is, when all of the switches in the H-bridges are turned off, the voltage across each winding is free to slew due to the transformer magnetisation current charging and discharging the output capacitances of the 'off-state' MOSFETs. In this way, the output capacitance of the power switching devices is used to obtain Zero Voltage Switching (ZVS). Once the voltage across the winding has completely reversed, the alternate pair of MOSFETs at each level are turned on. ZVS occurs at both turn-on and turn-off.

The effect of the low voltage multi-winding configuration, when combined with the slow linearly slewing adiabatic switching, means that the dV/dt across each winding is very low indeed, at least in comparison to what could be practically achieved with a hard-switched two-level inverter. This results in much lower generated EMI than from conventional topologies.

2.2 Output Waveform Synthesis

Output waveform shaping consists of a coarse/fine approach, with one of the main taps being selected using a tree structure of MOSFETs to give a coarse voltage (in nominal 100V steps), whilst the floating supply is pulse width modulated and added to or subtracted from this coarse voltage by a blender circuit. The fine adjustment winding is centre-tapped, providing floating-supplies of nominally 25V and 50V. This circuit topology enables the blender PWM to be performed at much lower voltages than would be possible in a normal hard-switched 2-level converter. This allows the use of low voltage MOSFETs with inherently lower switching losses.

A final 'reverser' H-bridge flips the half-sine output from the blender to either positive or negative polarity, to give the positive and negative swings in the full AC waveform. These transistors do need to be rated at the full maximum output voltage swing, but are only switched twice every full AC cycle, so the switching losses are negligible. As such, these transistors can be selected for lowest on-state losses and many can be connected in parallel.

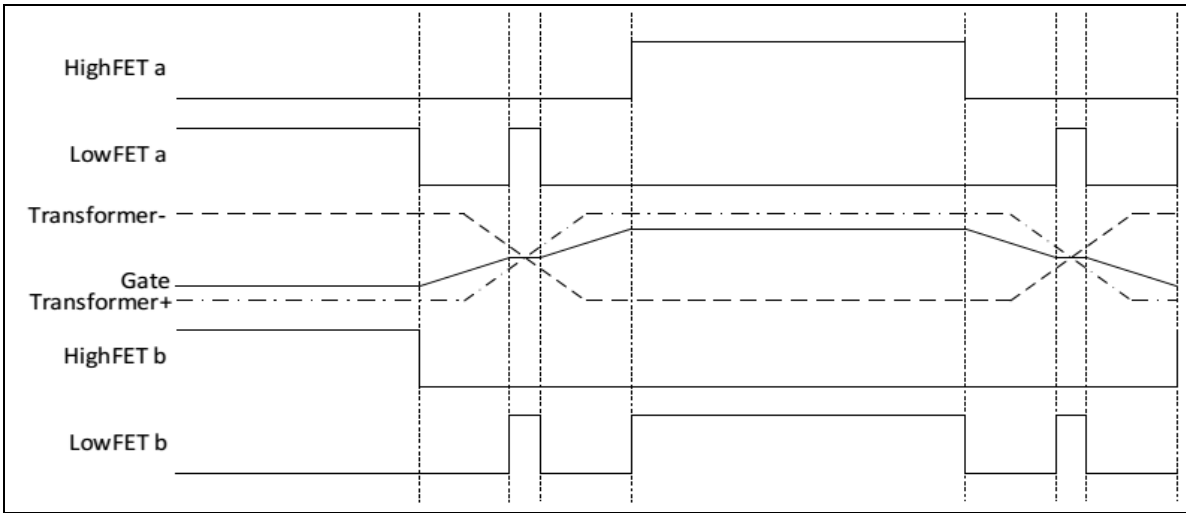

Fig. 4 Gate drive timing waveforms for adiabatic switching.

2.3 Gate Drives

A small gate drive isolating transformer is located in the centre of each main power transformer. It is used to drive the plethora of H-bridge MOSFET gates in a perfectly time-aligned manner for synchronized switching. There is one secondary winding per MOSFET. The primary side is driven by a single H-bridge low voltage driver. This is controlled by an FPGA, as are all other timings in the circuit. By using directly connected transformer windings and a unique switching strategy (*shown in Fig. 4*) the gate drive charge from the MOSFETs can be recovered back into the gate drive power supply, thereby reducing the gate driver losses. The clamping pulse in the middle of the drive period allows for more precise timing adjustment and low impedance during the main dV/dt event.

2.4 Active Ripple Compensation

The ripple compensation circuit works by deep charging and discharging a capacitor bank in response to the varying AC output current, such that the DC input current remains constant. This is achieved with an auxiliary converter phase that is connected internally to actively drive current in and out of the capacitor bank. It uses the main transformer stack voltage levels with an auxiliary binary tree MUX and blender stages to achieve this.

By actively moving the top DC connection on the capacitor bank through successive tap levels on the main power transformers, the voltage across the capacitors is forced to change in a controlled manner. The current that flows into or out of the capacitor bank is directly proportional to the rate of change of this voltage. However, the current that appears at the DC supply is not the same as the current through the capacitor bank: There is an 'auto-transformer' effect that means the current flowing through the capacitor bank needs to be proportionately greater as the auxiliary tap selector steps down through successive taps. Also the actual capacitance of the ceramic capacitors varies significantly with voltage. These effects are compensated for by a non-linear control algorithm.

In this design, the voltage across a 150µF capacitor bank is varied from 400V down to 200V, which gives a theoretical energy storage capacity in the reservoir of,

$$Energy\ stored = \tfrac{1}{2}C\mathrm{V}^2 = 150 \times 10^{-6}\,(400^2 - 200^2)/\,2 = 9\,Joules$$

$$Equivalent\ DC\ Bus\ Capacitance = 2E/\mathrm{V}^2 = 2 \times 9/(400^2 - 388^2) = 1.90 \times 10^{-3}\ \mu F$$

This is equivalent to a 1,900µF capacitor attached across the DC input with 3% ripple voltage present. Yet through the use of the active compensation mechanism, the 150µF capacitor in this design is sufficient to smooth the DC input voltage and current under full load conditions,

with the capability to give much better than 3% ripple. There is little to be gained from dropping lower than 200V, as the capacitor has already given up 75% of its energy. Clearly there is a size and cost advantage achieved in reducing this capacitance by more than a factor of ten.

2.5 Digital Control

The system is controlled by an FPGA, running various PWM timing blocks. The AC output is generated by stepping through a sinewave look-up table that controls the power routing in the output MUX stage and PWM blender. A compensation feedback control algorithm accounts for variations in output load and DC input voltage.

A software application has been developed to configure the FPGA controller remotely from a laptop PC, allowing choices in the operating frequency and timing parameters of the active transformer and the gate driver to be optimized for low loss operation.

3. Prototype Development

The transformers were manufactured to a very specific design and to exacting specifications. In order to keep any leakage inductance to a minimum, each winding is made up of multiple fine insulated wires, one from each winding set, and these are twisted together to form bundles. In this way, good high frequency magnetic coupling is achieved. A high frequency ferrite core is used with carefully engineered air gaps. The power switching MOSFETs are an integral part of the main transformer assembly in order to reduce stray inductance. Also the gate drive and floating power supply transformer sits inside the main power transformer to save space. This is all packaged together to form a single DC-DC Active Transformer assembly (*Fig. 5*).

Two active transformers are shown mounted on the MUX base-board in *Fig. 1*, with the ceramic energy storage capacitor PCB mounted underneath, showing the compact nature of the design. The FPGA control board normally sits on top of this assembly (not shown).

Fig. 5a Power windings with central gate drive transformer (perpendicular magnetic fields).

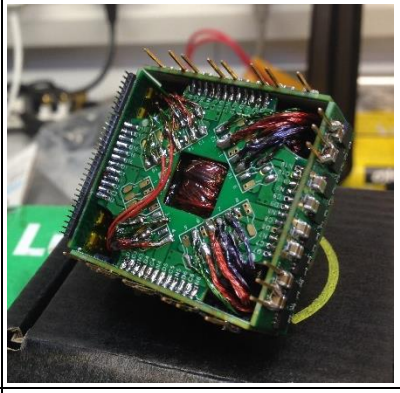

Fig. 5b Power winding PCB termination and H-bridge MOSFETs around the outside.

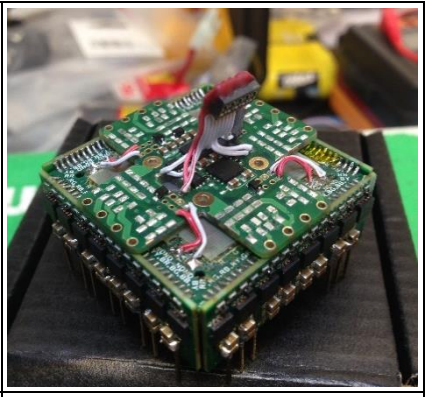

Fig. 5c Gate driver PCB, with gate winding termination PCB beneath.

The topology allows for much lower voltage rated MOSFETs to be predominantly used, giving gains in terms of component size and on-state resistance. High frequency PWM in the low voltage blender is used to shape the output voltage between steps, so a small LC filter is all that is required on the AC output to reduce conducted EMI emissions to acceptable levels. The high overall efficiency of the converter allows for the dense packing of components due to low heat dissipation, which is in the region of 16W at 2kVA. The whole inverter is enclosed in a copper housing. This spreads any local hot spots on the surface whilst affording excellent EMC shielding. The overall volume is 5 cubic inches, resulting in a power density of 400 W/cu-in.

4. Test Results

Tests were carried out on each part of the system to prove functionality and to check power losses at each stage through the converter. The results are summarized in this section.

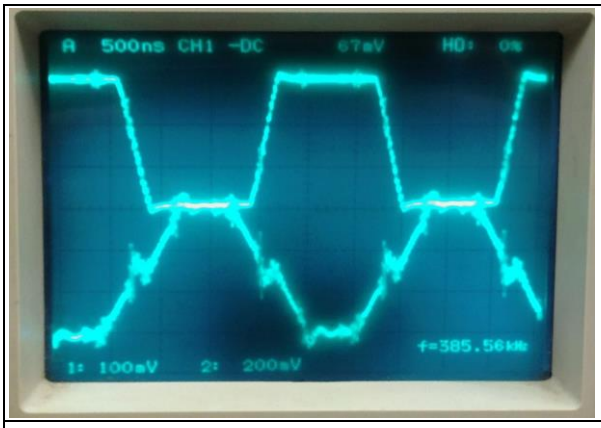

Fig. 6a Power switching waveform (top), and gate drive waveform (bottom trace).

Fig. 6b Stepped half-sine output waveform from binary-tree MUX (prior to blender and reverser).

The waveforms for the active transformer are shown in *Fig. 6a*. The upper trace shows the switched voltage across one power winding. The switching frequency is 385 kHz. The slow edges in the voltage waveform arise as a result of the adiabatic operation, where the transformer magnetisation current charges the MOSFET output capacitance. The MOSFET gate voltage is shown in the lower trace. It can be seen that there is a momentary shelf mid-way through the gate voltage ramp, where a clamp is applied across the gate winding primary to recirculate the magnetization current for a short time. The purpose of this is to adjust the timing of the gate voltage in relation to the power waveform, in order to achieve optimum switch transitions for lowest losses.

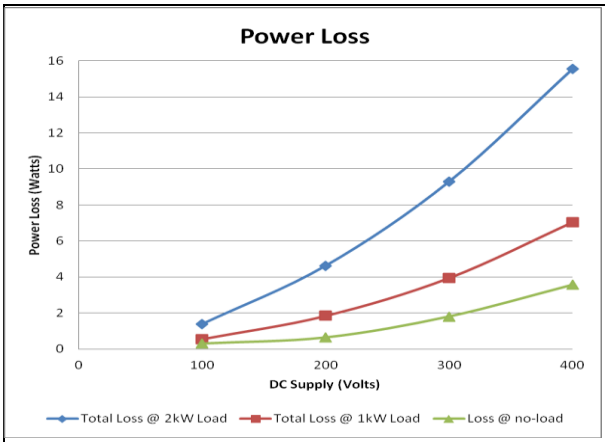

Fig. 7a Power loss at various load conditions.

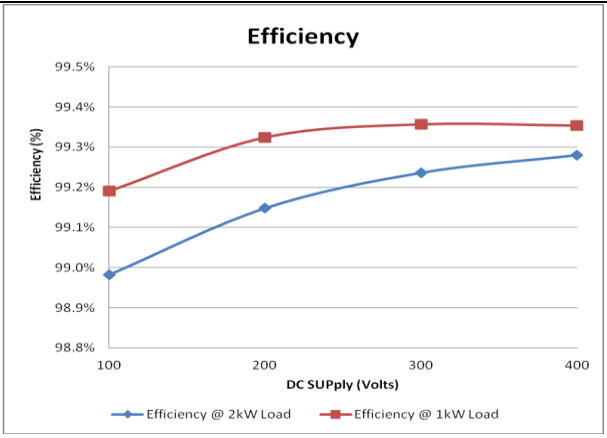

Fig. 7b An efficiency plot derived from Fig. 7a.

The output waveform created by the voltage selection MUX base-board is shown in *Fig. 6b*. The small steps are clearly seen and it is apparent that the waveform is very close to a rectified sinewave. The logic signal also shown in *Fig. 6b* drives the Reverser H-bridge to make the output AC. The small steps are smoothed by the PWM Blender, which is then added to the output to complete the synthesis of the sinewave.

The power loss and efficiency test results for the active transformer are shown in *Fig. 7a* and *Fig. 7b* respectively. The input voltage is varied for no-load and two nominal loads of 1kW and 2kW, at an input to output voltage ratio of 400/250. The same meter was used for measuring the input and output voltages and the calibration of the current meters were checked against each other. The measurements were taken at steady-state DC, so the errors are expected to be small. The efficiency is above 99% for both loads. At no load the losses show a square law dependence on the supply voltage, which implies the losses are mostly due to resistive winding losses from the magnetizing current. As the load is increased, the losses also follow a square law as expected, with losses due to the resistance of the MOSFETs and windings.

5. Discussion

Adiabatic switching of the transformer power MOSFETs eliminates power losses associated with switching. This allows the transformer to operate at a high frequency with standard low voltage silicon MOSFETs, whilst still achieving low losses. It is anticipated that use of GaN transistors would further reduce losses, giving improved power density and efficiency.

The transformer switching waveform has a relatively slow dv/dt, which reduces the high frequency EMI that might otherwise have been created. It also reduces the currents in the transformer winding capacitances to ground, reducing the stress on the insulation. Similarly, the adiabatic charging of the MOSFET gate capacitances allows a significant amount of gate charge and energy to be efficiently recovered by the gate transformer magnetizing inductance. The net effect of these adiabatic circuits is to dramatically reduce switching losses and change the trade-off between switching and conduction losses. This is clearly seen in the plots of losses, indicating that the principle loss mechanism throughout is resistive. Indeed, more MOSFETs may be used in parallel to increase the efficiency further without negative consequence. At 2kW load, and 400V in, 250V out, the losses are just under 16W. Even considering the compact size of the converter, 16W can be dissipated easily with a modest temperature rise by air convection alone.

The active ripple compensation technique described in this paper achieves far better ripple cancellation with a much smaller capacitor bank than the conventional approach of connecting the capacitors directly across the DC supply rails. The latter approach can only ever use a small proportion of the energy storage capability of the capacitors by virtue of the small voltage change. Indeed, the smaller the voltage ripple, the lower the capacitor storage utilisation.

Series cascaded H-bridges with a multi-winding transformer can be identified as a feature of the Uniflex high voltage modular power converter [6]. The use of a separate output phase to actively store energy in a capacitor bank is also proposed in the Uniflex project [7]. However, this is the first time that such a system has been shown to give a compact, efficient and low EMI converter for DC-AC conversion at domestic mains voltages. The Uniflex project was intended for high voltage grid applications: Thus we anticipate that some of the features proposed here will be applicable to higher power converters in the future.

6. Conclusions

The converter described in this paper exhibits very low power loss and high efficiency (greater than 99%), leading to compact dimensions and high power density.

This is possible because there are almost zero losses associated with switching of the transformer power windings or the gate drives to these power switches. This allows for an entirely different set of engineering trade-offs that are optimised for minimum conduction losses. This is in complete contrast to conventional high-speed hard-switching topologies, in which switching losses are invariably dominant, and a difficult trade-off between conduction and switching losses has to be found. Indeed, the converter prototype built here has many more MOSFETs connected in parallel to achieve low conduction losses than would be practical in a hard-switching converter, in this case without any negative consequence.

It is worth noting that whilst conventional resonant topologies also offer lossless switching and high efficiency, this is typically only over a narrow power band. Also they are notoriously difficult to initialise and control. Further to this, the converter described here produces a high fidelity output AC sine wave with little need for output EMI filtering.

7. References

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Appendix: Biographies

John Wood is a director at Silicon Contact Ltd. He has over 30 granted patents to his name in the fields of Rotary Travelling Wave Oscillators, power semiconductors and driver circuits. John founded MultiGig Ltd in 2000, which was subsequently acquired by Analogue Devices.

Ed Shelton studied Engineering at Cambridge University and graduated with a MEng in 1997. Since that time he has worked as an engineering consult developing high tech products. More recently Ed worked at Amantys Ltd. He is now working at Cambridge University.

Dr Kevin Rathbone is a robotics and mechatronics consultant. He holds a degree in mathematics and a diploma in computer science from Cambridge University, as well as a PhD in robotics and neuro-computing from Sheffield University.

Dr Mehdi Baghdadi received his PhD from Cambridge University in 2015. He is currently a lecturer at the Faculty of Science and Engineering, University of Greenwich.

Tim Regan is a director at Silicon Contact Ltd. He specializes in semiconductor design, providing tools and services to the silicon foundry industry. He is the the director of In2Fab.

Dr Patrick Palmer obtained his PhD from Imperial College London. In 1985 and was appointed to the Electrical Engineering Division at Cambridge University. In 2010 Patrick founded Amantys Ltd, which has recently been acquired by MR GmbH.