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Thermal-mechanical Modelling of Power Electronic Module Packaging

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Abstract

In this paper the reliability of the isolation substrate and chip mountdown solder interconnect of power modules under thermal-mechanical loading has been analysed using a numerical modelling approach. The damage indicators such as the peel stress and the accumulated plastic work density in solder interconnect are calculated for a range of geometrical design parameters, and the effects of these parameters on the reliability are studied by using a combination of the finite element analysis (FEA) method and optimisation techniques. The sensitivities of the reliability of the isolation substrate and solder interconnect to the changes of the design parameters are obtained and optimal designs are studied using response surface approximation and gradient optimization method.

1. Introduction

Power electronic modules(PEMs) are widely used in aerospace and automotive applications for the conversion and control of electrical power. A power module consists of several layers of insulator such as ceramic, conductor, and semiconductor, some metal wires, encapsulations, metal bars and the casing [1]. They are assembled together in the packaging process to form the power electronic circuit and the mechanical structure. Power electronic modules usually dissipate large amount of heat and operate in harsh environments. The stresses caused by the thermal, mechanical and electric voltage/currents greatly affect the long term reliability of these devices. The reliability of a power module is in general determined by the geometric design, choice of material and manufacturing technologies used. Since there are many different materials and joining technologies involved in a power module, it is a great challenge to the electronics packaging industry to address the power module reliability issues from the very early design stages of the product manufacturing cycle.

Two component structures are discussed in this paper: the isolation substrate and the chip mount-down solder interconnect. Of all the components in a power module, the alumina or AlN isolation substrates and the bonded copper conductor layer are the basic structures on which all other components are built on. The delamination of the copper tracks is an important reliability issue [2] whereas the solder interconnect of the chip mount-down is one of the major failure mechanisms [3]. Therefore the reliability of these two structures of the power module are fundamental to the reliability of the whole module and have attracted much research interest [4, 5, 6,7]. In this paper direct copper bonding (DCB) substrate and chip mount-down solder interconnect under thermal-mechanical loading conditions are modelled in order to understand the stress state in varying designs so that a physics-of-failure method can be used to predict the substrate's sensitivity to design parameters and the optimal design under certain constraints.

2. Isolation Substrate

The isolation substrate is a critical component in a PEM. Its functions are to provide mechanical support for other component and to electrically isolate the mounting plates and heat sink from the conductors wirebonds and semiconductor components. The isolation substrate is formed from a ceramic plate – usually alumina or Aluminium Nitride (AlN). A thin layer of copper (metallisation) is directly bonded to both sides of the ceramic. The copper layer on one side of the ceramic is etched to form a number of conductors.

To assess the substrate design the magnitude of the direction perpendicular to the substrate plane, i.e. the peel stress, induced by a thermal load has been selected as a performance metric. A response surface optimisation approach [8], has been used to evaluate optimal design and parameter sensitivity. The response surface has additionally been used in conjunction with parameter uncertainty data and a Monte-Carlo algorithm [9,10] to produce peel stress distribution data, an indicator toward component/product lifetime.

In order to determine the stresses induced by thermal load a numerical model has been developed. The Finite Element software package ANSYS [www.ansys.com] has been used to model the stresses and deformation of a simplified isolation substrate. The substrate geometry is symmetric about two axes. This symmetry is exploited, thus only a quarter of the isolation substrate tile structure has been modelled.

In order to reduce the number of degrees of freedom of the problem, shell elements were used. Two layers of shell elements were used for the ceramic layer to capture the behaviour in the ceramic close to the interface between the etched copper conductor and the ceramic more accurately. The layer close to that interface has a fixed thickness of 0.04mm regardless of the total thickness of the ceramic layer. This layer will be referred to as the top ceramic layer in this paper. Figures 1 and 2 shows a typical mesh and the normal stress distribution in the top ceramic layer. The FEA model geometry consists of two materials. The copper metallisation is subject to stresses near or in excess of the yield stress. It has therefore been modelled as an elastic-plastic material. The ceramic substrate is a brittle material which exhibits only limited plasticity at very high temperature and is therefore modelled as an elastic material. The material properties used in the simulation are listed in Table 1, in which E,

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ν, α, σ_y, and ε are the Young's modulus, the Poisson's ratio, the coefficient of thermal expansion (CTE) and the yield stress, respectively.

The damage indicator used in this work is the stress but at the bi-material interface the extrema are expected to be very mesh-dependent. Therefore, the elements with the highest stress magnitudes are identified, the stress values for these elements are volume averaged and the results are used as the damage indicator.

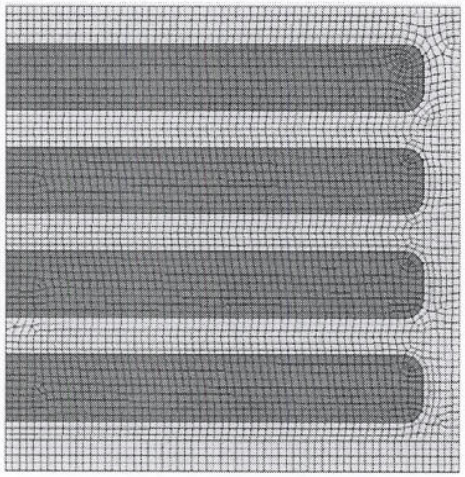

Figure 1: Typical FE model of the isolation substrate model.

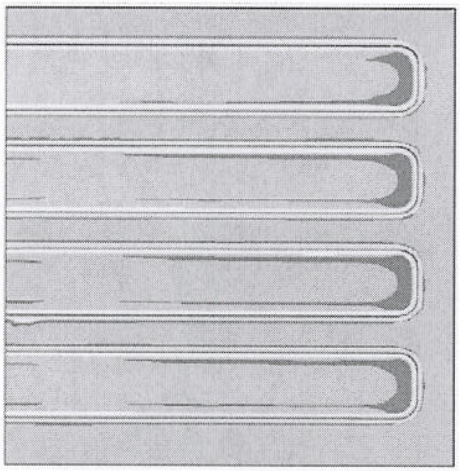

Figure 2: Out-of-plane normal stress distribution at the top ceramic layer.

Table 1: Material properties in the isolation substrate model.

	E(GPa)	ν	CTE(ppm/K)	σ_y(MPa)	ε (MPa)
AlN	310	0.24	5.6		
Cu	103.42	0.3	17	172	425

The design of experiment (DOE) [11,12] and the least squares methods [13] were used in order to form a response surface function. The substrate tile design has been described using six parameters. A random Latin Hypercube[14,15] method was used to select 28 design points within the predefined permissible range of each of the 6 parameters. The ANSYS FEA model was used to determine the peak peel stress within the substrate geometry in response to each of the discrete designs. The least square method, as implemented in the VisualDoc® package [16] fits a polynomial function consisting of linear, interaction and quadratic terms to the simulation data. The response surface is a function giving a value for the response variable (stress/lifetime/etc.) in reaction to a set of design variables. The general form of the response surface equation with six scaled design variables (labelled x_1 to x_6) is given in Equation 1. The design variables are scaled so that they take values between -1.0 and +1.0 as they vary over their permissible range. With this scaling the relative influence of the variables can be determined from the relative magnitude of the coefficients (a_0 to a_{27} in this case). These sensitivity results are shown in Figures 3-5. It can be concluded from the results that the thickness of the ceramic substrate, conductor spacing and conductor corner radius are the most important design parameters. The optimal design for the substrate can be determined from finding the minima of the response surface.

$$
\begin{aligned}
F(x) = \\
& a_0 + a_1x_1 + a_2x_2 + a_3x_3 + a_4x_4 + a_5x_5 + a_6x_6 + \\
& a_7x_1x_2 + a_8x_1x_3 + a_9x_1x_4 + a_{10}x_1x_5 + a_{11}x_1x_6 + \\
& a_{12}x_2x_3 + a_{13}x_2x_4 + a_{14}x_2x_5 + a_{15}x_2x_6 + a_{16}x_3x_4 + \\
& a_{17}x_3x_5 + a_{18}x_3x_6 + a_{19}x_4x_5 + a_{20}x_4x_6 + a_{21}x_5x_6 + \\
& a_{22}x_1^2 + a_{23}x_2^2 + a_{24}x_3^2 + a_{25}x_4^2 + a_{26}x_5^2 + a_{27}x_6^2
\end{aligned}
\qquad (1)
$$

Once the design engineer has determined the optimal design the component can progress to the manufacturing stage. The manufacturing process is imperfect and the final product will have small deviations from the design specification. These deviations or uncertainties have an impact on the performance and reliability of the product. In order to demonstrate how the manufacturing uncertainties impact on product reliability a Monte-Carlo method has been used in conjunction with the response surface function to evaluate the distribution in peel stress magnitude in a sample of components.

The Monte-Carlo method utilises the response surface to determine the stress in response to a set of design parameters. These design parameters are obtained by combining the optimal design values and an uncertainty value. In this work the uncertainty values have been generated by a Box-Muller transform [17]. The Box-Muller transform generates these values in a normal distribution around a mean (the optimum value). The magnitude of the standard deviation can be determined

from manufacturing quality control processes. However, in this work the simplification of setting the standard deviation to 0.5% of the optimal value has been made. The algorithm was used to produce a total of 10 million sample points. The resulting peel stress was evaluated for each. The distribution of peel stress is shown in Figure 6. This distribution shows that, with a standard deviation of 0.5% of the optimum value, the peel stress results vary over a substantial range, impacting significantly on the overall component/product lifetime. This result shows that if the stress for the deterministic optimal design satisfies the design requirement there is still a possibility that the product would fail because of the manufacturing uncertainties.

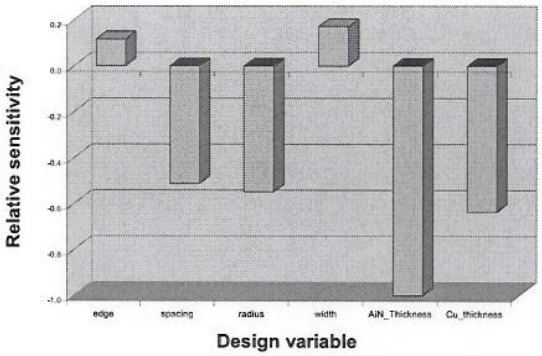

Figure 3. Sensitivity analysis – Linear terms.

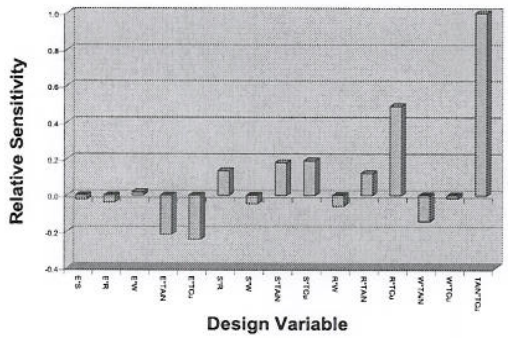

Figure 4. Sensitivity analysis – Interaction terms.

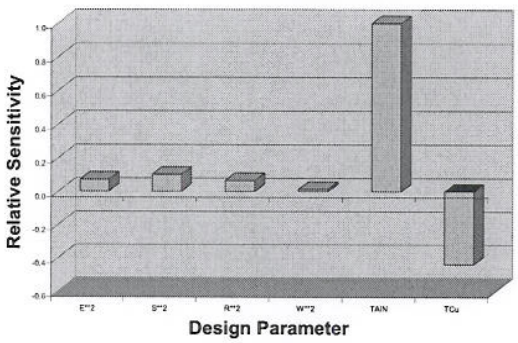

Figure 5. Sensitivity analysis – Quadratic terms.

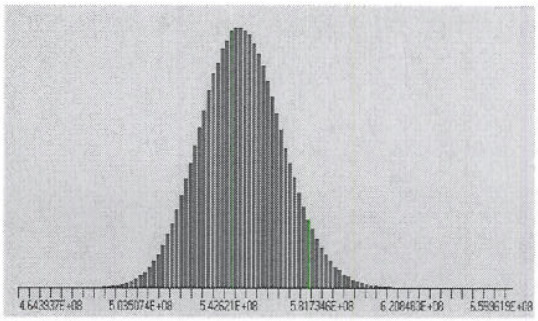

Figure 6. Peel Stress Distribution -10 million samples.

3. Chip Mount-down Solder Interconnect

Chip mount-down solder interconnects provide mechanical support to the chip and electrical connection from the chip to other components in the electric circuit. Figure 7 shows a simplified 2D chip mount-down interconnect model. Only one half of the device needs to be modelled because of the symmetry. The elastic material properties used in the modelling are listed in Table 2.

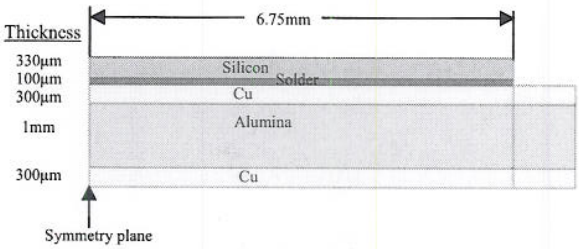

Figure 7. The basic 2D chip mount-down model.

Table 2: Material properties used in the modelling.

	E (GPa)	ν	CTE (ppm/K)
Sn3.5Ag	54.05-0.193T	0.4	21.85+0.02039T
63Sn37Pb	36.68-0.56T	0.4	24
Silicon	113	0.29	3
Cu	115	0.31	17.3
Alumina	370	0.22	7.4

Solder fatigue fracture is assumed to be the failure mechanism. Two solder materials are considered in this work: the eutectic SnPb solder and the Sn3.5Ag lead-free solder. Because of the high homologous temperature of solder alloys, the deformation of these solders is modelled using a creep law. The strain rate is represented by Equation 2.

$$\dot{\varepsilon}_{cr} = A \times \sinh^{n}(\alpha\sigma_e)\exp(\frac{-Q}{RT}) \quad (2)$$

where R is the gas constant, T is the temperature in Kelvin, σ_e is the von Mises equivalent stress, A, n, α, Q are material constants and the values are listed in Table 3 [18].

Table 3: Creep parameters for solder materials.

	A(s)	n	α (1/MPa)	Q/R
SnPb	9.60E+04	3.3	0.087	8110
SnAg	9.00E+05	5.5	0.06527	8690

The first part of the work on solder interconnect is to obtain the damage indicators and evaluate effects of temperature range and median temperature on the fatigue life of chip mountdown solder interconnect. Four temperature profiles have been used in the modelling. The ramp and dwell times of the profiles are all 15 minutes and the temperature extremes are listed in Table 4.

Table 4: Thermal cycling temperature profiles. The unit in Celsius °C.

Cycle	Tmin	Tmax	Tmed	ΔT
1	-55	125	35	180
2	-25	155	65	180
3	-40	110	35	150
4	-10	140	65	150

The plastic work density per temperature cycle, ΔW, has been used as the damage indicator. Approximately, the fatigue lifetime is inversely proportionally to ΔW [18].

The multiphysics software package PHYSICA [19] has been used to carry out the modelling. Figure 8 shows a typical distribution of the accumulated plastic work density in the solder interconnect. The maximum ΔW value is found at the chip-solder interface at the edge of the solder layer, and this is the location where cracks initiate. The value of ΔW around the most damaged location has been used as an indicator of the reliability of the chip mountdown interconnect.

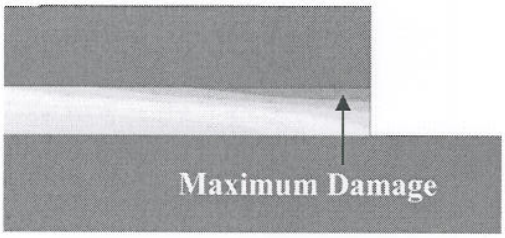

Figure 8: Typical distribution of accumulated plastic work density in solder joint.

The results are listed in Table 5. For SnAg solder interconnect, the ΔW value for Cycle 1 is about 27% higher than cycle 4 making it the most damaging temperature profile. The results also suggest that for temperature profiles with the same median temperature, the temperature range determines lifetime while for temperature profiles with the same temperature range the lower the median temperature the lower the lifetime.

Table 5: Plastic work per cycle.

Test Cycle	ΔW (MPa)	
	SnAg	SnPb
1	0.37	0.43
2	0.34	0.36
3	0.29	0.33
4	0.27	0.28

For the SnPb solder, a model relating ΔW to crack initiation and propagation rate can be expressed as:

$$N_0 = 5.42 \times 10^{7} / \Delta W \quad (3)$$

$$\frac{dl}{dN} = 5.792 \times 10^{-14} \Delta W^{1.13} \quad (4)$$

where N_0 is the number of cycles to crack initiation and l is the crack length and N is the number of cycles. The results are listed in Table 6.

Table 6: Number of cycles to crack initiation and crack propagation rate for SnPb solder interconnect.

Cycle	N_0	dl/dN (μm/cycle)
1	126	0.135
2	150	0.111
3	162	0.101
4	196	0.081

The second part of the work on solder interconnect is to analyse how reliability is affected by design variables. Design of experiment (DOE) and response surface methods (RSM) have been used to calculate the reliability sensitivity parameters for the changes in the die width, solder and substrate thickness, and gradient optimization method has been used to find the optimal design parameters [8]. The design space is defined in Table 7.

Table 7: Design space for the optimization of solder interconnect.

	Variable name	min	max	median
Die width	x_1	47.25	87.75	67.5
substrate thickness	x_2	1.4	2.6	2
solder thickness	x_3	0.7	1.3	1

A 27 points DOE was used. The plastic work density ΔW was defined as the objective function. The maximum von Mises stress in the die is an important response function to monitor because as the solder joint becomes more reliable the stress in the die may exceed the die strength. Figure 9 shows the location where these two functions are defined.

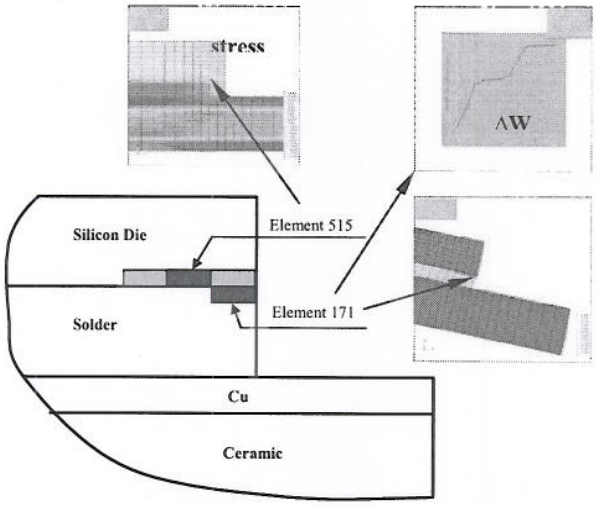

Figure 9: Locations where the stress and ΔW objective functions are defined.

For each design point in the DOE a FEA simulation is carried out and the results are then fitted to a quadratic response surface using the general optimization software VisualDoc®. In this analysis the temperature profile has a minimum temperature of -25°C, a maximum temperature of 125°C, a dwell time of 15 minutes, and a ramp time of 15 minutes. The resulting ΔW response surface has been expressed in Equation 5.

$$\Delta W(x_1,x_2,x_3) = 798700 + 36580x_1 - 3.2654\times10^7 x_2 - 2.7605\times10^8 x_3 + 6.8587\times10^6 x_1x_2 - 2.7435\times10^7 x_1x_3 + 5.5556\times10^8 x_2x_3 + 1.3548\times10^5 x_1^2 + 8.4877\times10^9 x_2^2 + 8.0247\times10^{10} x_2^2 \quad (5)$$

This analytical response surface equation can then be used to find the optimal design and calculate the sensitivity with regard to any objective function and any location in the design space. The first sign of the relative importance of the variables can be found in the coefficient of the linear terms. Obviously, solder thickness has the greatest absolute linear coefficient value and therefore is therefore expected to be the most important variable. The fact that its value is negative means that ΔW decreases as solder thickness increases.

The sensitivity with regard to each design variable can be defined as the derivative of Equation 5. Because the equation is quadratic sensitivity is location dependent. For example at the centre of the design space, the sensitivity values with regard to the three design variables are $8.9\text{x}10^4$, $2.3\text{x}10^6$ and $-1.16\text{x}10^8$ respectively. This again shows that solder thickness has the greatest impact on the fatigue life of the chip mountdown solder interconnect.

The response surface has also been used to find the best design, or the design with the lowest ΔW, in the specified design space. Instead of using a direct method, the optimization was carried out using the response surface in order to save computing efforts. The optimal design for minimum ΔW has been detailed in Table 8.

Table 8: Optimal design of the chip mountdown.

	Initial	Optimal
ΔW (kJ)	585	557.7
Die stress (MPa)	80.3	86
x_1 (m)	0.0675	0.0668
x_2 (m)	0.002	0.00147
x_3 (m)	0.001	0.0013

Compared with the initial design, the value of the objective function ΔW has an improved by about 5%. It is important to note that the maximum stress in the die has increased by about 7%. This stress is still low compared to the strength of the die but if die cracking is possible the optimization process should include a constraint on the maximum stress in the die.

Following the deterministic optimization analysis, the optimisation with uncertainties is now being carried out in which the stress in the die is constrained to the die fracture strength and the design parameters were all assumed to have a normal distribution. The results which include the optimal design results and n-Sigma design results will be published elsewhere.

4. Conclusions

Thermal-mechanical computer modelling techniques have been used in conjunction with numerical optimization tools to evaluate the reliability of isolation substrate and chip mountdown solder interconnects. For the isolation substrate the conductor edge distance, the conductor corner radius and the substrate thickness have been found to be the most important factor affecting the reliability. For the chip mountdown the thickness of the solder interconnect that has the strongest effect on lifetime. For the eutectic SnPb solder the number of

cycles to initiation and crack propagation rate have been obtained for four temperature profiles.

Acknowledgments

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